Brandon Lo

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EDUCATION

University of California, Los Angeles (UCLA) — **Los Angeles, California**

Bachelor of Science in Computer Science and Engineering - GPA: 3.78 — Expected June 2025

Master of Science in Computer Science — Expected June 2026

- **Relevant coursework:** Algorithms, Data Structures, Software Construction, Object-Oriented Programming, Operating Systems, Computer Organization, Theory of Computation, Data Science, Machine Learning, Circuits and Design, AI

SKILLS

Technical Skills: Java, C++, C, C#, Python, SQL, HTML, CSS, JS, Node.js, MongoDB, Verilog, Linux, API design, Git
Interpersonal Skills: Communication, Teamwork, Organization, Leadership, Awareness, Adaptability, Building Relationships

WORK EXPERIENCE

Amazon Web Services (AWS) - Cloud Computing and APIs — **Seattle, Washington**

Software Developer Engineering Intern — June 2024 - Present

- Integrate Perfetto into the Trainium (ML Accelerator) neuron profiler, enhancing performance and event rendering by modifying the profile output and plugin features, reducing delay by 10+ sec for 100,000+ users (Python, JSON, Golang)
- Optimize ML models to efficiently process large datasets, reducing computation time and improving scalability

ScAI Lab - UCLA Scalable AI Research Lab — **Los Angeles, California**

Machine Learning Researcher — March 2024 - Present

- Implement, validate, and integrate an optimized machine learning algorithm for the Bellman-Ford algorithm, achieving significant performance gains and increased accuracy by ~72% on large-scale datasets compared to existing AI models
- Co-authored a comprehensive research paper, highlighting potential impact of the work on real-world network analysis

Stellant Systems - Aerospace and Defense Products — **Torrance, California**

Software Engineering Intern — June 2023 - September 2023

- Developed software solutions using C# and Visual Basic to reprogram the continuity isolation station, used in effectively identifying and resolving current leakage issues 23% faster in all traveling wave tubes manufactured in the U.S.
- Automated air gauge system using PHP/MSSQL, facilitating data integration of tube diameters into a centralized database

Sensing and Robotics for Infrastructure Lab - UCLA Research Lab — **Los Angeles, California**

Tightly-Coupled, Graph-Based DVL/IMU Fusion Project Lead — April 2023 - September 2023

- Designed and implemented a custom DVL factor by architecting a robust class structure derived from existing preintegration classes within GTSAM, enhancing the accuracy of sensor fusion algorithms
- Created unit tests using C++ to validate the factor's functionality and ensure reliable performance in real-world scenario

FitDrive - Fitness Trainer/Client Application — **Toronto, Canada**

Software Engineering Intern — June 2020 – July 2020

- Implemented UI/UX design and backend development using HTML and Swift, resulting in seamless integration of frontend and backend functionalities (timer, calendar, touch-free interface) and improved user engagement

STUDENT ORGANIZATION EXPERIENCE

Rocket Project at UCLA - *Project Ares Software and Prometheus Avionics Lead* — September 2022 - Present

- Utilized EagleCad to design and optimize rocket components, integrating live flight data for real-time monitoring/analysis
- Built and maintained code that powers ground systems microcontrollers, DAQ GUI, and avionics GUI (C, C++, Python)

PROJECTS (https://github.com/brandonlo11) (https://brandonlo11.github.io/Portfolio-Website/)

Custom AI Chatbot — July 2023

- Developed AI chatbot using LlamaIndex and GPTIndex, incorporating custom knowledge bases for personalized interactions and leveraging GPT-3's language model for human-like responses (Python)

BSwipe Website — March 2023

- Leveraged the MERN technical stack to develop and deploy a fully functional website, featuring dynamic data processing, efficient client-to-backend data uploading, and server-side data search capabilities (MongoDB, Express.js, React, Node.js)

Verilog Binary Number Adder — May 2022

- Created an ALU, test bench, and other submodules in Verilog using only binary logic systems and wires without latches
- Automated 32 bit, 2 parallel 16 bit, or 4 parallel 8 bit additions, accounting for possible saturation and overflow