Lab 0: Comparator Quartus II

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Objective:

In Lab 0, we designed an 8-Bit Comparator in ModelSim. Now we must modify the lab to work in Quartus II. Then we must assign pins in order to display the functionality of our design on a DE2 Circuit Board.

Functionality an Specifications

1-Bit Comparator

First, a 1-bit comparator is created. This takes in two inputs, I0 and I1, and returns one output, Eq. The 1-bit comparator will now compare these two inputs, and check for equality. The return value, Eq, will be 0 if the inputs are not equal to each other, or 1 if they are equal to each other.

1-bit comparator VHDL file:

```
Library ieee;
Use ieee.std_logic_1164.all;

Entity equal is
Port(
I0, I1  : in std_logic;
Eq  : out std_logic);
End equal;

Architecture arch of equal is
Signal P0, P1 : std_logic;
begin
Eq <= P0 or P1;
P0 <= (not I0) and (not I1);
P1<= I0 and I1;
End arch;
```

8-Bit Comparator

Now, we will use port mapping to connect eight 1-bit comparators together in order to create the 8-bit comparator. Our inputs are "a" and "b", where these are each 8 bits long, and our output is "aeqb", which is also 8 bits long.

8-bit comparator VHDL file:

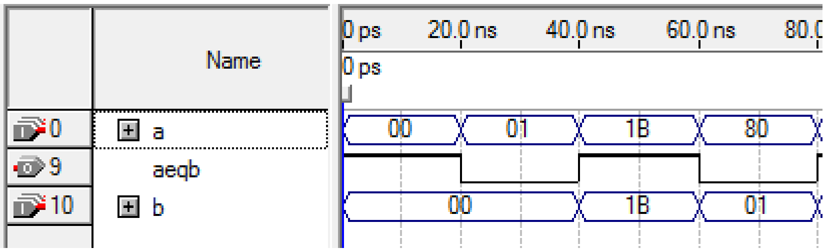
```
Library ieee;
Use ieee.std_logic_1164.all;

Entity eight_bit_equal_port is
Port (
a, b: in std_logic_vector(7 downto 0);
aeqb : out std_logic);
End eight_bit_equal_port;

Architecture arch of eight_bit_equal_port is

-- component declaration...we are telling the compiler which
-- components we want to use from the library.
component equal
Port (
I0, I1: in std_logic;
Eq : out std_logic);
End component;
```

```
signal e0,e1,e2,e3,e4,e5,e6,e7: std_logic;
begin
--instantiates eight one-bit comparators
H1: equal
port map(i0=>a(0), i1=>b(0), eq=>e0);
H2: equal
port map(i0=>a(1), i1=>b(1), eq=>e1);
H3: equal
port map(i0=>a(2), i1=>b(2), eq=>e2);
H4: equal
port map(i0=>a(3), i1=>b(3), eq=>e3);
H5: equal
port map(i0=>a(4), i1=>b(4), eq=>e4);
H6: equal
port map(i0=>a(5), i1=>b(5), eq=>e5);
H7: equal
port map(i0=>a(6), i1=>b(6), eq=>e6);
H8: equal
port map(i0=>a(7), i1=>b(7), eq=>e7);
-- a and b are equal if individual bits are equal.
aeqb <= e0 and e1 and e2 and e3 and e4 and e5 and e6 and e7;
end arch;
```

Simulation

Vector Waveform Simulation:

In order to test the 8-bit comparator, we will create a vector waveform file (.vwf) for the comparator. Then we will run this simulation, and verify the results.



Here, we can see that our results are indeed correct. Looking at the simulation, the following cases were tested (values are represented in hexadecimal notation):

Case 1: *a =* *00*

b = *00*

aeqb = 1

Case 2: *a =* *01*

b = *00*

aeqb = 0

Case 3: *a =* *1B*

b = *1B*

aeqb = 1

Case 4: *a =* *80*

b = *01*

aeqb = 0

DE2 Board Test:

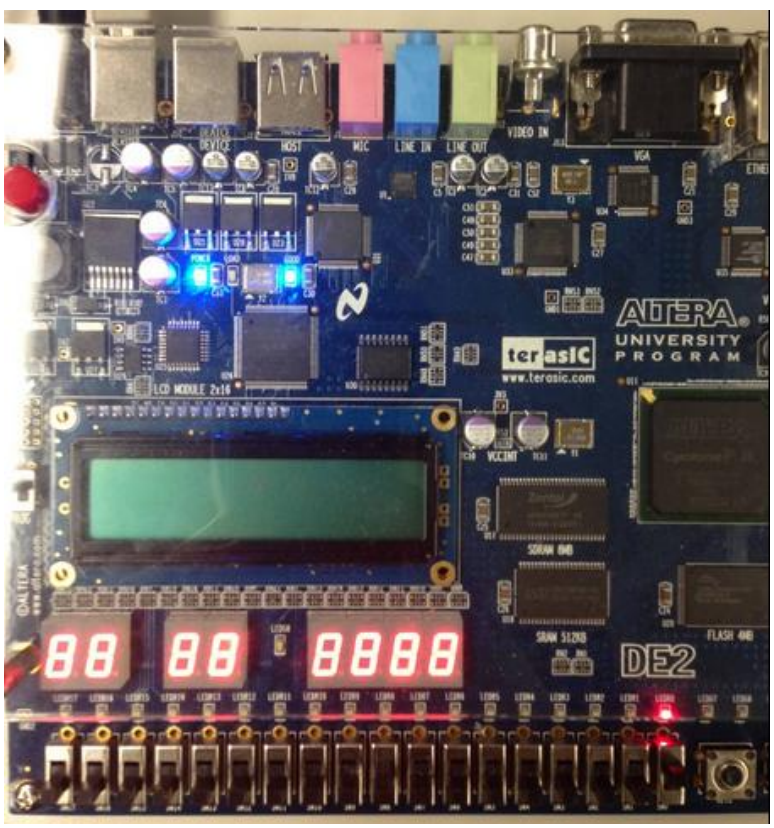
Before connecting to the DE2 board, we will first assign the correct pins to each component of the circuit. The inputs will be assigned to the board's toggle switches, and the output will assigned to the first red LED light.

Pin assignments text file:

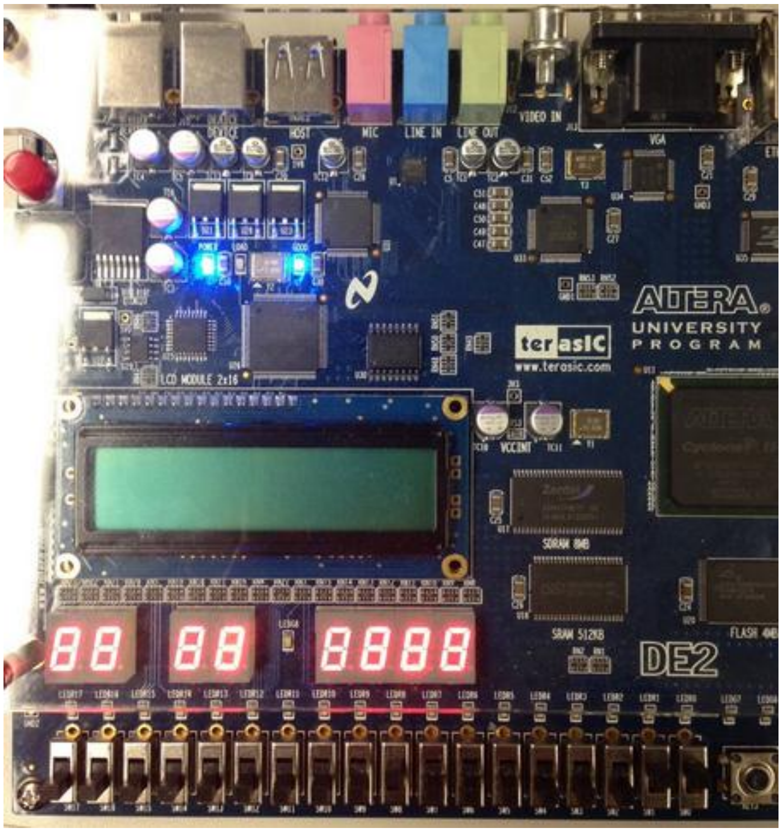
```
to, location

a[0], PIN_N25
a[1], PIN_N26
a[2], PIN_P25
a[3], PIN_AE14
a[4], PIN_AF14
a[5], PIN_AD13
a[6], PIN_AC13
a[7], PIN_C13

b[0], PIN_B13
B[1], PIN_A13
b[2], PIN_N1
b[3], PIN_P1
b[4], PIN_P2
b[5], PIN_T7
b[6], PIN_U3
b[7], PIN_U4

aeqb, PIN_AE23
```

Now we can start the simulation. The first test will check two equal inputs and verify that the LED output light turns on, indicating "aeqb" returns true. Then we will check a case where the inputs are not equal, thus resulting in the LED output light turning off.

Test 1:



Test 2:



Conclusion:

We began by importing our 1-bit comparator from the previous lab. Then we imported the 8-bit comparator which is built off port mapping eight 1-bit comparators in sequence. We learned how to run vector waveform simulations in Quartus II. We also learned how to test our circuit designs on a DE2 board, which serves as an extension to our Quartus II project. This can become very useful, and we intend to continue using Quartus II and the DE2 board for future labs.