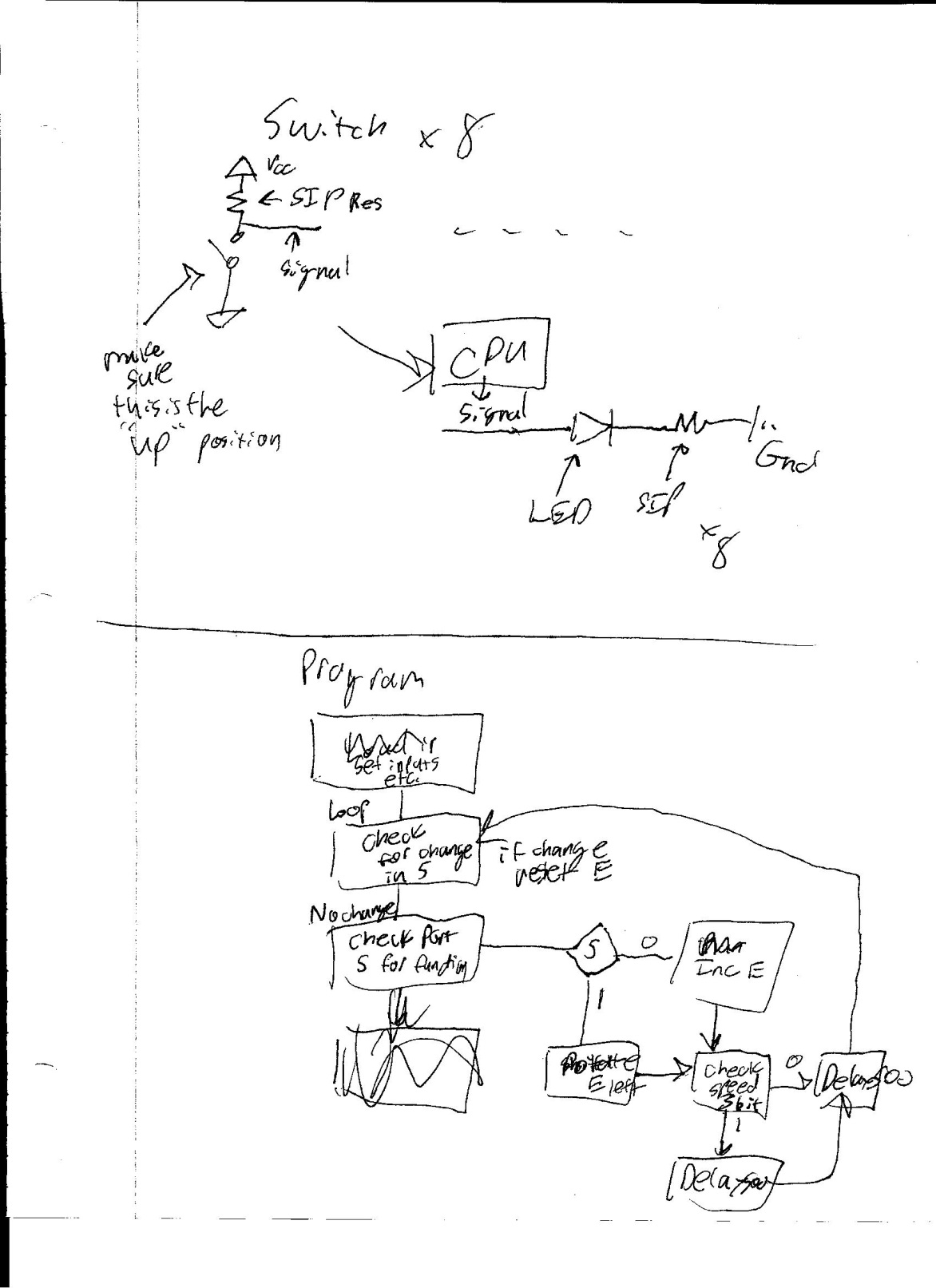
Brandon Pollack

Lab2

Report

Assembly Files Part 1

/\*Lab 2 Part 1

\* Name: Brandon Pollack

\* Section #: 1524

\* TA Name: Ivan

\* Description: Just reads port d and writes that to port e\*/

.include "ATxmega128A1Udef.inc"

.ORG 0x0

rjmp MAIN

MAIN:

.ORG 0x100

ldi R16, 0x00

ldi R17, 0xff

sts PORTD\_DIR, R16

sts PORTE\_DIR, R17

LOOP:

lds R16, PORTD\_IN

sts PORTE\_OUT, R16

rjmp LOOP

lds R17, PORTD\_IN

ASM files from part 2

/\*Lab 2 Part 2

\* Name: Brandon Pollack

\* Section #: 1524

\* TA Name: Ivan

\* Description: This is a subroutine that delays by 500 milliseconds\*/

.org 0xF00

DELAY500:

ldi R16, 0

ldi R17, 0

AGAIN:

NOP

NOP

NOP

NOP

NOP

NOP

NOP

NOP

NOP

NOP

NOP

NOP

NOP

NOP

NOP

INC R16

CPI R16, 0

BREQ CARRY

BACK:

CPI R17, 0xFF

BRNE AGAIN

BREQ RETURN

CARRY:

INC R17

rjmp BACK

RETURN:

RET

/\*Lab 2 Part 2

\* Name: Brandon Pollack

\* Section #: 1524

\* TA Name: Ivan

\* Description: inc port e\*/

INCPORTE:

lds R16, PORTE\_OUT

inc R16

sts PORTE\_OUT, R16

rjmp SPEEDCHECK

/\*Lab 2 Part 2

\* Name: Brandon Pollack

\* Section #: 1524

\* TA Name: Ivan

\* Description: rotate port e left\*/

SHIFTPORTE:

lds R16, PORTE\_OUT

ROL R16

sts PORTE\_OUT, R16

rjmp SPEEDCHECK

/\*Lab 2 Part 2

\* Name: Brandon Pollack

\* Section #: 1524

\* TA Name: Ivan

\* Description: mainfunction of part2\*/

.include "ATxmega128A1Udef.inc"

.include "Delay500.asm"

.org 0x0

rjmp MAIN

MAIN:

.org 0x100

ldi R16, 0xFF

ldi R17, 0

ldi R19, 1

sts PORTD\_DIR, R17

sts PORTE\_DIR, R16 //set the direction of the ports

sts PORTE\_OUT, R19

LOOP:

lds R16, PORTD\_IN

MOV R17, R16

ANDI R17, 0b00100000

ANDI R18, 0b00100000

CP R17, R18

BREQ NORESET

sts PORTE\_OUT, R19

CALL DELAY500

NORESET:

lds R16, PORTD\_IN

MOV R17, R16

ANDI R16, 0b00100000

CPI R16, 0b00100000

BREQ INCPORTE

//will just continue to shift port e otherwise

SHIFTPORTE:

lds R16, PORTE\_OUT

clc

ROL R16

BRCC NOCARRY

ROL R16

NOCARRY:

sts PORTE\_OUT, R16

rjmp SPEEDCHECK

INCPORTE:

lds R16, PORTE\_OUT

clc

inc R16

sts PORTE\_OUT, R16

SPEEDCHECK:

mov R18, R17

ANDI R17, 0b00001000

CPI R17, 0b00001000

BRNE HALFSEC

CALL DELAY500

HALFSEC:

CALL DELAY500

rjmp LOOP