Acoustic Neural Readings Via An Acoustically Resonant Piezoelectric Data Transmission Interface

Emma Kranich, Jade Pinkenburg, Patrick Wilcox, Brandon Wood
Cornell University

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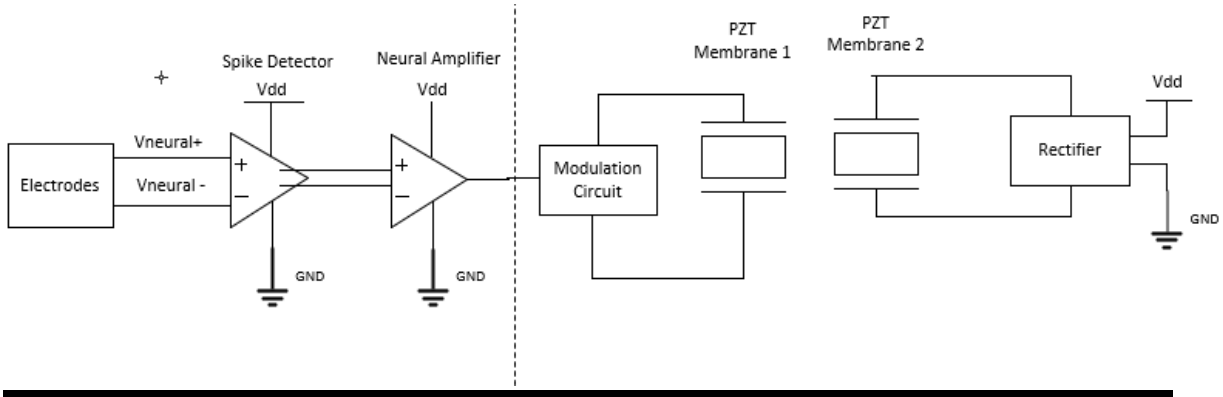
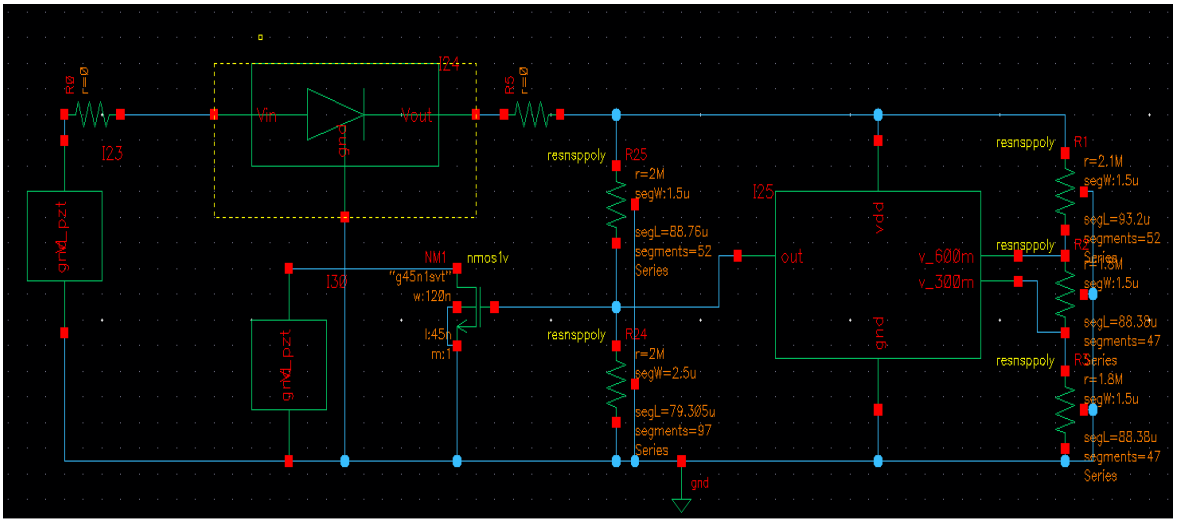




Abstract*—The frequency, intensity, and consistency of electrical pulses in the brain, known as neural spikes, is thought to be related to the onset of neurological disorders including Epilepsy, Schizophrenia, and Parkison's disease. Monitoring these (<500μV) pulses wirelessly requires high-gain, low-noise amplifiers with extreme power restrictions (on account of the micro-scale form factor needed). In this paper, we synthesize existing work to design a neural spike detector and amplifier capable of monitoring these pulses through acoustic backscattering via a piezo-electric transducer. The design was able to achieve an increase of 7.56μA of current consumption in the piezo-electric transducer. This resulted in a 342% spike in power consumption in the transmitter, allowing a data collection unit to determine that a neural spike had occurred. The average power consumption of this device was found to be 99.7μW.

1. Introduction

The rapid opening of ion channels due to positive feedback causes a spike in electrical activity of a neuron that lasts approximately 1ms. This is referred to as an action potential. Many neurological diseases are thought to be related to defects in neuronal firing of action potentials including Epilepsy, Schizophrenia, and Parkinson's Disease, though their mechanisms are unknown. By establishing communication via a piezoelectric interface, neuronal readings could be taken at a variety of locations in the brain, furthering diagnosis and treatment research for these diseases. Acoustic waves can penetrate deep into tissue, allowing the reading to take place at locations deep in the brain. By using a piezoelectric interface, it also eliminates the need for a battery or other power source on the device, which allows the device to be miniscule in size for insertion. We designed an analog circuit that can be placed on a small chip inside the brain. The circuit can detect an action potential spike, amplify the electrical signal of the neuron, then harvest the electrical signal to modulate a piezoelectric, allowing communication via acoustic waves and then powering the device to continue detecting and amplifying neural signals. This project includes various group members' interests including neuroscience and power electronics.

2. System Overview

Due to the size limitations of an implantable neural spike detector, power storage is infeasible. As a result, we turn to acoustic backscattering using a piezoelectric transducer as a means of both communication and power transfer [1]. In this method, we power the circuit using acoustic waves transmitted to a piezoelectric transducer (Section 4) and use the induced voltage to power both a neural amplification circuit (Section 8) and a spike detection circuit (Section 7). Power is first passed through a CMOS rectification circuit (Section 6) to provide a stable DC supply for both amplifiers. The amplified signal is then fed into a modulation circuit (essentially a MOSFET placed in parallel with the piezoelectric transducer, Section 5). This modulation presents a signal-dependent impedance in parallel with that of the transducer. This change in impedance results in a change in Q-Factor, which in turn changes the mechanical reflection coefficient of the piezoelectric, which can be read from an external probe, facilitating the backscattering communication.

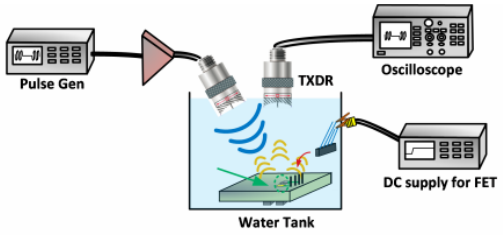


Fig 1: Example external receiver apparatus from [1].

Due to the modularity of our system, the governing equations, model parameters, analysis, and optimizations are presented, where applicable, in each subsection.

3. Design Specifications and Limitations

We sought to design a low power (< 100uW), low noise (< 5μV rms) medium-bandwidth (~10khz) neural amplifier and accompanying backscattering interface

(CMOS rectifier and piezoelectric electro-mechanical transducer). The full specifications for our design are tabulated in below (Table 1).

Specification	Desired Value	Achieved
Vddmax	1.5V	1.16V
Maximum Power Consumption	150μW	147μW
Average Power Consumption	<100μW	99.8μW
Maximum Noise	5μVrms	4.2μV rms
Minimum Bandwidth	>100Hz-2kHz	10 kHz

Table 1. List of critical design specifications and achieved results.

4. Piezoelectric Transducer

A wide range of existing power delivery systems fail to meet requirements for our current application. The limited form factor prevents magnetic back scattering and power storage [1]. Additionally, we would like to avoid wired power transfer to make the system less invasive, and to allow deeper implantation. Ultrasonic backscattering, then, presents an attractive solution as safe tissue penetration and (relatively) high efficiency power transfer can be combined with (relatively) high signal sensitivity [1].

A piezoelectric device is chosen to facilitate backscattering and power delivery. We leverage existing work from two papers, authored by teams from Cambridge [1] and Oregon State [2]. Several materials are considered based on their power transfer properties at ultrasonic frequencies able to penetrate soft tissue. Among the best suited for this application include lead-zirconate titanate (PZT), polyvinylidene difluoride (PVDF), and barium titanate (BaTiO). PZT is commonly used for such applications due to its excellent power transfer properties, however, the lead content can be a concern for medical applications [1]. The best alternative, according to the Cambridge group [1], is BaTiO3, possessing similar (though inferior) power transfer properties. However, given the popularity of PZT, and the resulting availability of transfer characteristics, models, and simulations [1, 2, 6], we opt to use PZT in our circuit and posit the development of a CMOS rectifier capable of performing similarly for BaTiO as an avenue of future research.

The range of PZT-based MEM devices valid for our application include several geometries on the order of ~100μm [1] to ~4mm [2]. Above or below this range, λ/4-matching becomes essentially impossible, rendering the transfer of suitable power intractable, though the Cambridge group calculates ~20μm is the smallest possible side length, though no designs are presented for such a device.

We break from the Cambridge design, which uses a 1mm, 1:1:1 ratio cube of PZT block placed between two electrodes, instead opting for a microcantilever as used by the Oregon State group [2]. This device is constructed from a thin PZT membrane with surface dimensions 2.54mm x 2.54mm sandwiched between two electrodes (Figure 2). This was chosen both because of the superior reported power transfer characteristics, and because

of the provision of a simple circuit model for the device at (mechanical) resonant frequency.

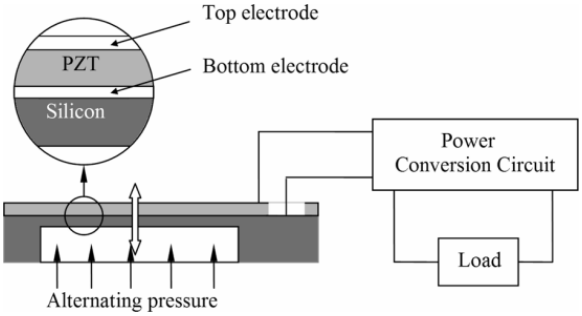
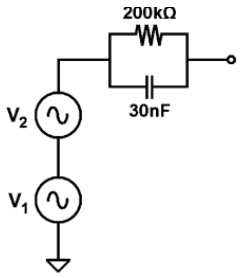


Figure 2. PZT cross section [2].

The PZT was modeled as two AC voltage sources in series with an impedance block consisting of a resistor in parallel with a capacitor. The resistor for this specific PZT was determined to be 200 kΩ and the capacitance was determined to be 30 nF. The two voltage sources represent the fundamental and second harmonic of the resonance frequency of the PZT. For this transducer, the resonant frequency is 340 Hz. The model and equations in figure 3 show the basis for the model we used [2]. This device model is directly connected to the modulation circuit and the CMOS rectifier in Cadence Virtuoso.

These equations were used to determine that $V_1(340) = 1.238V$ and $V_2(340) = .437V$. Thus, the input voltage was modeled as $V_{in} = 1.238 \cdot \sin(2\pi \cdot 340) + 0.437 \cdot \sin(2\pi \cdot 340 \cdot 2 \cdot t)$. This model was implemented in Cadence Virtuoso with ideal sinusoidal voltage sources and an ideal resistor and capacitor.



$$V_1(f) = a_1 * f^4 + a_2 * f^3 + a_3 * f^2 + a_4 * f + a_5$$
$$V_2(f) = b_1 * f^4 + b_2 * f^3 + b_3 * f^2 + b_4 * f + b_5$$

$a_1 = 2.0409 \times 10^{-8}$	$b_1 = 2.0188 \times 10^{-8}$
$a_2 = -2.8432 \times 10^{-5}$	$b_2 = -2.8541 \times 10^{-5}$
$a_3 = 1.4629 \times 10^{-2}$	$b_3 = 1.4952 \times 10^{-2}$
$a_4 = -3.2949$	$b_4 = -3.4392$
$a_5 = 2.7515 \times 10^{2}$	$b_5 = 2.9331 \times 10^{2}$

Figure 3. PZT cantilever equivalent circuit model [2].

Figure 4 is the transient plot of the output voltage of the PZT as tested in the full schematic. This figure is in the appendix.

5. Modulation Circuit

Backscattering is achieved by modulating the gate voltage of a mosfet in parallel with load of a secondary PZT in order to change the current through the PZT source model and change the amount of power in the acoustic wave that is reflected. The second PZT was used to get better resolution in transmission than if modulating the PZT used as a power source.

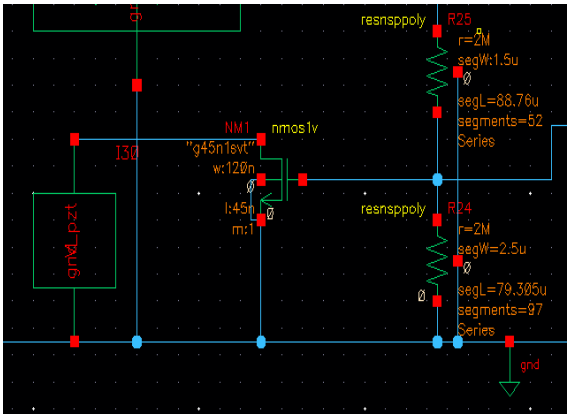


Figure 5. NM1: W = 120n, L = 45n. Vbias = 575 mV.

The modulation circuitry consists of an NMOSFET and a resistor divider for biasing. Figure 6 shows the circuitry as implemented in the full circuit.

Figure 6 shows the output current and voltage waveforms of the PZT and figure 7 shows the signal that modulated the NMOSFET. When the signal increased from 575mV to 675 mV, the PZT had to source more current at the same voltage. This 5.76 uA spike leads to a 342% jump in power consumption going from 7.49μW to 25.6μW. This power jump is measurable from an acoustic receiver. Since the waveform of the other PZT does not modulate, this change is observable and all of the abnormal modulation can be attributed to the transmission of a confirmed spike via the second PZT. Figures 6 and 7 can be found in the appendix.

6. Rectifier

The rectifier for this device consists of two transistors in parallel: a diode connected NMOS and a diode connected PMOS. The rectifier also has an off chip 500 nF reservoir capacitor for energy storage. This rectifier topology was chosen for two reasons: first was the simplicity of the design to interface with the system and the other was to use a topology that was resistant to large fluctuations in power supplied by the source due to the modulation of the PZT. The output of the rectifier is 8.06 μW which leads to a very low 8.1% efficiency. This is clearly not necessarily the best rectifier for this design, but the simplicity and large range of acceptable inputs made this design ideal for tuning the design and ensuring that the spike detector and amplifier, both power source sensitive, could be optimized. Also, much of the power delivered from the PZT is in intense, short pulses. This leads to inefficiency in converting and stabilizing the power to a relatively stable DC power source. Aslo, active diode rectifiers were designed and implemented, but the required current draw made them unfit for this system. Figure 8 shows the schematic for the rectifier. Figure 9 shows the transient current and voltage output from the rectifier as tested in the full schematic. Figures 8 and 9 can be found in the appendix.

7. Spike detector

Action potential spikes only last for approximately 1ms. These quick spikes need to be accurately detected and an output signal that is only ‘high’ during a spike must be output to the modulation unit (Fig. 15). The spike detection design was inspired by Kim’s 6-stage design [5]. However, a simplified version was optimized for our use (Figure 14). It begins with a high pass filter (Figure 10) that is a simple RC design with cutoff frequency $\frac{1}{RC} = \frac{1}{(20M)(53.7pF)}$ =931.1 rad/s. Following this, there are two cascaded current balanced instrumentation amplifiers (CBIAs) (Figure 11). The CBIAs allow for a wide bandwidth with low power consumption. The voltage difference across the top resistor (Rin) comes from the voltage difference between PM2 and PM3 (source followers). That voltage then leads to a current difference through PM2 and PM3. That current difference multiplied by the middle two resistor’s value (Rout) is the differential output. The gain is thus just the ratio of resistor values. The low pass filters

around the side return the low frequency components to self-bias. Recording only high frequency components still emphasizes spikes and lowers power consumption. In addition, the NMOS loads were added on the bottom for common mode feedback. The CBIAs use a Vdd around 0.6V and there are 2 cascaded to achieve a better gain [5].

After these, there is an analog nonlinear energy operator (NEO) (Figure 12). NEOs are known to be good in noisy circuits and allow for better power consumption than digital analysis (which requires a high sampling rate). The NEO emphasizes high frequency components and attenuates the low. The NEO consists of a differentiator and a multiplier circuit, but the multiplier circuit was left out because we decided it wasn't needed with another amplifier following the NEO and just added to power consumption. The NEO also uses 0.6Vdd and has common mode feedback added (Figure 13). The gain of the differentiator is shown below from the Kim paper, but ro_{CS} from the current source is replaced with ro from the current mirror used to bias [5].

$$A(s) = A_o \frac{sC_{DIFF}}{1 + sC_{DIFF}\left((r_{op4} // r_{op6}) + \left(\frac{1}{g_{mp5}} // r_{oCS}\right)\right)},$$

$$A_o = g_{mn2} g_{mp6} \left(r_{on2} // r_{op4}\right)\left(\frac{1}{g_{mp5}} // r_{oCS}\right)\left(r_{op4} // r_{op6}\right),$$

8. Neural Amplifier

Originally we had intended to put the neural amplifier before the spike detection system, since neural signals are generally quite weak (with spike amplitudes reaching only around 500 µV [3]). However, as described above, after testing the spike detection module we found that it was quite robust at these low voltages and was able to reliably detect spikes and filter out extraneous noise at very low voltages. For the data to be accurately transmitted over the piezoelectric interface, we needed an estimated 100 mV peak-to-peak or larger for the modulation circuit to function, so an op-amp was needed to amplify the differential signal output from the spike detector. To filter out extraneous biological noise in the system, we also aimed to introduce a low pass corner at around 10 kHz, since typical neuronal spikes have most of their energy concentrated in the 100 Hz - 7 kHz band [3]. Because the spike detection unit already filters out low frequency noise, we chose not to include a high pass corner at low frequencies. To achieve these specifications, we used a folding cascode topology (as suggested by Ng et al. for low V_{DD}) [4] followed by a cascoded common source stage for increased gain. Although adding a second stage introduces a low pole into the system, it is still far higher than the low pass corner introduced by our filtering system and the 60+ dB gain required for our amplifier to function meant that a second stage was necessary. After the proper gain was achieved, component parameters were then tuned to achieve a low current consumption of 4.2 µA and V_{DD} of 1.2V, yielding a power consumption of 5.0 µW, which was significantly lower than our already ambitious goal of 10 µW for the amplifier. Figure 16 shows the schematic design of our amplifier circuit.

Theoretical Analysis: The overall gain of the neural amplifier is equal to the product of the first and second stage gains.

For an input multiplicity of K, first stage multiplicity of N, and output multiplicity of M, the gain A_v is given by: $A_v = Kg_{mp}R_{out1}Mg_{mp}R_{out2}$, where $R_{out1} = g_{mp}r_{op}\frac{r_{op}}{N}||g_{mn}r_{on}(\frac{r_{on}}{N+K}||\frac{r_{op}}{K})$, $R_{out2} = r_{op}||r_{on}$

Because the input signals are so small, low input-referred noise is paramount to the accuracy of our system; if the incoming signal to noise ratio is too low, the neural spikes will not be recorded accurately. To accomplish this, we had to address both the flicker noise and thermal noise (equations below):

$$\frac{i_{out}^2}{Hz} = 2 \cdot (\frac{i_{diffpair}^2}{Hz} + \frac{i_{topMirr}^2}{Hz} + \frac{i_{currMirr}^2}{Hz})$$

$$\frac{i_d^2}{Hz} = 4kTg_m\gamma \qquad \frac{i_f^2}{Hz} = \frac{K_{f1}I_{DC}}{L^2f}$$

To mitigate the effects of flicker noise, the length of the first stage transistors was made significantly larger. Widths were also scaled to keep the gain within the necessary range and multiplicities were kept as low to minimize current consumption. Once the flicker noise was taken care of, we then addressed the remaining thermal noise (which was about 10 μV rms) by adjusting the widths of the input differential pair transistors in order to hit the noise spec. This spec was arguably one of the most difficult to achieve, since we had to adjust our amplifier while still maintaining high gain and low power consumption.

Bandwidth calculations for the amplifier would not be very meaningful since the dominant pole is set by the RC low pass filter on the output of the op-amp (break frequency at 1/RC). The lowest internal pole is on the output of the first stage, but this is still orders of magnitude higher than the filter pole.

Simulation Results: Running an AC simulation on the neural amplifier indicated that the gain was 72.3 dB with an input referred noise of 4.2μV and a 3-dB bandwidth of 10.8 kHz. We also achieved a CMRR of 74.8 dB and a PSRR of 75.7 dB. The gain and noise were well within spec and, after hooking it up to the spike detection unit, the system was able to amplify the signal output by the spike detector to a level appropriate for our modulation circuit. Figure 17 shows a transient plot of an amplified signal from the spike detector (same signal in Fig. 15)

9. Conclusions

Overall, the neural transducer we designed is successfully able to signal when there is a neural spike due to an action potential. When we simulated the full top-level schematic depicted on the front page, we observed clear spikes in the PZT transmitter circuit (as shown in Fig 7) which would allow a receiver module to determine that a neural spike had occurred. Further inspection indicated that the test spikes were accurately detected (Fig 15) and amplified (Fig 17) in the presence of common-mode background noise. However, after designing and simulating the entire circuit, we also discovered some interesting (and unexpected) drawbacks. First, we use two PZTs instead of one which can be problematic in terms of increasing the average power consumption. In this case we were able to keep power low but power could be lowered further with one PZT. The one drawback is that this came at a cost to resolution when we tested it. Also, the rectifier is serviceable, but a higher efficiency rectifier

could be implemented to increase the gain of the amplification stage and thus also the resolution of the spikes. All though our device met its desired specs, we would recommend improving power consumption first and then rectification to further reduce power consumption and make a more efficient, better resolution device. This project really helped us learn about system-level design, power source design, transistor-level component optimization, and the massive potential for advancements in neuroscience as applied to medical fields and academia.

10.References

[1] D.J. Seo, "Neural Dust: Ultrasonic Biological Interface," Electrical Engineering and Computer Sciences University of California Berkeley. Report.https://www2.eecs.berkeley.edu/Pubs/TechRpts/2018/EECS-2018-146.html. 1 Dec. 2018.

[2] T.T. Le, "Piezoelectric micro-power generation interface circuits" *IEEE Journal of Solid State Circuits* (Vol. 41 Issue 6), June 2006, pp 1411-1420

[3] R. R. Harrison and C. Charles, "A Low-Power Low-Noise CMOS Amplifier for Neural Recording Applications." *IEEE Journal Of Solid-State Circuits* (Vol 38, No 6), June 2003, pp 958-965

[4] K. A. Ng et al., "Implantable Neurotechnologies: a review of integrated circuit neural amplifiers." *Medical & Biological Engineering & Computing* (Vol 54, Jan. 2016, pp 45-62

[5] J. Kim, H. Lee, and H. Ko, "0.6V, 116nW Neural Spike Acquisition IC with Self-Biased Instrumentation Amplifier and Analog Spike Extraction" *Sensors (Basel)* (Vol 18, No 8), July 2018.

[6] Lu, F., Lee, H.P., and Lim, S.P., "Modeling and analysis of micro piezoelectric power generators for micro-electromechanical-systems applications." *Smart Materials and Structures*. (Vol 13). 26 Nov, 2003. pp 57-63

11.Figures

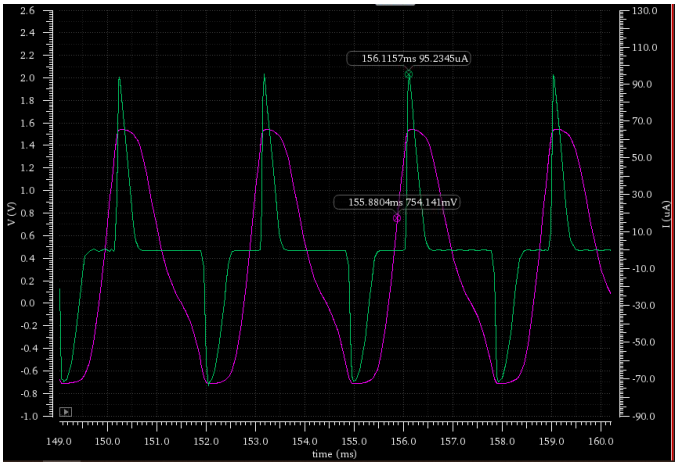


Fig. 4 (above) Voltage (pink,V) across and current (green,uA) through the power supply PZT vs time (149-160 ms), V_{Max} = 1.54V, I_{Max} = 95.2µA

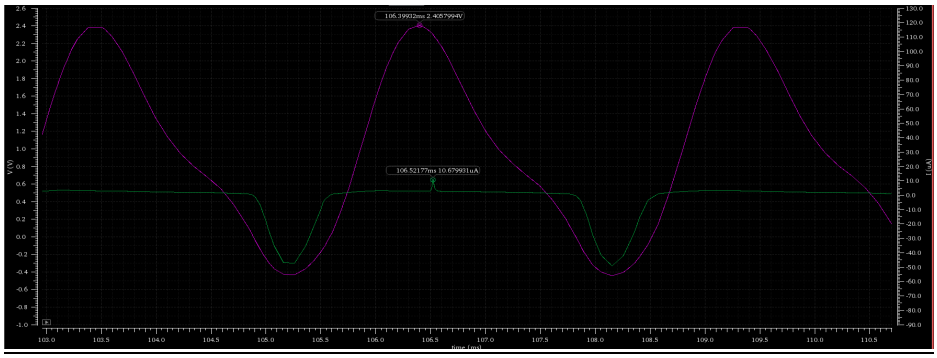


Fig. 6 Voltage (pink,V) across and current through the transmitter PZT (green,uA) vs time (100-110 ms). V_{Max} = 2.41V, I_{Max} = 10.68µA

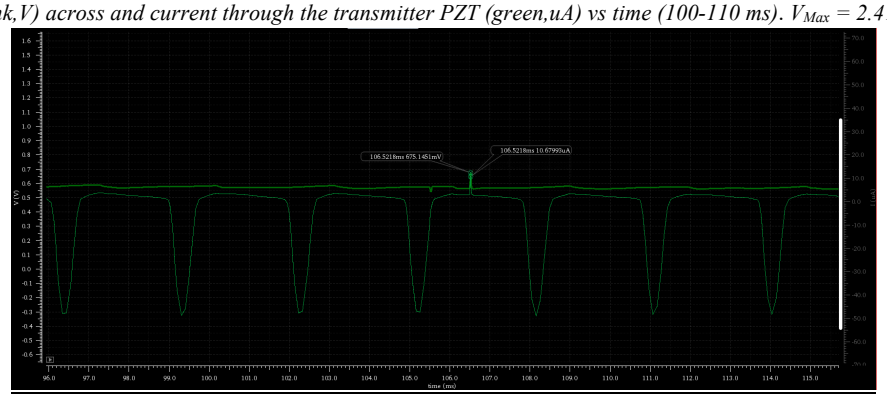


Fig. 7 Voltage modulation (top) with spike and current (bottom) through the transmitter PZT vs time (96-116 ms) . I_{Max}= 10.68µA , V_{Spike} = 675 mV

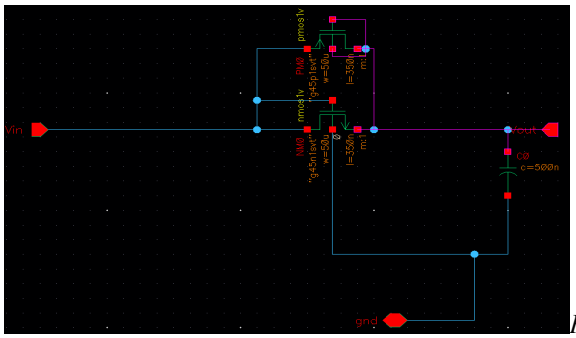


Fig. 8 Rectifier schematic.

Fig. 9 V_{DD} outputs corresponding to the current draw (green, uA) and voltage (pink, V) of the DC power rail vs time (140-160 ms). V_{Avg} =1.165V , I_{Avg} =6.91 µA

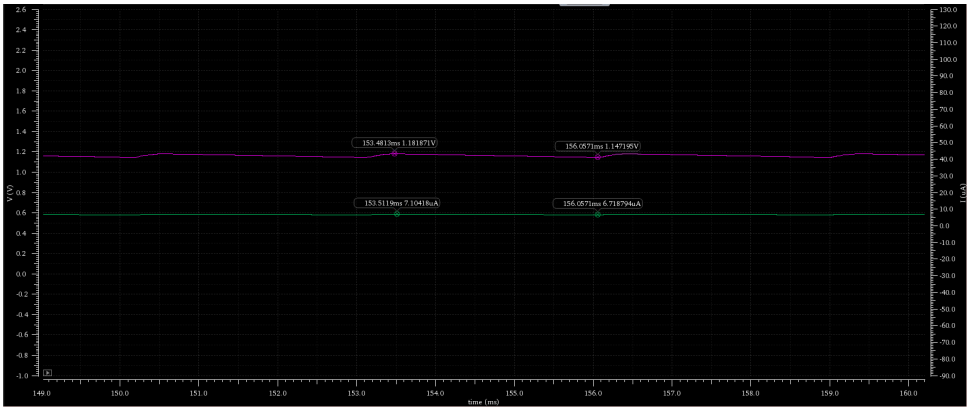


Fig. 10 High Pass Filter

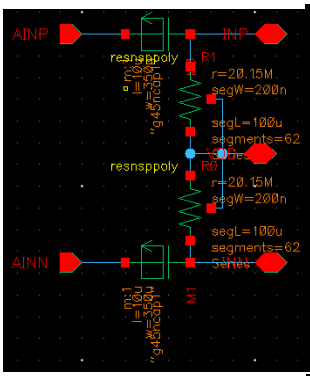


Fig. 11 CBIA

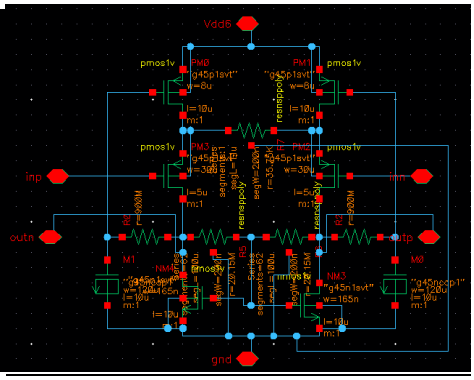


Fig. 12 NEO schematic

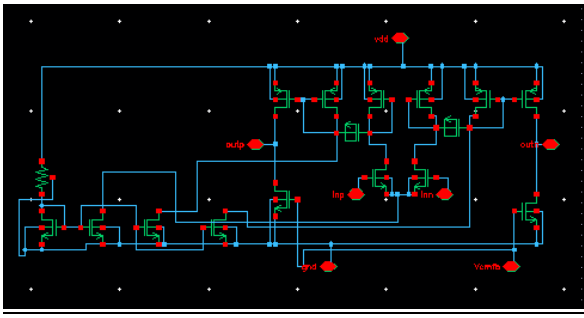


Fig. 13 NEO CMFB

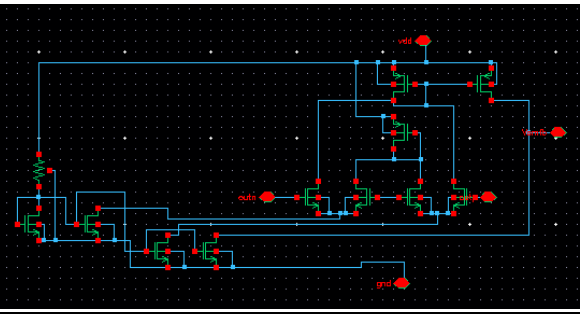
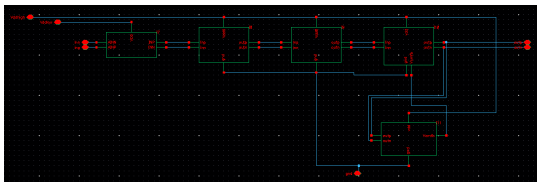
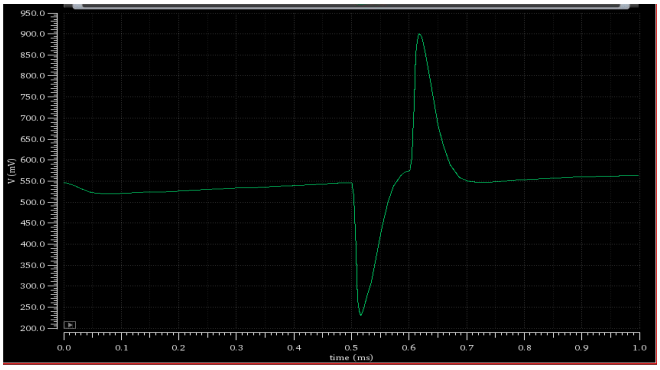


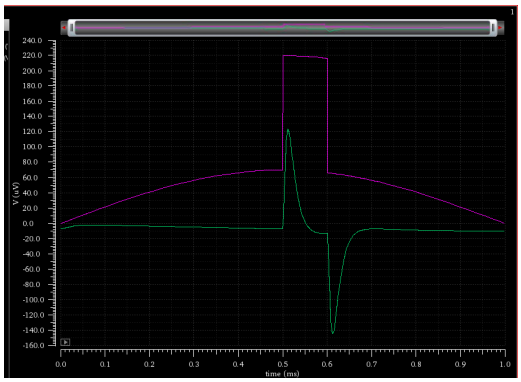
Fig. 14 Spike Detection Schematic



Below: Fig. 15 Spike Sim (pink = incoming spike, 140 uV pp, green = spike detector output, 120 uV pp) vs time (1 ms).



Top: *Fig 17: Amplified Neural Spike Voltage (~700 mV peak-to-peak) vs time (1 ms)*



Right: *Fig 16: Neural amplifier schematic. Biasing circuitry on right, amplifier stages + LPF on left*