```
    1: library STD;
    2: library IEEE;
    3: use IEEE.std_logic_1164.all;
    4:
    5: entity valid_test is
    6:
    7: end valid_test;
    8:
    9: architecture test of valid_test is
   10:
   11:     component Cache_Cell_Valid
   12:     port(
   13:         s       :   in  std_logic;
   14:         r       :   in  std_logic;
   15:         Rd_En   :   in  std_logic;
   16:         Wr_En   :   in  std_logic;
   17:         q       :   out std_logic
   18:     );
   19:     end component;
   20:
   21:     signal s_s, s_r, s_Rd_En, s_Wr_En, s_q  :   std_logic   := '0';
   22:
   23:     for asdf    :   Cache_Cell_Valid use entity work.Cache_Cell_Valid(structur
al);
   24:
   25: begin
   26:
   27:     asdf    :   Cache_Cell_Valid    port map(s_s, s_r, s_Rd_En, s_Wr_En, s_q);
   28:
   29: p   :   process
   30: begin
   31:
   32:     s_s   <=  'U';
   33:     s_Wr_En <= 'U';
   34:     s_r     <= '1';
   35:     wait for 5 ns;
   36:     s_r <= '0';
   37:     wait for 5 ns;
   38:     s_s   <=  '0';
   39:     s_Rd_En <= '1';
   40:     s_Wr_En <= '0';
   41:     wait for 5 ns;
   42:     s_s <=  '1';
   43:     wait for 5 ns;
   44:     s_s <= '0';
   45:     wait for 5 ns;
   46:     s_r <= '1';
   47:     wait for 5 ns;
   48:     s_r <= '0';
   49:     wait for 5 ns;
   50:     s_q <= '1';
   51:     s_Rd_En <= '1';
   52:     wait for 5 ns;
   53:     s_q <= '0';
   54:     s_Rd_En <= '0';
   55:     wait for 5 ns;
   56:     wait;
   57: end process;
   58: end test;
```