```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity nor3 is
 6: port(
 7:     in1     :   in  std_logic;
 8:     in2     :   in  std_logic;
 9:     in3     :   in  std_logic;
10:     out1    :   out std_logic
11: );
12: end nor3;
13:
14: architecture structural of nor3 is
15:
16: begin
17:
18:     out1 <= (in1 or in2) nor in3;
19:
20: end structural;
```