```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity SR18_Test is
 6: end SR18_Test;
 7:
 8: architecture test of SR18_Test is
 9:
10:     component SR18
11:     port(
12:         clk     :   in  std_logic;
13:         reset   :   in  std_logic;
14:         Vdd     :   in  std_logic;
15:         Gnd     :   in  std_logic;
16:         output  :   out std_logic_vector(0 to 17)
17:     );
18:     end component;
19:
20:     signal clk, reset   :   std_logic;
21:     signal output   :   std_logic_vector(0 to 17);
22:     shared variable done    :   boolean := false;
23:
24:     for pm  : SR18 use entity work.SR18(structural);
25:
26: begin
27:
28:     pm  :   SR18    port map(clk, reset, '1', '0', output);
29:
30:     c   :   process
31:     begin
32:         if done = true then
33:             wait;
34:         else
35:             clk <= '1', '0' after 5 ns;
36:             wait for 10 ns;
37:         end if;
38:     end process;
39:
40:     p   :   process
41:     begin
42:         reset <= '1';
43:         wait for 10 ns;
44:         reset <= '0';
45:         wait for 150 ns;
46:         done := true;
47:         wait;
48:     end process;
49: end test;
```