```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity Dlatch is
 6:   port ( d   : in  std_logic;
 7:          clk : in  std_logic;
 8:          q   : out std_logic;
 9:         qbar : out std_logic
10:          );
11: end Dlatch;
12:
13: architecture structural of Dlatch is
14:
15:
16:
17: begin
18:
19:   output: process(clk, d)
20:   begin
21:     if clk = '1' then
22:         q <= d;
23:         qbar <= not d;
24:     end if;
25:  end process output;
26:
27: end structural;
```