```
    1: library STD;
    2: library IEEE;
    3: use IEEE.std_logic_1164.all;
    4:
    5: entity rd_wr_hit_miss_reg_test is
    6:
    7: end rd_wr_hit_miss_reg_test;
    8:
    9: architecture test of rd_wr_hit_miss_reg_test is
   10:
   11:     component rd_wr_hit_miss_reg
   12:     port(
   13:         rd_wr       :   in  std_logic;
   14:         rd_wr_set_en:   in  std_logic;
   15:         hit_miss    :   in  std_logic;
   16:         hit_miss_en :   in  std_logic; --signal for latching hit miss
   17:         clk         :   in  std_logic;
   18:         reset       :   in  std_logic;
   19:         Gnd         :   in  std_logic;
   20:         rd_wr_o     :   out std_logic;
   21:         rd_hit      :   out std_logic;
   22:         wr_hit      :   out std_logic;
   23:         rd_miss     :   out std_logic;
   24:         wr_miss     :   out std_logic
   25:     );
   26:     end component;
   27:
   28:     signal rd_wr, rd_wr_set_en, hit_miss, hit_miss_en, clk, reset, rd_hit, wr_
hit, rd_miss, wr_miss :   std_logic;
   29:     shared variable done    :   boolean := false;
   30:
   31:     for pm  :   rd_wr_hit_miss_reg use entity work.rd_wr_hit_miss_reg(structur
al);
   32:
   33: begin
   34:
   35:     pm  :   rd_wr_hit_miss_reg port map(rd_wr, rd_wr_set_en, hit_miss, hit_mis
s_en, clk, reset, '0', open, rd_hit, wr_hit, rd_miss, wr_miss);
   36:
   37:     c   :   process
   38:     begin
   39:         if done = true then
   40:             wait;
   41:         else
   42:             clk <= '1', '0' after 5 ns;
   43:             wait for 10 ns;
   44:         end if;
   45:     end process;
   46:
   47:     p   :   process
   48:     begin
   49:         reset <= '1';
   50:         rd_wr_set_en <= '0';
   51:         hit_miss_en <= '0';
   52:         wait for 10 ns;
   53:         reset <= '0';
   54:         wait for 10 ns;
   55:         rd_wr <= '1';
   56:         hit_miss <= '1';
   57:         wait for 10 ns;
   58:         rd_wr_set_en <= '1';
   59:         wait for 10 ns;
   60:         rd_wr_set_en <= '0';
   61:         rd_wr <= '0';
   62:         hit_miss_en <= '1';
   63:         wait for 10 ns;
   64:         hit_miss_en <= '0';
   65:         wait for 5 ns;
   66:         hit_miss <= '0';
   67:         wait for 5 ns;
   68:         done := true;
   69:         wait;
   70:     end process;
   71: end test;
```