```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4: use IEEE.std_logic_textio.all;
 5: use STD.textio.all;
 6:
 7: entity Dlatch_Test is
 8:
 9: end Dlatch_Test;
10:
11: architecture test of Dlatch_Test is
12:
13:     component Dlatch
14:         port(
15:             d       :   in  std_logic;
16:             clk     :   in  std_logic;
17:             q       :   out std_logic;
18:             qbar    :   out std_logic
19:         );
20:     end component;
21:
22:     signal s_d      :   std_logic;
23:     signal s_clk    :   std_logic;
24:     signal s_q      :   std_logic;
25:     signal s_qbar   :   std_logic;
26:
27:     for a   :   Dlatch use entity work.Dlatch(structural);
28:
29: begin
30:
31:     a   :   Dlatch  port map(s_d, s_clk, s_q, s_qbar);
32:
33:     t   :   process
34:
35:     begin
36:
37:         s_clk   <=  '1';
38:         s_d     <=  '0', '1' after 5 ns;
39:         wait for 10 ns;
40:         s_clk   <=  '0';
41:         wait for 1 ns;
42:         s_d     <=  '0';
43:         wait for 4 ns;
44:         s_clk   <=  '1';
45:         wait for 5 ns;
46:         wait;
47:
48:     end process;
49:
50: end test;
```