```
    1: library STD;
    2: library IEEE;
    3: use IEEE.std_logic_1164.all;
    4:
    5: entity Decoder is
    6:     port(
    7:         Mem_Add :   in  std_logic_vector(4 downto 0);
    8:         Col_En  :   out std_logic_vector(3 downto 0);
    9:         Row_En  :   out std_logic_vector(7 downto 0)
   10:     );
   11: end Decoder;
   12:
   13: architecture structural of Decoder is
   14:
   15:     component nor3
   16:     port(
   17:         in1     :   in  std_logic;
   18:         in2     :   in  std_logic;
   19:         in3     :   in  std_logic;
   20:         out1    :   out  std_logic
   21:     );
   22:     end component;
   23:
   24:     component nor2
   25:     port(
   26:         in1     :   in  std_logic;
   27:         in2     :   in  std_logic;
   28:         out1    :   out std_logic
   29:     );
   30:     end component;
   31:
   32:     component invX1
   33:     port(
   34:         in1     :   in  std_logic;
   35:         out1    :   out std_logic
   36:     );
   37:     end component;
   38:
   39:     signal nMem_Add :   std_logic_vector(4 downto 0);
   40:
   41:     for inv0, inv1, inv2, inv3, inv4    :   invX1   use entity work.invX1(stru
ctural);
   42:     for r_off0, r_off1, r_off2, r_off3, r_off4, r_off5, r_off6, r_off7  :   no
r3    use entity work.nor3(structural);
   43:     for by_off0, by_off1, by_off2, by_off3  :   nor2    use entity work.nor2(s
tructural);
   44:
   45: begin
   46:
   47:     inv0    :   invX1   port map(Mem_Add(0), nMem_Add(0));
   48:     inv1    :   invX1   port map(Mem_Add(1), nMem_Add(1));
   49:     inv2    :   invX1   port map(Mem_Add(2), nMem_Add(2));
   50:     inv3    :   invX1   port map(Mem_Add(3), nMem_Add(3));
   51:     inv4    :   invX1   port map(Mem_Add(4), nMem_Add(4));
   52:
   53:     r_off0  :   nor3    port map(Mem_Add(4), Mem_Add(3), Mem_Add(2), Row_En(0)
);
   54:     r_off1  :   nor3    port map(Mem_Add(4), Mem_Add(3), nMem_Add(2), Row_En(1
));
   55:     r_off2  :   nor3    port map(Mem_Add(4), nMem_Add(3), Mem_Add(2), Row_En(2
));
   56:     r_off3  :   nor3    port map(Mem_Add(4), nMem_Add(3), nMem_Add(2), Row_En(
3));
   57:     r_off4  :   nor3    port map(nMem_Add(4), Mem_Add(3), Mem_Add(2), Row_En(4
));
   58:     r_off5  :   nor3    port map(nMem_Add(4), Mem_Add(3), nMem_Add(2), Row_En(
5));
   59:     r_off6  :   nor3    port map(nMem_Add(4), nMem_Add(3), Mem_Add(2), Row_En(
6));
   60:     r_off7  :   nor3    port map(nMem_Add(4), nMem_Add(3), nMem_Add(2), Row_En
(7));
   61:
   62:     by_off0 :   nor2    port map(Mem_Add(1), Mem_Add(0), Col_En(0));
   63:     by_off1 :   nor2    port map(Mem_Add(1), nMem_Add(0), Col_En(1));
   64:     by_off2 :   nor2    port map(nMem_Add(1), Mem_Add(0), Col_En(2));
   65:     by_off3 :   nor2    port map(nMem_Add(1), nMem_Add(0), Col_En(3));
   66:
   67: end structural;
```