```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity and3 is
 6: port(
 7:     in1     :   in  std_logic;
 8:     in2     :   in  std_logic;
 9:     in3     :   in  std_logic;
10:     out1    :   out std_logic
11: );
12: end and3;
13:
14: architecture structural of and3 is
15:
16:     component and2
17:     port(
18:         in1     :   in  std_logic;
19:         in2     :   in  std_logic;
20:         out1    :   out std_logic
21:     );
22:     end component;
23:
24:     signal o1   :   std_logic;
25:     for a1  :   and2 use entity work.and2(structural);
26:     for a2  :   and2 use entity work.and2(structural);
27:
28:
29: begin
30:
31:     a1  :   and2    port map(in1,   in2,    o1);
32:     a2  :   and2    port map(o1,    in3,    out1);
33:
34: end structural;
```