```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity Hit_Miss is
 6:     port(
 7:         tag1    :   in  std_logic_vector(2 downto 0);
 8:         tag2    :   in  std_logic_vector(2 downto 0);
 9:         Valid   :   in  std_logic;
10:         HitMiss :   out std_logic
11:     );
12: end Hit_Miss;
13:
14: architecture structural of Hit_Miss is
15:
16:     component Compare
17:     port(
18:         in1     :   in  std_logic_vector(2 downto 0);
19:         in2     :   in  std_logic_vector(2 downto 0);
20:         out1    :   out std_logic
21:     );
22:     end component;
23:
24:     component nand2
25:     port(
26:         in1     :   in  std_logic;
27:         in2     :   in  std_logic;
28:         out1    :   out std_logic
29:     );
30:     end component;
31:
32:     component invx1
33:     port(
34:         in1     :   in  std_logic;
35:         out1    :   out std_logic
36:     );
37:     end component;
38:
39:     signal comp_out :   std_logic;
40:     signal n_valid  :   std_logic;
41:
42:     for comp    :   Compare use entity work.Compare(structural);
43:     for v       :   nand2   use entity work.nand2(structural);
44:     for nv      :   invX1   use entity work.invX1(structural);
45:
46: begin
47:
48:     comp    :   Compare port map(tag1, tag2, comp_out);
49:     v       :   nand2    port map(comp_out, valid, n_valid);
50:     nv      :   invX1   port map(n_valid, HitMiss);
51:
52:
53: end structural;
```