```
    1: library STD;
    2: library IEEE;
    3: use IEEE.std_logic_1164.all;
    4:
    5: entity SR18 is
    6:     port(
    7:         clk     :   in  std_logic;
    8:         reset   :   in  std_logic;
    9:         Vdd     :   in  std_logic;
   10:         Gnd     :   in  std_logic;
   11:         output  :   out std_logic_vector(0 to 17)
   12:     );
   13: end SR18;
   14:
   15: architecture structural of SR18 is
   16:
   17:     component dff_reset_high
   18:     port(
   19:         d       :   in  std_logic;
   20:         clk     :   in  std_logic;
   21:         reset   :   in  std_logic;
   22:         Gnd     :   in  std_logic;
   23:         q       :   out std_logic
   24:     );
   25:     end component;
   26:
   27:     signal out1, out2, out3, out4, out5, out6, out7, out8, out9, out10, out11,
 out12, out13, out14, out15, out16, out17, out18   :   std_logic := '0';
   28:
   29:     for r0, r1, r2, r3, r4, r5, r6, r7, r8, r9, r10, r11, r12, r13, r14, r15,
r16, r17  :   dff_reset_high use entity work.dff_reset_high(structural);
   30:
   31: begin
   32:
   33:     r0  :   dff_reset_high  port map(Vdd,   clk,    reset,  Gnd,    out1);
   34:     r1  :   dff_reset_high  port map(out1,  clk,    reset,  Gnd,    out2);
   35:     r2  :   dff_reset_high  port map(out2,  clk,    reset,  Gnd,    out3);
   36:     r3  :   dff_reset_high  port map(out3,  clk,    reset,  Gnd,    out4);
   37:     r4  :   dff_reset_high  port map(out4,  clk,    reset,  Gnd,    out5);
   38:     r5  :   dff_reset_high  port map(out5,  clk,    reset,  Gnd,    out6);
   39:     r6  :   dff_reset_high  port map(out6,  clk,    reset,  Gnd,    out7);
   40:     r7  :   dff_reset_high  port map(out7,  clk,    reset,  Gnd,    out8);
   41:     r8  :   dff_reset_high  port map(out8,  clk,    reset,  Gnd,    out9);
   42:     r9  :   dff_reset_high  port map(out9,  clk,    reset,  Gnd,    out10);
   43:     r10 :   dff_reset_high  port map(out10, clk,    reset,  Gnd,    out11);
   44:     r11 :   dff_reset_high  port map(out11, clk,    reset,  Gnd,    out12);
   45:     r12 :   dff_reset_high  port map(out12, clk,    reset,  Gnd,    out13);
   46:     r13 :   dff_reset_high  port map(out13, clk,    reset,  Gnd,    out14);
   47:     r14 :   dff_reset_high  port map(out14, clk,    reset,  Gnd,    out15);
   48:     r15 :   dff_reset_high  port map(out15, clk,    reset,  Gnd,    out16);
   49:     r16 :   dff_reset_high  port map(out16, clk,    reset,  Gnd,    out17);
   50:     r17 :   dff_reset_high  port map(out17, clk,    reset,  Gnd,    out18);
   51:
   52:     output(0)  <= out1;
   53:     output(1)  <= out2;
   54:     output(2)  <= out3;
   55:     output(3)  <= out4;
   56:     output(4)  <= out5;
   57:     output(5)  <= out6;
   58:     output(6)  <= out7;
   59:     output(7)  <= out8;
   60:     output(8)  <= out9;
   61:     output(9)  <= out10;
   62:     output(10) <= out11;
   63:     output(11) <= out12;
   64:     output(12) <= out13;
   65:     output(13) <= out14;
   66:     output(14) <= out15;
   67:     output(15) <= out16;
   68:     output(16) <= out17;
   69:     output(17) <= out18;
   70:
   71: end structural;
```