```
 1: -- Entity: tx
 2: -- Architecture : structural
 3: -- Author: cpatel2
 4: --
 5:
 6: library STD;
 7: library IEEE;
 8: use IEEE.std_logic_1164.all;
 9:
10: entity tx is
11: port (
12:         sel   : in std_logic;
13:         selnot: in std_logic;
14:         input : in std_logic;
15:         output:out std_logic
16:     );
17: end tx;
18:
19: architecture structural of tx is
20:
21: begin
22:
23:     txprocess: process(sel, selnot, input)
24:     begin
25:         if (sel = '1' and selnot = '0') then
26:             output <= input;
27:         else
28:             output <= 'Z';
29:         end if;
30:     end process txprocess;
31:
32: end structural;
```