```
    1: library std;
    2: library ieee;
    3: use ieee.std_logic_1164.all;
    4:
    5: entity Output_Enable is
    6: port (
    7:     in8     :   in  std_logic_vector(7 downto 0);
    8:     enable  :   in  std_logic;
    9:     out8    :   out std_logic_vector(7 downto 0)
   10: );
   11: end Output_Enable;
   12:
   13: architecture structural of Output_Enable is
   14:
   15:     component tx
   16:     port(
   17:         sel     :   in  std_logic;
   18:         selnot  :   in  std_logic;
   19:         input   :   in  std_logic;
   20:         output  :   out std_logic
   21:     );
   22:     end component;
   23:
   24:     component invX1
   25:     port(
   26:         in1     :   in  std_logic;
   27:         out1    :   out std_logic
   28:     );
   29:     end component;
   30:
   31:     signal  n_enable    :   std_logic;
   32:
   33:     for n_en    :   invX1 use entity work.invX1(structural);
   34:     for tx0, tx1, tx2, tx3, tx4, tx5, tx6, tx7  : tx use entity work.tx(struct
ural);
   35:
   36: begin
   37:
   38:     n_en    :   invX1   port map(enable, n_enable);
   39:     tx0     :   tx      port map(enable, n_enable, in8(0), out8(0));
   40:     tx1     :   tx      port map(enable, n_enable, in8(1), out8(1));
   41:     tx2     :   tx      port map(enable, n_enable, in8(2), out8(2));
   42:     tx3     :   tx      port map(enable, n_enable, in8(3), out8(3));
   43:     tx4     :   tx      port map(enable, n_enable, in8(4), out8(4));
   44:     tx5     :   tx      port map(enable, n_enable, in8(5), out8(5));
   45:     tx6     :   tx      port map(enable, n_enable, in8(6), out8(6));
   46:     tx7     :   tx      port map(enable, n_enable, in8(7), out8(7));
   47:
   48: end structural;
```