```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity Dlatch_Reset is
 6:     port(
 7:         d       :   in  std_logic;
 8:         clk     :   in  std_logic;
 9:         reset   :   in  std_logic;
10:         Gnd     :   in  std_logic;
11:         q       :   out std_logic
12:     );
13: end Dlatch_Reset;
14:
15: architecture structural of Dlatch_Reset is
16:
17:     component Dlatch
18:     port(
19:         d       :   in  std_logic;
20:         clk     :   in  std_logic;
21:         q       :   out std_logic;
22:         qbar    :   out std_logic
23:     );
24:     end component;
25:
26:     component mux2_1
27:     port(
28:         in1     :   in  std_logic;
29:         in2     :   in  std_logic;
30:         sel     :   in  std_logic;
31:         out1    :   out std_logic
32:     );
33:     end component;
34:
35:     signal mux_out  :   std_logic;
36:
37:     for mux : mux2_1 use entity work.mux2_1(structural);
38:     for dl  : Dlatch use entity work.Dlatch(structural);
39:
40: begin
41:
42:     mux     :   mux2_1  port map(d,         Gnd,    reset,  mux_out);
43:     dl      :   Dlatch  port map(mux_out,   clk,    q, open);
44:
45: end structural;
```