```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity Decoder_Test is
 6:
 7: end Decoder_Test;
 8:
 9: architecture test of Decoder_Test is
10:
11:     component Decoder
12:     port(
13:         Mem_Add :   in  std_logic_vector(4 downto 0);
14:         Col_En  :   out std_logic_vector(3 downto 0);
15:         Row_En  :   out std_logic_vector(7 downto 0)
16:     );
17:     end component;
18:
19:     signal Mem_Add  :   std_logic_vector(4 downto 0);
20:     signal Col_En   :   std_logic_vector(3 downto 0);
21:     signal Row_En   :   std_logic_vector(7 downto 0);
22:
23:     for pm  :   Decoder use entity work.Decoder(structural);
24:
25: begin
26:
27:     pm  :   Decoder port map(Mem_Add, Col_En, Row_En);
28:
29:     p   :   process
30:     begin
31:         Mem_Add <= "00000";
32:         wait for 5 ns;
33:         Mem_Add <= "00001";
34:         wait for 5 ns;
35:         Mem_Add <= "10011";
36:         wait for 5 ns;
37:         wait;
38:     end process;
39: end test;
```