```
    1: library STD;
    2: library IEEE;
    3: use IEEE.std_logic_1164.all;
    4:
    5: entity Cache_Cell_Tag is
    6:     port(
    7:         Data    :   in  std_logic_vector(2 downto 0);
    8:         Tag_Wr  :   in  std_logic; --tag wr enable
    9:         reset   :   in  std_logic;
   10:         Gnd     :   in  std_logic;
   11:         Output  :   out std_logic_vector(2 downto 0);
   12:         Row_En  :   in  std_logic
   13:     );
   14: end Cache_Cell_Tag;
   15:
   16: architecture structural of Cache_Cell_Tag is
   17:
   18:     component Cache_Cell
   19:     port(
   20:         Data    :   in  std_logic;
   21:         W_En    :   in  std_logic;
   22:         reset   :   in  std_logic;
   23:         Gnd     :   in  std_logic;
   24:         Output  :   out std_logic;
   25:         Rd_En   :   in  std_logic;
   26:         nRd_En  :   in  std_logic
   27:     );
   28:     end component;
   29:
   30:     component and2
   31:     port(
   32:         in1     :   in  std_logic;
   33:         in2     :   in  std_logic;
   34:         out1    :   out std_logic
   35:     );
   36:     end component;
   37:
   38:     component or2
   39:     port(
   40:         in1     :   in  std_logic;
   41:         in2     :   in  std_logic;
   42:         out1    :   out std_logic
   43:     );
   44:     end component;
   45:
   46:     component invX1
   47:     port(
   48:         in1     :   in  std_logic;
   49:         out1    :   out std_logic
   50:     );
   51:     end component;
   52:
   53:     signal Wr_En    :   std_logic;
   54:     signal nRd_En   :   std_logic;
   55:
   56:     for nrd :   invX1 use entity work.invX1(structural);
   57:     for cell0, cell1, cell2 :   Cache_Cell use entity work.Cache_Cell(structur
al);
   58:
   59: begin
   60:
   61:     nrd     :   invX1       port map(Row_En, nRd_En);
   62:
   63:     cell0   :   Cache_Cell  port map(Data(0), Tag_Wr, reset, Gnd, Output(0), R
ow_En, nRd_En);
   64:     cell1   :   Cache_Cell  port map(Data(1), Tag_Wr, reset, Gnd, Output(1), R
ow_En, nRd_En);
   65:     cell2   :   Cache_Cell  port map(Data(2), Tag_Wr, reset, Gnd, Output(2), R
ow_En, nRd_En);
   66:
   67: end structural;
```