12/11/17 22:27:27 chip\_test.vhd

```
1: -- Entity: chip test
 2: -- Architecture : test
                                                                                      64:
                                                                                             write (out line, string'(" Memory data: "));
 3: -- Author: cpatel2
                                                                                      65:
                                                                                             write (out line, mem data);
 4: -- Created On: 11/01/05
                                                                                      66:
                                                                                             writeline(output, out_line);
5: --
                                                                                      67:
                                                                                             writeline(output, out_line);
6: library IEEE;
                                                                                      68:
                                                                                      69:
7: use IEEE.std_logic_1164.all;
                                                                                             write (out_line, string'(" Busy: "));
8: use IEEE.std_logic_textio.all;
                                                                                      70:
                                                                                             write (out_line, busy);
9: use IEEE.std logic arith.all;
                                                                                             write (out_line, string'(" Memory Enable: "));
                                                                                      71:
10: use STD.textio.all;
                                                                                      72:
                                                                                             write (out_line, mem_en);
                                                                                      73:
                                                                                             writeline(output, out_line);
12: entity chip_test is
                                                                                      74:
                                                                                             write (out_line, string'(" Memory Address: "));
13:
                                                                                      75:
14: end chip test;
                                                                                      76:
                                                                                             write (out line, mem add);
                                                                                      77:
                                                                                             writeline(output, out line);
16: architecture test of chip_test is
                                                                                      78:
17:
                                                                                      79:
                                                                                             write (out_line, string'(" -----")
18:
    component chip
                                                                                    );
19:
       port (
                                                                                      80:
                                                                                             writeline(output, out_line);
20:
         cpu_add
                    : in std_logic_vector(7 downto 0);
                                                                                      81:
21:
         cpu_data : inout std_logic_vector(7 downto 0);
                                                                                      82:
22:
         cpu_rd_wrn : in std_logic;
                                                                                      83: end print_output;
23:
         start : in std_logic;
                                                                                      84:
24:
         clk
                   : in std logic;
                                                                                      85:
                                                                                      86:
25:
         reset
                    : in std_logic;
26:
         mem_data : in std_logic_vector(7 downto 0);
                                                                                      87: begin
27:
         Vdd
                    : in std logic;
                                                                                      88:
28:
         Gnd
                    : in std_logic;
                                                                                      89:
                                                                                            Vdd <= '1';
29:
         busy
                    : out std_logic;
                                                                                      90:
                                                                                            Gnd <= '0';
30:
         mem en
                    : out std logic;
                                                                                      91: clk <= clock;
         mem_add : out std_logic_vector(7 downto 0));
31:
                                                                                      92:
32:
      end component;
                                                                                            c1 : chip port map (cpu_add, cpu_data, cpu_rd_wrn, start, clk, reset, mem_da
33:
                                                                                    ta, Vdd, Gnd, busy, mem en, mem add);
34:
                                                                                      94:
35:
                                                                                      95:
                                                                                            clking : process
36:
     for c1 : chip use entity work.chip(structural);
                                                                                      96:
                                                                                            begin
37:
                                                                                      97:
                                                                                              if done then
38:
     signal Vdd, Gnd: std logic;
                                                                                      98:
                                                                                                  wait;
39:
      signal cpu add, cpu data, mem data, mem add: std logic vector(7 downto 0);
                                                                                      99:
                                                                                              else
      signal cpu_rd_wrn, reset, clk, start, clock, busy, mem_en: std_logic;
                                                                                     100:
                                                                                                  clock<= '1', '0' after 5 ns;
                                                                                     101:
                                                                                                  wait for 10 ns;
42:
      signal clk count: integer:=0;
                                                                                     102:
                                                                                              end if;
43:
       shared variable done : boolean :=false;
                                                                                     103:
                                                                                            end process clking;
44: procedure print output is
                                                                                     104:
      variable out line: line;
                                                                                     105: io_process: process
45:
46:
                                                                                     106:
47:
                                                                                     107:
                                                                                              file infile : text is "./chip_in.txt";
      begin
48:
                                                                                     108:
                                                                                              variable out_line: line;
      write (out_line, string' (" Clock: "));
49:
      write (out_line, clk_count);
                                                                                     109:
                                                                                              variable buf: line;
50:
      write (out_line, string'(" Start: "));
                                                                                     110:
                                                                                              variable value: std logic vector(7 downto 0);
51:
      write (out line, start);
                                                                                     111:
                                                                                              variable value1: std logic;
      write (out_line, string'(" Cpu Read/Write: "));
                                                                                     112:
53:
      write (out_line, cpu_rd_wrn);
                                                                                     113:
                                                                                            begin
      write (out line, string'(" Reset: "));
                                                                                     114:
54:
55:
      write (out_line, reset);
                                                                                     115:
                                                                                              while not (endfile(infile)) loop
                                                                                     116:
56:
      writeline(output, out_line);
                                                                                     117:
57:
                                                                                                wait until rising_edge(clock);
                                                                                     118:
58:
      write (out_line, string' (" CPU address: "));
                                                                                                print_output;
                                                                                     119:
59:
      write (out_line, cpu_add);
60:
      write (out_line, string'(" CPU data: "));
                                                                                     120:
                                                                                                readline(infile, buf);
      write (out_line, cpu_data);
                                                                                     121:
                                                                                                read(buf, value);
61:
      writeline(output, out_line);
                                                                                     122:
                                                                                                cpu_add <= value;
```

2

## chip\_test.vhd

```
124:
           readline(infile, buf);
125:
           read(buf, value);
126:
           cpu_data <= value;
127:
128:
           readline(infile, buf);
129:
           read(buf, value1);
130:
           cpu_rd_wrn <= value1;</pre>
131:
132:
           readline(infile, buf);
133:
           read(buf, value1);
134:
           start <= value1;
135:
           readline(infile, buf);
136:
137:
           read(buf, value1);
138:
           reset <= value1;
139:
           wait until falling_edge(clock);
140:
141:
142:
           readline(infile, buf);
143:
           read(buf, value);
144:
           mem_data <= value;</pre>
145:
146:
           clk_count <= clk_count+1;</pre>
147:
148:
           print_output;
149:
150:
         end loop;
151:
         done := true;
152:
         wait;
153:
154:
       end process io_process;
155:
156:
157: end test;
```

12/11/17 22:27:27