

```
1: library STD;
2: library IEEE;
3: use IEEE.std_logic_1164.all;
4:
5: entity or4 is
6: port(
7:     in1      : in  std_logic;
8:     in2      : in  std_logic;
9:     in3      : in  std_logic;
10:    in4      : in  std_logic;
11:    out1     : out std_logic
12: );
13: end or4;
14:
15: architecture structural of or4 is
16:
17:     component or2
18:     port(
19:         in1      : in  std_logic;
20:         in2      : in  std_logic;
21:         out1     : out std_logic
22:     );
23:     end component;
24:
25:     signal o1   : std_logic;
26:     signal o2   : std_logic;
27:
28:     for og1, og2, og3 : or2 use entity work.or2(structural);
29:
30: begin
31:
32:     og1 : or2 port map(in1, in2, o1);
33:     og2 : or2 port map(in3, in4, o2);
34:     og3 : or2 port map(o1, o2, out1);
35:
36: end structural;
```