```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity dff_reset_high is
 6:     port(
 7:         d       :   in  std_logic;
 8:         clk     :   in  std_logic;
 9:         reset   :   in  std_logic;
10:         Gnd     :   in  std_logic;
11:         q       :   out std_logic
12:     );
13: end dff_reset_high;
14:
15: architecture structural of dff_reset_high is
16:
17:     component dff
18:     port(
19:         d       :   in  std_logic;
20:         clk     :   in  std_logic;
21:         q       :   out std_logic
22:     );
23:     end component;
24:
25:     component mux2_1
26:     port(
27:         in1     :   in  std_logic;
28:         in2     :   in  std_logic;
29:         sel     :   in  std_logic;
30:         out1    :   out std_logic
31:     );
32:     end component;
33:
34:     component invX1
35:     port(
36:         in1     :   in  std_logic;
37:         out1    :   out std_logic
38:     );
39:     end component;
40:
41:     signal mux_out  :   std_logic;
42:     signal n_clk    :   std_logic;
43:
44:     for asdf    :   invX1 use entity work.invX1(structural);
45:     for mux     :   mux2_1 use entity work.mux2_1(structural);
46:     for dl      :   dff use entity work.dff(structural);
47:
48: begin
49:
50:     asdf    :   invX1   port map(clk, n_clk);
51:     mux     :   mux2_1  port map(d, Gnd, reset,  mux_out);
52:     dl      :   dff     port map(mux_out, n_clk, q);
53:
54: end structural;
```