```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity mux2_1 is
 6: port(
 7:     in1     :   in  std_logic;
 8:     in2     :   in  std_logic;
 9:     sel     :   in  std_logic;
10:     out1    :   out std_logic
11: );
12: end mux2_1;
13:
14: architecture structural of mux2_1 is
15:
16:     component nand2
17:     port(
18:         in1     :   in  std_logic;
19:         in2     :   in  std_logic;
20:         out1    :   out std_logic
21:     );
22:     end component;
23:
24:     component invX1
25:     port(
26:         in1     :   in  std_logic;
27:         out1    :   out std_logic
28:     );
29:     end component;
30:
31:     signal n_sel        :   std_logic;
32:     signal and1_out     :   std_logic;
33:     signal and2_out     :   std_logic;
34:
35:     for inv :   invX1 use entity work.invX1(structural);
36:     for and_1, and_2, o :  nand2 use entity work.nand2(structural);
37:
38: begin
39:
40:     inv     :   invX1   port map(sel,       n_sel);
41:     and_1   :   nand2   port map(in1,       n_sel,        and1_out);
42:     and_2   :   nand2   port map(in2,       sel,      and2_out);
43:     o       :   nand2   port map(and1_out,  and2_out,  out1);
44:
45: end structural;
```