```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity invX1 is
 6: port(
 7:     in1     :   in  std_logic;
 8:     out1    :   out std_logic
 9: );
10: end invX1;
11:
12: architecture structural of invX1 is
13: begin
14:     out1 <= not in1;
15: end structural;
```