```
    1: library STD;
    2: library IEEE;
    3: use IEEE.std_logic_1164.all;
    4: use IEEE.std_logic_textio.all;
    5: use STD.textio.all;
    6:
    7: entity Cache_Cell_Test is
    8:
    9: end Cache_Cell_Test;
   10:
   11: architecture test of Cache_Cell_Test is
   12:
   13:     component Cache_Cell
   14:     port(
   15:         Data    :   in  std_logic;
   16:         W_En    :   in  std_logic;
   17:         reset   :   in  std_logic;
   18:         Gnd     :   in  std_logic;
   19:         Output  :   out std_logic;
   20:         Rd_En   :   in  std_logic;
   21:         nRd_En  :   in  std_logic
   22:     );
   23:     end component;
   24:
   25:     component invX1
   26:     port(
   27:         in1     :   in  std_logic;
   28:         out1    :   out std_logic
   29:     );
   30:     end component;
   31:
   32:     signal s_Data   :   std_logic;
   33:     signal s_W_En   :   std_logic;
   34:     signal s_reset  :   std_logic;
   35:     signal s_Output :   std_logic;
   36:     signal s_Rd_En  :   std_logic;
   37:     signal s_nRd_En :   std_logic;
   38:
   39:     for inv :   invX1 use entity work.invX1(structural);
   40:     for cache   :   Cache_Cell use entity work.Cache_Cell(structural);
   41:
   42: begin
   43:
   44:     inv     :   invX1       port map(s_Rd_En, s_nRd_En);
   45:
   46:     cache   :   Cache_Cell  port map(s_Data, s_W_En, s_reset, '0', s_Output, s
_Rd_En, s_nRd_En);
   47:
   48:     t   :   process
   49:
   50:     begin
   51:
   52:         s_reset <=  '1', '0' after 10 ns;
   53:         s_Data  <= '0';
   54:         s_W_En  <= '0';
   55:         s_Rd_En <=  '1' after 2 ns;
   56:         wait for 20 ns;
   57:         s_Data  <=  '1' after 1 ns;
   58:         s_W_En  <=  '1';
   59:         wait for 5 ns;
   60:         s_Rd_en <=  '0' after 4 ns;
   61:         s_W_En  <=  '0';
   62:         s_Data  <=  '0' after 1 ns;
   63:         wait for 5 ns;
   64:         s_reset <= '1', '0' after 5 ns;
   65:         wait for 10 ns;
   66:         wait;
   67:
   68:     end process;
   69:
   70: end test;
```