```
 1: --
 2: -- Entity: dff
 3: -- Architecture : structural
 4: -- Author: cpatel2
 5: --
 6: --
 7: library STD;
 8: library IEEE;
 9: use IEEE.std_logic_1164.all;
10:
11: entity dff is
12: port (
13:     d   : in  std_logic;
14:     clk : in  std_logic;
15:     q   : out std_logic
16:     );
17: end dff;
18:
19: architecture structural of dff is
20:
21: begin
22:     output: process
23:     begin
24:         wait until ( clk'EVENT and clk = '0' );
25:         q <= d;
26:     end process output;
27: end structural;
```