```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity tx_test is
 6:
 7: end tx_test;
 8:
 9: architecture test of tx_test is
10:
11:     component tx
12:     port(
13:         sel     :   in  std_logic;
14:         selnot  :   in  std_logic;
15:         input   :   in  std_logic;
16:         output  :   out std_logic
17:     );
18:     end component;
19:
20:     signal input, sel, selnot, output   :   std_logic;
21:
22:     for asdf    :   tx use entity work.tx(structural);
23:
24: begin
25:
26:     asdf    :   tx  port map(sel, selnot, input, output);
27:
28:     p   :   process
29:     begin
30:         sel <= 'U';
31:         selnot <= 'U';
32:         input <= 'U';
33:         wait for 10 ns;
34:         sel <= '0';
35:         selnot <= '1';
36:         wait for 10 ns;
37:         wait;
38:     end process;
39:
40: end test;
```