```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity dff_reset is
 6:     port(
 7:         d       :   in  std_logic;
 8:         clk     :   in  std_logic;
 9:         reset   :   in  std_logic;
10:         Gnd     :   in  std_logic;
11:         q       :   out std_logic
12:     );
13: end dff_reset;
14:
15: architecture structural of dff_reset is
16:
17:     component dff
18:     port(
19:         d       :   in  std_logic;
20:         clk     :   in  std_logic;
21:         q       :   out std_logic
22:     );
23:     end component;
24:
25:     component mux2_1
26:     port(
27:         in1     :   in  std_logic;
28:         in2     :   in  std_logic;
29:         sel     :   in  std_logic;
30:         out1    :   out std_logic
31:     );
32:     end component;
33:
34:     signal mux_out  :   std_logic;
35:
36:     for mux :   mux2_1 use entity work.mux2_1(structural);
37:     for dl  :   dff use entity work.dff(structural);
38:
39: begin
40:
41:     mux     :   mux2_1  port map(d,         Gnd,    reset,  mux_out);
42:     dl      :   dff     port map(mux_out,   clk,    q);
43:
44: end structural;
```