```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity or5 is
 6: port(
 7:     in1     :   in  std_logic;
 8:     in2     :   in  std_logic;
 9:     in3     :   in  std_logic;
10:     in4     :   in  std_logic;
11:     in5     :   in  std_logic;
12:     out1    :   out std_logic
13: );
14: end or5;
15:
16: architecture structural of or5 is
17:
18:     component or2
19:     port(
20:         in1     :   in  std_logic;
21:         in2     :   in  std_logic;
22:         out1    :   out std_logic
23:     );
24:     end component;
25:
26:     component or4
27:     port(
28:         in1     :   in  std_logic;
29:         in2     :   in  std_logic;
30:         in3     :   in  std_logic;
31:         in4     :   in  std_logic;
32:         out1    :   out std_logic
33:     );
34:     end component;
35:
36:     signal o1   :   std_logic;
37:
38:     for og1 : or4 use entity work.or4(structural);
39:     for og2 : or2 use entity work.or2(structural);
40:
41: begin
42:
43:     og1 :   or4 port map(in1, in2, in3, in4, o1);
44:     og2 :   or2 port map(o1,  in5, out1);
45:
46: end structural;
```