```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity or3 is
 6: port(
 7:     in1     :   in  std_logic;
 8:     in2     :   in  std_logic;
 9:     in3     :   in  std_logic;
10:     out1    :   out std_logic
11: );
12: end or3;
13:
14: architecture structural of or3 is
15:
16:     component or2
17:     port(
18:         in1     :   in  std_logic;
19:         in2     :   in  std_logic;
20:         out1    :   out std_logic
21:     );
22:     end component;
23:
24:     signal o1   :   std_logic;
25:
26:     for og1, og2 : or2 use entity work.or2(structural);
27:
28: begin
29:
30:     og1 :   or2 port map(in1, in2, o1);
31:     og2 :   or2 port map(in3, o1, out1);
32:
33:
34: end structural;
```