```
  1: library STD;
  2: library IEEE;
  3: use IEEE.std_logic_1164.all;
  4:
  5: entity Cache_Cell is
  6:     port(
  7:         Data    :   in  std_logic;
  8:         W_En    :   in  std_logic;
  9:         reset   :   in  std_logic;
 10:         Gnd     :   in  std_logic;
 11:         Output  :   out std_logic;
 12:         Rd_En   :   in  std_logic;
 13:         nRd_En  :   in  std_logic
 14:     );
 15: end Cache_Cell;
 16:
 17: architecture structural of Cache_Cell is
 18:
 19:     component Dlatch_Reset
 20:     port(
 21:         d       :   in  std_logic;
 22:         clk     :   in  std_logic;
 23:         reset   :   in  std_logic;
 24:         Gnd     :   in  std_logic;
 25:         q       :   out std_logic
 26:     );
 27:     end component;
 28:
 29:     component invX1
 30:     port(
 31:         in1     :   in  std_logic;
 32:         out1    :   out std_logic
 33:     );
 34:     end component;
 35:
 36:     component tx
 37:     port(
 38:         sel     :   in  std_logic;
 39:         selnot  :   in  std_logic;
 40:         input   :   in  std_logic;
 41:         output  :   out std_logic
 42:     );
 43:     end component;
 44:
 45:     component or2
 46:     port(
 47:         in1     :   in  std_logic;
 48:         in2     :   in  std_logic;
 49:         out1    :   out std_logic
 50:     );
 51:     end component;
 52:
 53:     signal Dout :   std_logic;
 54:     signal b1   :   std_logic; --buffer intermediate signal
 55:     signal bout :   std_logic; --buffer output
 56:     signal eout :   std_logic; --enable signal going into Dlatch
 57:
 58:     for r_or    :   or2 use entity work.or2(structural);
 59:     for dl      :   Dlatch_Reset use entity work.Dlatch_Reset(structural);
 60:     for trans   :   tx  use entity work.tx(structural);
 61:
 62: begin
 63:
 64:     r_or    :   or2             port map(reset, W_En, eout);
 65:     dl      :   Dlatch_Reset    port map(Data, eout, reset, Gnd, Dout);
 66:     trans   :   tx              port map(Rd_En, nRd_En, Dout, Output);
 67:
 68: end structural;
```