```
 1: --
 2: -- Entity: srff
 3: -- Architecture : structural
 4: -- Author: cpatel2
 5: --
 6: --
 7: library STD;
 8: library IEEE;
 9: use IEEE.std_logic_1164.all;
10:
11: entity srff is
12: port (
13:     s   :   in  std_logic := '0';
14:     r   :   in  std_logic := '0';
15:     clk :   in  std_logic;
16:     q   :   out std_logic;
17:     qbar:   out std_logic
18:     );
19: end srff;
20:
21: architecture structural of srff is
22:
23: begin
24:     output: process
25:     begin
26:         wait until ( clk'EVENT and clk = '0' );
27:         if s = '1' and r /= '1' then
28:             q <= '1';
29:             qbar <= '0';
30:         elsif r = '1' and s /= '1' then
31:             q <= '0';
32:             qbar <= '1';
33:         elsif r = '1' and s = '1' then
34:             q <= 'U';
35:             qbar <= 'U';
36:         end if;
37:     end process output;
38: end structural;
```