```
    1: library IEEE;
    2: library STD;
    3: use IEEE.std_logic_1164.all;
    4:
    5: entity Cache_Row_Test is
    6:
    7: end Cache_Row_Test;
    8:
    9: architecture test of Cache_Row_Test is
   10:
   11:     component Cache_Cell_Row
   12:     port(
   13:         Data_In     :   in  std_logic_vector(7 downto 0);
   14:         Tag_In      :   in  std_logic_vector(2 downto 0);
   15:         Col0_Rd_En  :   in  std_logic;
   16:         Col1_Rd_En  :   in  std_logic;
   17:         Col2_Rd_En  :   in  std_logic;
   18:         Col3_Rd_En  :   in  std_logic;
   19:         Col0_Wr_En  :   in  std_logic;
   20:         Col1_Wr_En  :   in  std_logic;
   21:         Col2_Wr_En  :   in  std_logic;
   22:         Col3_Wr_En  :   in  std_logic;
   23:         Tag_Wr_En   :   in  std_logic;
   24:         Row_Rd_En   :   in  std_logic;
   25:         Row_Wr_En   :   in  std_logic;
   26:         Gnd         :   in  std_logic;
   27:         reset       :   in  std_logic;
   28:         Data_Out    :   out std_logic_vector(7 downto 0);
   29:         Tag_Out     :   out std_logic_vector(2 downto 0);
   30:         Valid_Out   :   out std_logic
   31:     );
   32:     end component;
   33:
   34:     signal  s_Data_In     :    std_logic_vector(7 downto 0);
   35:     signal  s_Tag_In      :    std_logic_vector(2 downto 0);
   36:     signal  s_Col0_Rd_En  :    std_logic;
   37:     signal  s_Col1_Rd_En  :    std_logic;
   38:     signal  s_Col2_Rd_En  :    std_logic;
   39:     signal  s_Col3_Rd_En  :    std_logic;
   40:     signal  s_Col0_Wr_En  :    std_logic;
   41:     signal  s_Col1_Wr_En  :    std_logic;
   42:     signal  s_Col2_Wr_En  :    std_logic;
   43:     signal  s_Col3_Wr_En  :    std_logic;
   44:     signal  s_Tag_Wr_En   :    std_logic;
   45:     signal  s_Row_Rd_En   :    std_logic;
   46:     signal  s_Row_Wr_En   :    std_logic;
   47:     signal  s_Gnd         :    std_logic;
   48:     signal  s_reset       :    std_logic;
   49:     signal  s_Data_Out    :    std_logic_vector(7 downto 0);
   50:     signal  s_Tag_Out     :    std_logic_vector(2 downto 0);
   51:     signal  s_Valid_Out   :    std_logic;
   52:
   53:     for row :   Cache_Cell_Row use entity work.Cache_Cell_Row(structural);
   54:
   55: begin
   56:
   57:     row :   Cache_Cell_Row  port map(s_Data_In, s_Tag_In, s_Col0_Rd_En, s_Col1
_Rd_En, s_Col2_Rd_En, s_Col3_Rd_En, s_Col0_Wr_En, s_Col1_Wr_En, s_Col2_Wr_En, s_Col3_W
r_En, s_Tag_Wr_En, s_Row_Rd_En, s_Row_Wr_En, '0', s_reset, s_Data_Out, s_Tag_Out, s_Va
lid_Out);
   58:
   59:     p   :   process
   60:     begin
   61:         s_reset <=  '0';
   62:         s_row_Wr_En <= '0';
   63:         wait for 5 ns;
   64:
   65:         s_reset <=  '1', '0' after 10 ns;
   66:         wait for 15 ns;
   67:         s_Data_In   <=  "00000001";
   68:         s_Col0_Wr_En  <=  '1';
   69:         s_Row_Wr_En   <=  '1';
   70:         s_Tag_In    <=  "010";
   71:         wait for 10 ns;
   72:         s_Tag_Wr_En <=  '1';
   73:         s_Data_In   <=  "00000010";
   74:         s_Col0_Wr_En  <=  '0';
   75:         s_Col1_Wr_En  <=  '1';
   76:         wait for 10 ns;
   77:         s_Tag_Wr_En <=  '0';
   78:         s_Data_In   <=  "00010000";
   79:         s_Col1_Wr_En  <=  '0';
   80:         s_Col2_Wr_En  <=  '1';
   81:         wait for 10 ns;
   82:         s_Data_In   <=  "01110000";
   83:         s_Col2_Wr_En  <=  '0';
   84:         s_Col3_Wr_En  <=  '1';
   85:         wait for 10 ns;
   86:         s_Col3_Wr_En  <=  '0';
   87:         s_Row_Wr_En   <=  '0';
   88:         s_Data_In   <=  "00000000";
   89:         wait for 10 ns;
   90:         s_Row_Rd_En   <=  '1';
   91:         s_Col0_Rd_En  <=  '1';
   92:         wait for 10 ns;
   93:         s_Row_Rd_En   <=  '0';
   94:         s_Row_Rd_En   <=  '0';
   95:         wait;
   96:     end process;
   97: end test;
```