```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity and2 is
 6: port(
 7:     in1     :   in  std_logic;
 8:     in2     :   in  std_logic;
 9:     out1    :   out std_logic
10: );
11: end and2;
12:
13: architecture structural of and2 is
14: begin
15:     out1 <= in1 and in2;
16: end structural;
```