```
    1: library STD;
    2: library IEEE;
    3: use IEEE.std_logic_1164.all;
    4:
    5: entity register8 is
    6:     port(
    7:         d       :   in  std_logic_vector(7 downto 0);
    8:         clk     :   in  std_logic;
    9:         reset   :   in  std_logic;
   10:         Gnd     :   in  std_logic;
   11:         q       :   out std_logic_vector(7 downto 0)
   12:     );
   13: end register8;
   14:
   15: architecture structural of register8 is
   16:
   17:     component dff_reset
   18:     port(
   19:         d       :   in  std_logic;
   20:         clk     :   in  std_logic;
   21:         reset   :   in  std_logic;
   22:         Gnd     :   in  std_logic;
   23:         q       :   out std_logic
   24:     );
   25:     end component;
   26:
   27:     for register0, register1, register2, register3, register4, register5, regi
ster6, register7  :   dff_reset use entity work.dff_reset(structural);
   28:
   29: begin
   30:
   31:     register0   :   dff_reset port map(d(0), clk, reset, Gnd, q(0));
   32:     register1   :   dff_reset port map(d(1), clk, reset, Gnd, q(1));
   33:     register2   :   dff_reset port map(d(2), clk, reset, Gnd, q(2));
   34:     register3   :   dff_reset port map(d(3), clk, reset, Gnd, q(3));
   35:     register4   :   dff_reset port map(d(4), clk, reset, Gnd, q(4));
   36:     register5   :   dff_reset port map(d(5), clk, reset, Gnd, q(5));
   37:     register6   :   dff_reset port map(d(6), clk, reset, Gnd, q(6));
   38:     register7   :   dff_reset port map(d(7), clk, reset, Gnd, q(7));
   39:
   40: end structural;
```