```
 1: library IEEE;
 2: use IEEE.STD_LOGIC_1164.ALL;
 3:
 4: entity SRlatch is
 5:     Port ( s : in    STD_LOGIC;
 6:            r : in    STD_LOGIC;
 7:            q : out STD_LOGIC); -- changed out to inout
 8: end SRlatch;
 9:
10: architecture structural of SRlatch is
11: begin
12:     p   :   process(s, r)
13:     begin
14:         if r = '1' and s /= '1' then
15:             q <= '0';
16:         elsif s = '1' and r /= '1' then
17:             q <= '1';
18:         elsif s = '1' and r = '1' then
19:             q <= 'U';
20:         end if;
21:     end process;
22:
23: end structural;
```