```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity Hit_Miss_Test is
 6:
 7: end Hit_Miss_Test;
 8:
 9: architecture test of Hit_Miss_Test is
10:
11:     component Hit_Miss
12:      port(
13:         tag1    :   in  std_logic_vector(2 downto 0);
14:         tag2    :   in  std_logic_vector(2 downto 0);
15:         Valid   :   in  std_logic;
16:         HitMiss :   out std_logic
17:     );
18:     end component;
19:
20:     signal tag1, tag2   :   std_logic_vector(2 downto 0);
21:     signal Valid, HitMiss   :   std_logic;
22:
23:     for pm  :   Hit_Miss use entity work.Hit_Miss(structural);
24:
25: begin
26:
27:     pm  :   Hit_Miss port map(tag1, tag2, Valid, HitMiss);
28:
29:     p   :   process
30:     begin
31:         tag1 <= "000";
32:         tag2 <= "000";
33:         Valid <= '1';
34:         wait for 5 ns;
35:         tag2 <= "001";
36:         wait for 5 ns;
37:         tag1 <= "001";
38:         Valid <= '0';
39:         wait for 5 ns;
40:         Valid <= '1';
41:         wait for 5 ns;
42:         wait;
43:     end process;
44:
45: end test;
```