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STUDIES ON SMALL SIGNAL CE AMPLIFIER:

OBJECTIVE:

To study small signal CE Amplifiers.

APPARATUS REQUIRED:

- Printed circuit board.
- DC Power supply 12V.
- AC signal generator
- connecting wires
- Cathode Ray oscilloscope.
- Multimeter.

MEASUREMENT OF DC CONDITIONS:

The following experimental values of resistors are measured using multimeter:

$R_X \rightarrow 1.05K\Omega$

$R_2 \rightarrow 4.67K\Omega$

$R_1 \rightarrow 47.1K\Omega$

$R_{E2} \rightarrow 357\Omega$

$R_{E1} \rightarrow 359\Omega$

$R_C \rightarrow 6.85K\Omega$

$R_L \rightarrow 1.024k\Omega$

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+12V V_{cc} is applied to amplifier circuit from dc power supply and the values of V_B, V_C and V_E are measured:

V_B : 1.019V
V_C : 7.57V
V_E : 0.441V

} with respect to ground.

Thus $V_{BE} = V_B - V_E = 0.578V$

$V_{CE} = V_C - V_E = 7.129V$.

$$I_C = \frac{V_{IN} - V_C}{R_C} = \frac{12 - 7.57}{6.8 \times 10^3} = 0.65\,mA.$$

writing Kirchoff's loop law;

$$V_B - V_{BE} - I_E(R_{E1} + R_{E2}) = 0.$$

$$\Rightarrow I_E = \left(\frac{V_B - V_{BE}}{R_{E1} + R_{E2}}\right) = 0.668\,mA.$$

Readings of this experiment lead us to following conclusions:

-> ~~Region~~ collector junction is reverse biased and emitter is ~~forw~~ forward biased.

-> $I_B > 0$ and $V_{CE} > 0.5V$ and thus, it is in active region. and Q-point is suitably located.

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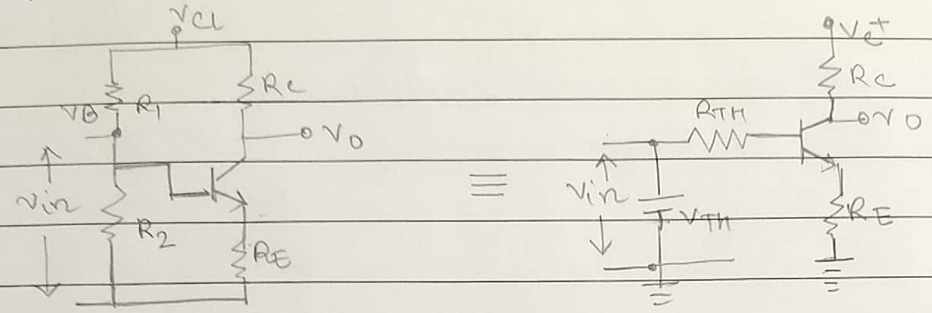
THEORY:

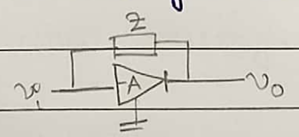
We also emphasize the use of transistor biasing in this experiment with resistance divider or v-divider bias.



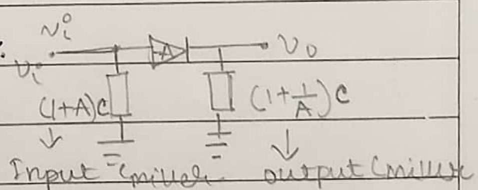
This circuit stabilises the Q-point of DC equivalent circuit by stabilising β for ~~*~~ significant changes in v_{in}.

The capacitors act as open circuit for DC equivalent circuit and hence has no effect on I_{DQ}. However for AC circuit and significant values of ω (it acts as High Pass filter), it can be treated as short ~~the~~ circuit ($X_C << R_E, R_C, R_B$) and hence accounts for stability of AC circuit.

Next we have seen miller effect. Miller equation can be used to provide equivalent circuit formed due to application of C_{cb}:



In our experiment, Z is $X_{C_{cb}}$. Using miller equation, we shall have:



Lastly we have found out R_i and R_o for the transistor circuits;

$$r_i = \frac{\beta V_T}{I_{CQ}}$$

$$r_o = \frac{V_A}{I_{CQ}} \quad (A \rightarrow \text{Early voltage})$$

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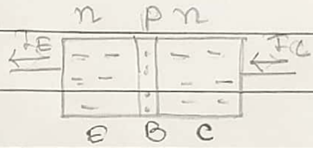
THEORY :

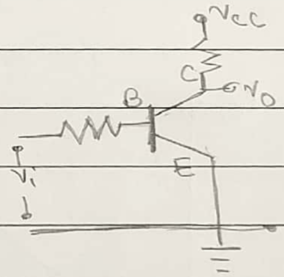
In this experiment, we are working with BJT ~~with~~ in amplifier configuration.

BJT stands for Bipolar Junction transistor. There can be ~~two~~ three types of BJTs – common Base (CB), Common Emitter (CE) and common collector.



In common emitter, v_i is applied across Base and emitter. Thus,

$$I_B = \frac{V_i - V_{BE(on)}}{R_B}$$



also, it is constant for a given V_{BE}.
The current in I_B is due to movement of electrons. They cross the B-E depletion layer and reach the Base. The electrons then move across the p-n junction in BC by diffusion while some of them recombine giving rise to I_B.

The relations are;

$I_C = \alpha I_E$. (α is common base gain ≈ 1).

$I_C = \beta I_B$. (β is common emitter gain >> 1)

The circuit has two equivalent circuits – DC equivalent and AC equivalent. Addition of R_E decreases I_B and thus gain, however it stabilises the circuit to prevent thermal runoff.

Capacitors are used in various experiments in this circuit to prevent dc offset voltages in the source currents, without changing the Q-points.

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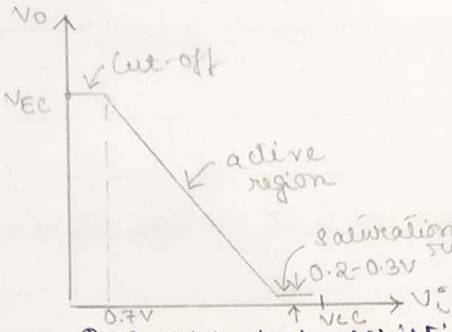
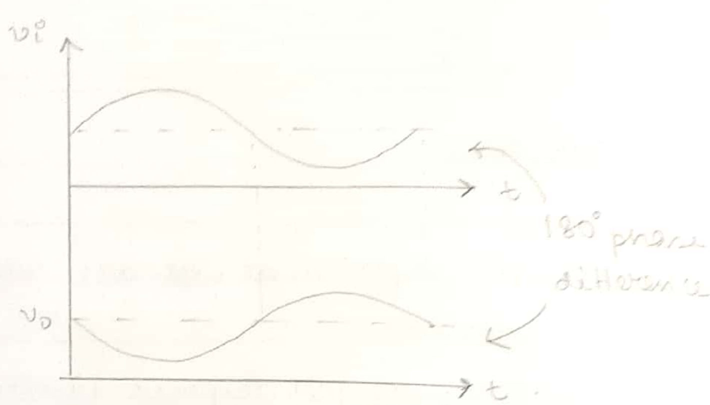
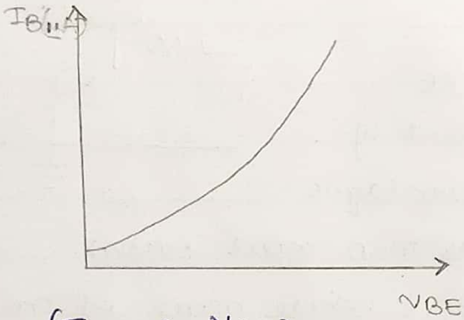


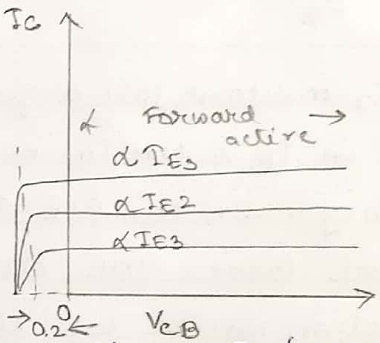
Transfer characteristics.
(Vo vs Vi)



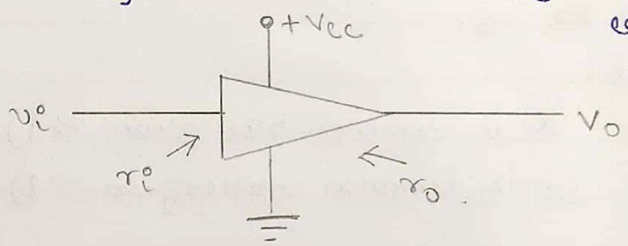
Transfer characteristics
(Vo and Vi vs T).



(IB vs VBE)



VCB vs Ic (neglecting early voltage).



(input and output resistance)

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MEASUREMENT OF SIGNAL HANDLING CAPACITY:

R_x is shorted by connecting 1-1' and capacitor is connected across R_{E2} by joining 2-2'.

case 1:

$R = \infty$ (no load).   Frequency: 3.962 KHZ.

Sl. No.	V_{in} (mV)	V_{out} (V)	Gain (V_o/V_i)
1.	100	1.8	18
2.	120	2.2	18.33
3.	140	2.6	18.57
4.	250	3.8	17.75
5.	350	6.3	18.00
6.	500	8.6	17.2
7.	590	9.6	16.27
8.	670	10.4	~~0.0~~ 15.5
9.	1000	10.4	10.4.

V_{sm} is the point where clipping starts. The V_{sm} is thus concluded to be at 580mV of V_{in}. The output voltage is undistorted till this point.

Thus, $V_{sm} = 580$mV.

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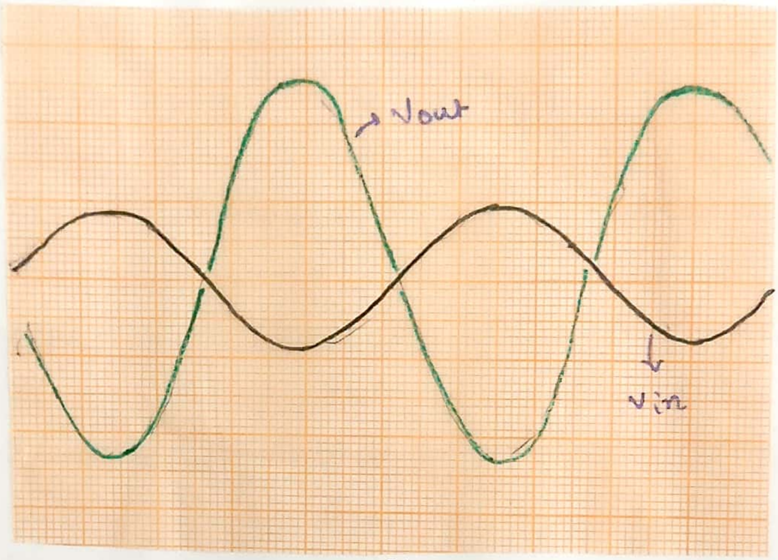
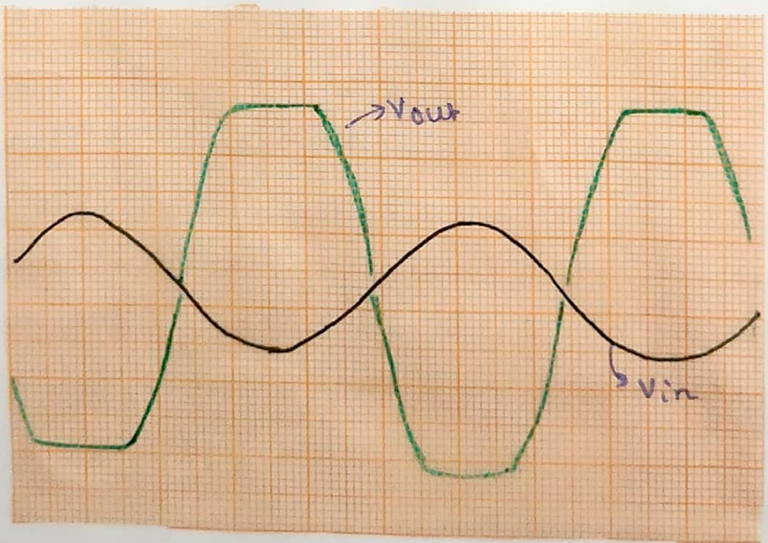


V_i below V_{SM}



V_i Above V_{SM} (Saturated)

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(ii) R_L connected case:

$R_L = 1K\Omega$ $f \rightarrow 4KHz$.

Sl. No.	Vin (mV)	Vout (V)	Gain (V_o/V_i)
1	100	.24	2.4
2	160	.38	2.375
3	250	.60	2.4
4	350	.84	2.4
5	500	1.14	2.28
6	540	1.2	2.22
7	880	1.5	1.87
8	1000	1.7	1.7.

Similar to previous case, we note the value of V_{sm} : 540mV. We also notice that V_{sm} is approximately same for both the cases.

Gain decreased due to connection of R_L.

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FREQUENCY RESPONSE :

V_{in} : 0.5V (maintained constant). R_L = 1KΩ

Sl.NO.	Frequency(Hz)	Vout (V)	20log(Vo/Vi)
1	~~117.2~~ 10.38	.804	4.12
2	20.03	1.04	6.36
3	35.31	1.10	6.85
4	49.3	1.12	7.00
5	100 ~~117.2~~	1.12	7.00
6	117.2 ~~400~~	1.12	7.00
7	150K	1.10	6.85
8	201.K	1.08	6.69
9	268.7K	1.06	6.53
10	379.4 K	1.04	6.36
11	383.3K	1.00	6.02
12	526 K	0.96	5.66
13	590 K	0.92	5.29
14	651 K	0.88	4.91
15	736 K	0.84	4.50
16	804 K	0.80	4.08
17	911 K	0.76	3.64
18	980 K	0.72	3.17
19	1084 K	0.68	2.67

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(iii) vin = 0.5 V. $R_L = \infty$ (no load)

Sl. No.	Frequency (Hz)	Vout (V)	20 log (Vo/Vi) db
1	10.33	6.8	~~2.67~~ 22.67
2	20	8	~~4.08~~ 24.08
3	35	8.4	24.5
4	42.6	8.6	24.7
5	319	8.6	24.7
6	26.27K	8.4	~~24.08~~ 24.5
7	54.5K	8.0	24.08
8	82.5K	7.6	23.63
9	104.2K	7.2	23.17
10	128.8K	6.8	22.6
11	148K	6.4	22.14
12	173.5K	6	21.58
13	221.3K	5.2	20.34
14	279.4K	4.4	18.89
15	324.4K	4	18.06
16	386K	3.4	16.65
17	440K	3	15.56
18	567K	2.4	13.62
19	681K	2	12.04
20	846K	1.6	10.1
21	1000K	1.3	8.29

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(iii) Effect of C_E :

a) $R_L = 1 K\Omega$. $v_{in} = 0.5V$.

SL. No.	Frequencies	v_{out} (V)	$20 \log(v_o/v_i)$ db
1	·5	0.42	~~2.114~~, -1.514
2	10	0.48	-0.354
3	20	0.55	0.828
4	100	0.58	1.289
5	20K	0.57	1.138
6	300K	0.56	0.984
7	500K	0.55	0.828
8	800K	0.52	0.341
9	1M	0.50	0
10	2M	0.37	-2.615
11	3M	0.28	-5.036

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b) R_{E1} and R_{E2} fully bypassed:

Sl. No.	Frequency	Vout (V)	20log(Vo/Vi) dB
1	10.3	1.9	11.59
2	19.2	2	12.04
3	35.15	3.8	17.61
4	54	4.2	18.48
5	76	4.4	18.89
6	100	4.5	19.08
7	167	4.6	19.27
8	292.4	4.7	19.46
9	932	4.8	19.64
10	14.09K	4.6	19.27
11	31.45K	4.4	18.88
12	46K	4.2	18.48
13	64.3K	4	18.06
14	94.1K	3.8	17.61
15	178.3K	3.4	16.65
16	282.3K	3	15.56
17	383K	2.7	14.64
18	500K	2.2	12.86
19	730K	2	12.04
20	950K	1.8	11.12
21	1009K	1.8	11.12

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iv) Miller effect due to C_{cb} :

Disconnect 1-1' and 4-4' are connected :

$V_{in} = 0.5V$

Sl.No.	Frequency(Hz)	Vout(V)	20log(Vo/Vi) db
1	9.47	0.72	3.167
2	14.91	0.86	4.71
3	21.58	0.88	4.91
4	35.41	0.92	5.29
5	51.1	0.94	5.48
6	61.8K	0.92	5.29
7	138.9K	0.88	4.91
8	198.6K	0.84	4.506
9	257.8K	0.8	4.08
10	351.4K	0.72	3.167
11	466K	0.64	2.14
12	503K	0.6	1.58
13	574K	0.56	0.98
14	707K	0.48	-0.35
15	920K	0.40	-1.93
16	1000K	0.36	-2.8

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b) Terminals 4-4' are disconnected:

Sl. NO.	Frequency	Vout(V)	20log (Vo/Vi) db.
1	10.63	0.76	3.636
2	21.05	0.84	4.506
3	51.8	0.86	4.71
4	76.6	0.92	5.29
5	79.2	0.94	5.48
6	116.9	0.94	5.48
7	37.93k	0.92	5.29
8	240.2k	0.88	4.91
9	348.3k	0.84	4.506
10	412 K	0.80	4.08
11	542k	0.76	3.636
12	632 K	0.72	3.167
13	678K	0.68	2.67
14	761K	0.64	2.14
15	864K	0.6	1.58
16	931K	0.56	0.98
17	1002K	0.54.	0.668

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~~DISCUSSION:~~

MEASUREMENT OF INPUT RESISTANCE IN MID-FREQUENCY RANGE:

$V_{in} = 500mV$. $R_x = 1k\Omega$

Frequency = 4KHZ.

$R_s (\Omega)$	$V_{out}\|_o$ (V)	$V_{out}\|_{R_x}$ (V)	R_{IN} $\frac{R_x \cdot V_{out}\|_{R_x}}{V_{out}\|_o - V_{out}\|_{R_x}} - R_s$
50Ω	3.2V	2.7V.	5350Ω
600Ω	2.6V	2.24V	5560Ω

MEASUREMENT OF OUTPUT RESISTANCE IN MID-FREQUENCY RANGE:

$V_{in} = 150mV$ $R_L = 1K\Omega$

Frequency = 4KHZ.

$R_s(\Omega)$	$V_{out}\|_{R_L}$ (V)	$V_{out}\|_\infty$	R_{OUT} $R_L \cdot \frac{V_{out}\|_\infty - V_{out}\|_{R_L}}{V_{out}\|_{R_L}}$
50Ω	0.41V	3.2V	6805Ω
600Ω	0.39V	3.0V.	6894Ω

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DISCUSSION:

Swastika Dutta
(16CS10060)

In active region, BE is forward biased while BC is reverse biased. Thus suitable V_g is applied such that saturation level is not reached (less than V_{sm}). Hence we achieve an amplified output voltage without deformation in signal waveform

The capacitors used at input and output act as coupling capacitors and DC blocking capacitors. The offset DC voltage effect and sine voltage effects can be superposed on the circuit to find the net effect. Capacitor acts as open circuit for DC current and allows current to pass at high ~~circ~~ frequencies (high pass ~~circuit~~ filter). Suitable values of capacitors are used to reduce attenuation of input voltage. Again, this setting does not bring about change of DC Quiescent point (i.e., maintains it at active region).

In signal handling experiment, we show the working of voltage divider. Thus, V_0 reduced and gain(A) = V_0/V_i reduced subsequently. However, bias stability of the circuit increases on account of voltage divider biasing.

In measurement of frequency response, voltage gain improved from 7.00 to 24.64db, alongside reduction in cutoff frequency as depicted in the results.

In the next part of the frequency response experiment, we use C_E as a bypass circuit for resistors R_{E1} and R_{E2}.

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Reduction of resistance in path of input (Base-emitter loop) increases I_B, and subsequent increase in $I_C (= \beta I_B)$. Thus, saturation point is reached at a lesser v_i, transistor was becoming saturated. Also the voltage gain improved from max at 1.289 to max at 19.64 when R_{E1} & R_{E2} were bypassed.

In the next part of the experiment, we consider Miller effect. This effect is observed due to presence or absence of C_{cb} in the circuit. This is also called feedback effect. The capacitive feedback from collector to base effectively multiplies C_{cb} with β. The amount of negative gain-reducing feedback is related to both current gain and amount of collector-base capacitance.

Then in the last part of the experiment we took mid-frequency range and calculated the ~~a~~ input and output resistances in respective cases.

10/10 KBP

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Discussion :-

By Chelsi Raheja
(16CS10013)

1. For BJT to work as an amplifier, it should operate in its active region where the configuration between base-emitter junction is in FB but base-collector junction is in Reverse Bias. We should have kept voltage quite below V_{sm}, i.e. the maximum input voltage for which the gain remains almost constant. This is called signal handling capacity.

2. ~~The~~ Observation of V_{sm} ~~for~~ was obtained by ~~a~~ voltage that initiates the distortion of CRO displayed output voltage curve. Voltage above V_{sm} leads the transistor to switch to saturation region where both junctions are in forward bias.

3. R_1 and R_2 are providing voltage divider biasing which provides stability such that $I_B << I_{R_2}$ which implies V_B almost constant.

4. C_{c_2} capacitor was used to avoid change in Q-point by the load because direct coupling without C_c leads to voltage divider b/w R_C and R_L ~~whereas~~ which leads to change in Q-point.

Direct coupled: $V_C = V_{CC} \frac{R_L}{R_C + R_L}$ Capacitor-coupled: $V_C = V_{CC} - I_C R_C$

5. C_{c_1} capacitor was similarly used to avoid formation of voltage divider by R_1 and $R_2 \| R_S$ to limited involvement of only two resistors R_1 and R_2 to form voltage divider such that $V_B = V_{CC} \frac{R_2}{R_1 + R_2}$ stays valid.

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6. In measurement of frequency response, voltage gain improved from 7 db ~~2~~ to 24.64 db alongside reduction in cut-off frequency

7. R_{E1} and R_{E2} as emitter resistances are used to provide ~~stability~~ biasing stability, i-e, change in I_C is reduced by a factor of R_E but ~~red~~ increment in stability cost for the output voltage supplied. R_E are acting as feedback resistors (negative).

8 If Vin increases leading increment in I_C which leads to decrease in V_{CE} which lead to decrement in I_B due to R_1 which leads to decrease in I_C. Thus, providing good-bias stability with reduced gain and less distortion in input waveform.

9 C_{cb} also act as feedback capacitor across base collector which is used to restrict the range of operation to lower frequensies. Stray capacitance ~~incre~~ between capacitor and base increase by Miller effects due to its high gain lowering the high frequency response of the device.

10 Increment in Vin resulting in increment in V_{RE} as I_B increases leading to reduced increase in V_B leading to avoid thermal runaway because increase in I_B to a large extent ~~to~~ heat up the transistor which will require more bias current to provide same bias voltage and

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also as R_1 / R_2 voltage divider is designed to provide the correct quiescent current through base to operate it in desired operation needs to get changed. ~~its~~ leading to errors in output to a large extent.

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