Switching Theory & Logic Design Laboratory
CSE Department, IIT Kharagpur
Spring Semester 2022-23

Module 3 : SEQUENTIAL CIRCUITS AND FSM

Assignment 7 :

1. Design of Synchronous Sequential Circuits

   a. Design a circuit that will take a serial bit stream as input in synchronism with a clock, and will output a 1 whenever the pattern (possibly overlapping) 01001 is encountered.
   b. Design a modulo-10 synchronous binary counter using JK flip-flops.

(1 day)