1. According to Amdahl's Law

   SpeedUp = 1/((1-f) + f/s)

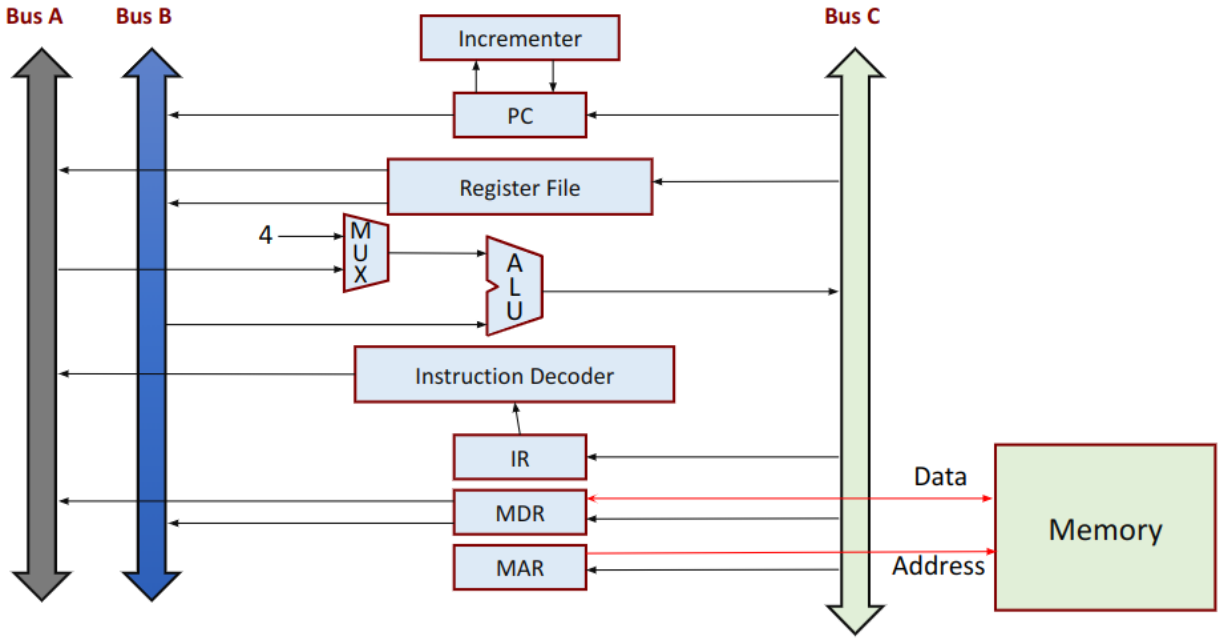
   Design 1: 1/(0.95 + 0.05/2) = 1.0256
   Design 2: 1/(0.8 + 0.2/ 1.8) = 1.0977
   Design 3: 1/(0.55+ 0.45/1.5) = 1.1765
   Design 4: 1/(0.7 + 0.3/1.1) = 1.0277

   Design 3 is the best design.

2. 64 registers can be addressed by 6 bits
   I type instruction: 6 bit opcode, 6 bit register, 4 bit immediate value
   R type instruction: 4 bit opcode, 6 bit src register, 6 bit dst register
   There can be maximum 16 distinct opcodes possible since there are 4 bit opcodes in R type instruction.

3. i) RISC processor has large number of general purpose registers.
   ii) RISC supports fewer addressing modes than CISC.
   iii) Instructions in RISC processor are of same size.
   iv) RISC has fewer number of instructions than CISC.
   v) RISC does not have flag registers and general purpose registers.
   vi) RISC instructions are easier to decode than CISC.

4a) Three bus architecture



4b) BEQZ Label

T1: PC_out, MAR_in, Read, Select_4, Add, Z_in
T2: Z_out, PC_in, Y_in, WMFC
T3: MDR_out, IR_in
T4: Offset-field-of-IR_out, Select_Y, Add, Z_in, If Z != 0 then End
T5: Zout, PCin, End

LOAD R2, 2000

T1: PC_out, MAR_in, Read, Select_4, Add, Z_in
T2: Z_out, PC_in, Y_in, WMFC
T3: MDR_out, IR_in
T4: Address_field_of_IR_out, MAR_in, Read, WMFC
T5: MDR_out, R1_in, END