COA Lab - Assignment 9

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1 Introduction

In this project, we designed a circuit that takes a 32-bit input x (4 bytes) and computes the value of $y = \frac{x}{255}$ without using any multiplier or division unit. The circuit utilizes an 8-bit subtractor and shifters as the primary data path elements. To achieve this, we use the equation $y = 256y - x$ as a basis for our design.

2 Approach

To divide x by 255, we adopted a bit-by-bit division approach, which involves calculating the quotient and remainder iteratively. Here is an overview of our approach:

1. Initialize the quotient and remainder to zero.
2. For each bit of the input x from the most significant bit (MSB) to the least significant bit (LSB):
    - Shift the remainder left by one bit and append the current bit of x.
    - If the remainder is greater than or equal to 255, subtract 255 from the remainder and set the least significant bit of the quotient to 1; otherwise, set the least significant bit of the quotient to 0.

3 Pseudocode

We describe the algorithm in pseudocode:

```
remainder = 0
quotient = 0
for i from 15 downto 0:
    remainder = (remainder << 1) | x[i]
    if remainder >= 255:
```

```
        remainder = remainder - 255
        quotient = (quotient << 1) | 1
    else:
        quotient = (quotient << 1)
```

4 Conclusion

We successfully designed a circuit to compute $y = \frac{x}{255}$ using an 8-bit subtractor and shifters. Our approach involves iteratively calculating the quotient and remainder for each bit of the input. The circuit can be implemented in FPGA devices to perform the desired division operation.

5 Implementation

We implemented the Verilog code in the Xilinx tool for FPGA realization and also created a test bench for simulation. The top-level module `divide` is structural, while the internal modules may be behavioral. We downloaded the bitstream onto the FPGA device and demonstrated its working.