CMP 334 Practice Exam 2 (Spring 2019)

1) For each row in the following table, determine whether the assertion would hold if the indicated operation produced the indicated condition flag values.

	operation		flags	assertion	T / F
a	**A** $\overset{\cdots}{+}$ **B**	unsigned	$\overline{Z}N\overline{C}V$	result is honest	
b	**A** $\overset{\cdots}{+}$ **B**	signed	$\overline{Z}N\overline{C}\overline{V}$	result is honest	
c	**A** $\overset{\cdots}{-}$ **B**	unsigned	$\overline{Z}\overline{N}CV$	result is honest	
d	**A** $\overset{\cdots}{-}$ **B**	signed	$\overline{Z}\overline{N}CV$	result is honest	
e	**A** $\overset{\cdots}{-}$ **B**	unsigned	$\overline{Z}N\overline{C}\overline{V}$	**A** $\leq$ **B**	
f	**A** $\overset{\cdots}{-}$ **B**	signed	$\overline{Z}\overline{N}CV$	**A** < **B**	
g	**A** $\overset{\cdots}{-}$ **B**	unsigned	$\overline{Z}\overline{N}CV$	**A** $\geq$ **B**	
h	**A** $\overset{\cdots}{-}$ **B**	signed	$\overline{Z}N\overline{C}V$	**A** < **B**	
i	**A** $\overset{\cdots}{-}$ **B**	unsigned	$\overline{Z}N\overline{C}V$	**A** $\leq$ **B**	
j	**A** $\overset{\cdots}{-}$ **B**	signed	$\overline{Z}N\overline{C}\overline{V}$	**A** > **B**	
k	**A** $\overset{\cdots}{-}$ **B**	unsigned	$\overline{Z}N\overline{C}\overline{V}$	**A** < **B**	
l	**A** $\overset{\cdots}{-}$ **B**	signed	$\overline{Z}\overline{N}\overline{C}\overline{V}$	**A** $\leq$ **B**	
m	**A** $\overset{\cdots}{-}$ **B**	unsigned	$\overline{Z}N\overline{C}\overline{V}$	**A** $\geq$ **B**	
n	**A** $\overset{\cdots}{-}$ **B**	signed	$\overline{Z}N\overline{C}\overline{V}$	**A** > **B**	

2) Draw a Boolean circuit, having the condition flags – **Z**, **N**, **C**, and **V** – as inputs, that will be 1, following the execution of the instruction: `sub $0, $5, $6` if, and only if, the signed integers **A** and **B** in registers $5 and $6 (respectively) satisfy the relationship **A > B**.

3) Write a **TOY** AL subprogram to determine the number of distinct values in three registers (that is: **3**, if all three values are different; **2**, if two registers have the same value but the other is not; and **1**, if all three retisters are equal) consistent with the following subprogram interface:

Label: `Diff`

On entry:

Register **`$1`** is the return address of the caller.

The registers in question are **`$A`**, **`$B`**, and **`$C`**.

`@B` (the address in memory of variable **`B`**) is **`@A+7`**.

On exit:

The result will be in register **`$F`**.

Registers **`$4`** to **`$F`** may have been changed; registers **`$0`** to **`$3`** will not have been.

Main memory will be unchanged.

4) Write a **TOY** AL subprogram to accomplish the following assignment:

```
A = (A + B) & (17 - B)
```

consistent with the following subprogram interface:

Label: `AB17`

On entry:

Register **`$1`** is the return address of the caller.

`@A` (the address in memory of variable **`A`**) is in register **`$A`**.

`@B` (the address in memory of variable **`B`**) is **`@A+7`**.

On exit:

Variable **`A`** will have been updated; no other values in main memory will have changed.

Registers **`$4`** to **`$F`** may have been changed; registers **`$0`** to **`$3`** will not have been.

5) Write a **TOY** AL subprogram to negate each of the elements of an array **`A`**, consistent with the following subprogram interface:

Label: `Negate`

On entry:

Register **`$1`** is the return address of the caller.

Register **$B**. contains n the number of elements in the array **A**.

@B (the address in memory of variable **B**) is **@A+7**.

On exit:

The elements of **A** will have been negated; other memory values will be unchanged.

Registers **$4** to **$F** may have been changed; registers **$0** to **$3** will not have been.

6) Follow the four step combinational circuit design process outlined below to design a circuit for a Boolean function that takes as input two 2-bit ***signed*** integers, **A** and **B**, and outputs 1 if, and only if, their difference, **A – B**, is **4**.

a) Draw a black box for the circuit that specifies its inputs and output.

b) Formalize the informal semantics of this circuit with a truth table.

c) Construct the boolean formula corresponding to the truth table.

d) Draw the circuit corresponding to the boolean formula.

7) For the following distribution of instructions

40% ALU instructions
20% Load instructions
15% Store instructions
20% Conditional branch instructions
5% Unconditional branch instructions

a) How many memory accesses are required for each instruction (on average)?

b) On a multi-cycle per instruction processor: ALU instructions require 5 cycles; loads, 9 cycles; stores, 7 cycles; **taken** conditional branches, 8 cycles; not taken conditional branches, 6 cycles; and unconditional branches, 4 cycles. If one fifth of all conditional branches are taken, what is the CPI for this distribution of instructions?

For the parts **c**, **d**, and **e**, assume that the processors execute instructions in the following stages:

IM — 100 ps
RR — 100 ps
EX — 200 ps
DM — 250 ps

RW — 150 ps.

c) What would be the cycle time of a single-cycle-per-instruction-execution processor having these stages?

d) What would be the cycle time of a pipeline processor with these stages?

e) What would be the speedup of the pipeline processor in **d** over the single-cycle processor of **c**?

8) Assuming the same distribution of instructions as in problem 7, compute the stall cycles per instruction SCPI due to each of the following four hazards:

a) a 1 cycle delay for 1 of every 20 load instructions.

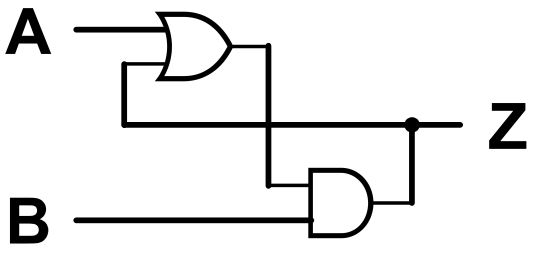
b) a 2 cycle delay for a quarter of the conditional branch.

c) a 40 cycle delay for 1 of every 900 memory accesses.

d) a 5,000 cycle delay for 3 of every 100,000 instructions.

e) What is would be the actual CPI for a pipeline processor experiencing these four hazards (assuming that its perfect pipeline CPI = 1)?

9) Complete the transition truth table for the following circuit:



A	B	$Z_{(old)}$	$Z_{(new)}$
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

10) Program Q takes 45 seconds to run on processor X and 18 seconds to run on processor Y. The clock rate for X is 2 GHz and for Y is 4 GHz. The CPI of Y is 3.6. Both processors implement the same instruction set architecture.

a) What is the relative performance of Y to X?

b) How many instructions are executed running program Q?

c) What is the CPI for X?