HW 15: Memory Access Costs

a) Computer A had a processor that connects to an L_1 cache with a hit-cost of *1* cycle and a hit-rate of 99%. The L_1 cache connects to a main memory with hit-cost of *500* cycles. What is the **memory access cost** of Computer A?

b) Computer B is Computer A with a L_2 cache between the L_1 cache and main memory with hit-cost of *15* cycles and a miss-rate of 5%. What is the **memory access cost** of Computer B?

c) Computer C is Computer B with an L_3 cache between the L_2 cache and main memory with a hit-cost of *25* cycles and a miss-rate of 7%. What is the **memory access cost** of Computer C?

d) If the processor generates (on average) 1.25 memory accesses for each instruction, how many **stall cycles per instruction** are due to memory accesses on Computer C?