CMP 334 practice final (Spring 2019)

- 1) Given: X = 0x6E and Y = 0x9B,
 - a) Convert X and Y to 8-bit binary numbers.

X=01101110 Y=10011011

b) Compute the 8-bit sum X + Y of X and Y.

```
\begin{array}{c} 01101110 \\ \underline{10011011} \\ {}^{11111110} \end{array} + \\ \mathbf{1}00001001 \end{array}
```

c) Compute $\ddot{\mathbf{Y}}$ the 8-bit two's complement of Y.

01100100

d) Compute the 8-bit difference X-Y of X and Y. (Use two's complement addition.)

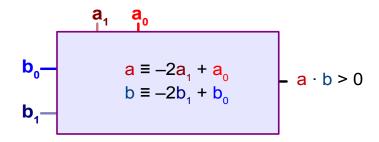
$$\begin{array}{c} 01101110 \\ \underline{01100100} \\ {}^{01101100} \\ 011010010 \\ \end{array} +$$

e) Convert X+Y, Y, and, X-Y to hexadecimal.

0x09 0x64 0xD2

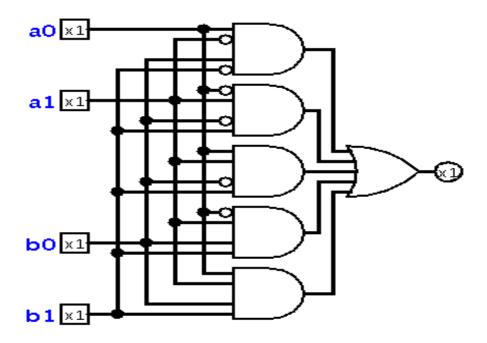
- f) What are the values of the condition flags z n c v upon computing X+Y?
- g) What are the values of the condition flags z n c v upon computing X Y?
- h) T or F The *unsigned* 8-bit sum X + Y is honest. c=1
- i) T or \mathbb{F} The signed 8-bit sum $\mathbf{X} + \mathbf{Y}$ is honest. $\mathbf{v} = \mathbf{0}$
- j) T or F The unsigned 8-bit difference X-Y is honest. c=0
- k) T or F The signed 8-bit difference X-Y is honest. v=1
- 2) Use the combinational circuit design process:
 - a) Draw a black box for the circuit that specifies its inputs and output.
 - b) Formalize the informal semantics of this circuit with a truth table.
 - c) Construct the boolean formula corresponding to the truth table.
 - d) Draw the circuit corresponding to the boolean formula.

to design the circuit that takes as input two 2-bit *signed* integers $\bf a$ and $\bf b$ and is $\bf 1$ if $\bf a \cdot \bf b > 0$



b ₁	b _o	a ₁	a _o	b	а	a· b	a · b > 0	
0	0	0	0	0	0	0	0	
0	0	0	1	0	1	0	0	
0	0	1	0	0	-2	0	0	
0	0	1	1	0	-1	0	0	
0	1	0	0	1	0	0	0	
0	1	0	1	1	1	1	1	$\overline{\mathbf{b}}_{1}\mathbf{b}_{0}\overline{\mathbf{a}}_{1}\mathbf{a}_{0}$
0	1	1	0	1	-2	-2	0	
0	1	1	1	1	-1	-1	0	
1	0	0	0	-2	0	0	0	
1	0	0	1	-2	1	-2	0	
1	0	1	0	-2	-2	4	1	$\mathbf{b}_{1}\overline{\mathbf{b}}_{0}\mathbf{a}_{1}\overline{\mathbf{a}}_{0}$
1	0	1	1	-2	-1	2	1	$\mathbf{b}_{1}\overline{\mathbf{b}}_{0}\mathbf{a}_{1}\mathbf{a}_{0}$
1	1	0	0	-1	0	0	0	
1	1	0	1	-1	1	-1	0	
1	1	1	0	-1	-2	2	1	$\mathbf{b}_{1}\mathbf{b}_{0}\mathbf{a}_{1}\mathbf{\overline{a}}_{0}$
1	1	1	1	-1	-1	1	1	$\mathbf{b}_{1}\mathbf{b}_{0}\mathbf{a}_{1}\mathbf{a}_{0}$

$$\overline{\boldsymbol{b}}_1\boldsymbol{b}_0\overline{\boldsymbol{a}}_1\boldsymbol{a}_0 + \ \boldsymbol{b}_1\overline{\boldsymbol{b}}_0\boldsymbol{a}_1\overline{\boldsymbol{a}}_0 + \boldsymbol{b}_1\overline{\boldsymbol{b}}_0\boldsymbol{a}_1\boldsymbol{a}_0 + \boldsymbol{b}_1\overline{\boldsymbol{b}}_0\boldsymbol{a}_1\boldsymbol{a}_0 + \boldsymbol{b}_1\boldsymbol{b}_0\boldsymbol{a}_1\overline{\boldsymbol{a}}_0 + \boldsymbol{b}_1\boldsymbol{b}_0\boldsymbol{a}_1\boldsymbol{a}_0 = \boldsymbol{b}_1\boldsymbol{a}_1 + \ \overline{\boldsymbol{b}}_1\boldsymbol{b}_0\overline{\boldsymbol{a}}_1\boldsymbol{a}_0$$



3) Write **TOY** AL subprogram that implements the following <u>subprogram interface</u>:

Label: ArrayAnd

On entry:

Register \$1 is the return address of the caller.

A, **B**, and **C** are non overlapping arrays in memory.

Register \$D contains **n**, the size of all three arrays.

On exit:

C[i] = A[i] & B[i] for all i such that $0 \le i < n$.

Otherwise, no values in memory have changed.

Any of the registers may have changed value.

4) Write **TOY** AL subprogram that implements the following <u>subprogram interface</u>:

Label: Mult

On entry:

Register **\$1** is the return address of the caller.

On exit:

Register \$F contains the (unsigned) product of the unsigned values in registers \$A and \$B. (Note: your result need not be accurate unless these values are less than 256.)

Main memory will not have changed, but any of the registers may have.

```
0
Mult
            lis
                  $F,
                       0
                                           $F
            lis
                  $9,
                                           $9
                       1
                                                     1
Loop
            sub
                  $0, $B, $0
                                           $В
                                                 ?
                                                     0
                  EQ, Done
            bc
                  $F, $F, $A
            add
                                           $F
                                                    $F + $A
                  $B, $B, $9
                                           ŚΒ
                                                    $B - 1
            sub
                                    :
                  ALL, Loop
            bc
                  ALL, $1, $0
Done
            bcl
                                           return
```

5 a) Computer A had a processor that connects to an L₁ cache with a hit-cost of 1 cycle and a miss-rate of 4%. The L₁ cache connects to a main memory with hit-cost of 600 cycles. What is the *memory access cost* of computer A?

```
MAC_{\Delta} = 1 + 0.04 * (600) = 25
```

b) Computer B is computer A with a L_2 cache between the L_1 cache and main memory with hit-cost of 15 cycles and a miss-rate of 10%. What is the *memory access cost* of computer B?

$$MAC_{B} = 1 + 0.04 * (15 + 0.1*(600)) = 1 + 0.04*75 = 1 + 3 = 4$$

c) Computer C is computer B with an L₃ cache between the L₂ cache and main memory with a hit-cost of 30 cycles and a miss-rate of 20%. What is the *memory access cost* of computer C?

$$MAC_C = 1 + 0.04 * (15 + 0.1*(30 + 0.2*(600))) = 1 + 0.04*(15 + 0.1*150) = 2.2$$

d) On program P with an execution consisting of 50% ALU instructions, 20% load instructions, 5% store instructions, and 25% branch instructions, how many memory accesses per instruction are there on computer C? How many *stall cycles per instruction* are due to memory accesses on execution of program P on computer C?

```
SCPI = MAPI * (MACC - 1) = 1.25 *1.2 = 1.5
```

6) Consider a disk with the following specifications:

```
block size 512 bytes sectors per track 400 overhead 2.5 ms seek time 20 ms rotation speed 12000 RPM
```

a) How big is a track on this disk in bytes?

```
1 track = 512 bytes \frac{\text{per block}}{\text{per block}} \cdot 400 \frac{\text{blocks}}{\text{blocks}} = 204800 \text{ bytes}
```

b) What is its rotation time in ms?

$$1/12000 \cdot 60/1 * 1000/1 = 60/12 = 5 \text{ ms}$$

c) What is its bandwidth in megabytes per second?

```
204800 / 5 * 1000 / 1000000 = 40960 / 1000 = 40.96 Megabytes per second
```

d) What would be the data transfer time in ms of a record 768,000 bytes long?

$$76800 / 4096 = 4800 / 256 = 300 / 16 = 75 \text{ ms}$$

e) What would be the total disk access time in ms for this record?

$$2.5 + 20 + 5/2 + 75 = 100 \text{ ms}$$

7) Co	nsider	the following	g TOY A	ssembly Lan	guage ins	tructions:		
	A)	add,	B)	and,	C)	bc,	D)	1,
	E)	lis,	F)	nor,	G)	st,	H)	sub,
a)	Whic	A, B, D, E, F, H						
b)	Whic	G						
c)	Whic	С						
d)	Whic	A, B, F, H						
e)	Whic	C, D, E, G						