HW 14 Pipeline Performance

This problem considers the performance of several implementations of the same instruction set architecture on a suite of programs with the following characteristics:

ALU instructions	45%	
Load instructions	20%	
Store instructions	10%	
Branch instructions	25%	
Unconditional	5%	
Conditional	20%	
Backward	16%	(taken 6%, not taken 10%)
Forward	4%	(taken 2%, not taken 2%)

HW 14 part A

A multiple-cycle serial implementation has the following cycle counts for the various instructions:

ALU instructions	3 cycles
Load instructions	8 cycles
Store instructions	6 cycles
Unconditional branches	3 cycles
Taken conditional branches	5 cycles
Not-taken conditional branches	4 cycles

What is the CPI of the program suite on this implementation?

HW 14 part B

A second serial implementation executes every instruction in a single cycle. Instruction execution is performed in the following phases having the indicated execution times:

IF	instruction fetch	150 ps
RR	register read	100 ps
EX	ALU operation	400 ps
MW	memory write	300 ps
MR	memory read	150 ps
RW	register write	100 ps

How long is the cycle time for this implementation?

HW 14 part C

A third implementation executes instructions in a pipeline using the stages given in part B.

How long is the cycle time for this implementation?

What is the relative performance of this implementation to that of part B?

HW 14 part D

A final implementation is also a pipeline of the stages given in part B except that the execute phase, EX, is partitioned into two phases, EX1 and EX2 each requiring 200 ps.

How long is the cycle time for this implementation?

What is the relative performance of this implementation to that of part C?