CMP 334 Spring 2019 Quiz 6 Name ________________

The problem considers various implementations of the same ISA running a program with the following distribution of instructions: 50% ALU, 20% Load, 10% Store and 20% Branch.

1) How many memory accesses per instruction are there for this distribution?

MAPI = # fetches + # loads + # stores = 1.0 + 0.2 + 0.1 = 1.3

On implementation 1, execution of ALU instructions take 4 cycles; loads, 5 cycles; stores, 6 cycles; and branches, 7 cycles.

2) What is the average CPI (cycles per instruction) for this distribution?

$\text{CPI} = 0.5 \cdot 4 + 0.2 \cdot 5 + 0.1 \cdot 6 + 0.2 \cdot 7 = 5$ cycles per instruction.

Implementation 2 executes all instructions in a single cycle composed of these 5 stages (with their execution times): IM (400 ps), RR (300 ps), EX (800 ps), DM (600 ps), and RW (300 ps).

3) What is the cycle-time of this implementation?

$\text{Cycle-time}_2 = 400 + 300 + 800 + 600 + 300 = 2400$ ps.

On this implementation, the program executes in 36 seconds. There are 10^{12} ps in a second.

4) How many instruction are executed running the program?

$36 \cdot 10^{12} = \#\text{instructions} \cdot \text{CPI}_2 \cdot 2400$

$\#\text{instructions} = 36 \cdot 10^{12} / (\text{CPI}_2 \cdot 2400) = 36 \cdot 10^{13} / 1 \cdot 2.4 \cdot 10^{3} = 15 \cdot 10^{9}$

Implementation 3 executes the same stages as Implementation 2 in a perfect pipeline.

5) What is the cycle-time of implementation 3?

$\text{Cycle-time}_3 = \max(400, 300, 800, 600, 300) = 800$ ps.

6) What is the relative performance of implementation 3 to implementation 2?

P3 / P2 = T2 / T3 = 2400 / 800 = **3**.

Implementation 4 is the same pipeline as implementation 3 except that 1 in 10 branch instruction is delayed 2 cycles.

7) What is the SCPI (stall cycles per instruction) for this implementation?

$\text{SCPI}_4 = 0.2 \cdot 0.1 \cdot 2 = 0.04$

8) What is the CPI for this actual pipeline?

$\text{CPI}_4 = \text{CPI}_{pp} + \text{SCPI}_4 = 1 + 0.04 = 1.04$