HARI SHASHANK SINGH THAKUR

(971)-427-9428 | harishashanksinghthakur@gmail.com| www.linkedin.com/in/hari-shashank

Objective

Aspiring Design Verification Engineer with 1.5 years of experience, looking for new opportunities in RTL Design/Verification.

Education

Master of Science in Electrical and Computer Engineering **Sep 2022-June2024**

Portland State University, Portland Oregon**.** **GPA: 3.82/4.0**

Coursework: Microprocessor system design, Computer architecture, System Verilog, ASIC Modelling and Synthesis, Formal Verification, Post Silicon Validation, Digital IC Design, Advance Computer Architecture.

Bachelor of Engineering in Electronics and Communication **July 2018-June 2022**

Osmania University, Hyderabad, India **GPA: 3.7/4.0**

Technical Skills

Languages: Proficient in System Verilog, Verilog, C, UVM/UVM Framework, comfortable with Python .

Operating Systems: Windows, Linux. **Protocols:** MESI, AHB, APB, AXI, I2C, SPI, UART,DDR

Technical Tools: Questa Sim, Visualizer, EDA playground, QVIP configurator, Xilinx-Vivado, QVRM, SVVA (SystemVerilog-VHDL Assistant)., Cadence Virtuoso, Vmanager, Verissimo (Testbench Linter)

Technical Concepts: System Verilog assertions, Coverage, Constraints, Cache Coherency, Branch Prediction, Pipelining, UVM Environment Components, RAL Model ,STA, TBX, DPI Pipes, Class Based Verification concepts, Virtual sequencer, UVM,Factory, TLM ports, UVM Phases, Test planning and Debugging. CDC, synchronizers, linting.

Work Experience

Onsemi: Digital Verification Engineer [Full-Time] Corvallis, Oregon **July 2024-Present**

- Responsible for Block level verification of a hardware security system used in Next-Gen Image sensors ,developing verification environment, writing directed, random testcase and running regressions and top-level simulations.
- Ensuring a bug-free designs by verifying corner scenarios and perform an analyze the design functionality in real-time by using emulator.
- Verification owner for an OTPM memory block, verified corner cases, test planning and debugging and developing a re-usable UVM environment with DPI-C interfaces for C- based reference model and find bugs and working with design teams for coverage closure.
- Verified Cryptographic RTL designs for AES128 engine, CMAC modules developing random and directed testcases and perform coverage closure.
- Collaborate with algorithm development teams and verify and compare RTL with algorithm models and identified bugs and reported for a bug free development of reference model.

Onsemi: Digital Verification Intern Corvallis, Oregon **June 2023-May 2024 [1 year]**

- Understand the working of cybersecurity based cryptographic algorithms utilized in development of security blocks of an image sensor.
- Developed re-usable verification environments for hardware security block developed using cryptographic algorithms for image sensor using UVM framework for simulation and emulation.
- Developed and implemented RAL based test sequences both directed and constraint randomized driven cases for efficient verification of sub-system blocks including advanced C models and DPI-C interfaces and check for bugs and perform regression testing using regression management tools and improve coverage and perform coverage closure.
- Collaborate with senior verification engineers and helped in developing testplan , functional coverage and writing directed and random testcases compliant with various rulesets for better practices for complex UVM environments and perform emulation of RTL blocks using veloce.

Technical Projects

[System Verilog/UVM]: Developed UVM based verification environment for ALU design

- Developed a re-usable, maintainable verification environment with Master/Slave agents with in-order scoreboard component.
- Developed a DPI-C reference model with predictor component to compare and functionally verify the RTL responses for the developed constraint randomized and directed testcases.

[System Verilog/UVM]: Developed UVM Environment for Router 4x4 Design

- Developed the following Environment Components Master &Slave Agents, Out-of order Scoreboard, call backs to implement error injections.
- Developed RAL Environment to configure CSR registers, Developed Test plan and directed and randomized Testcases and including Coverage component to functionally verify all corners in design.

[System Verilog/UVM]: AXI VIP Development for Multi-Master/Multi-Slave Interface

- Developed Multiple testcases to verify all features of AMBA-AXI protocol including out of order transactions.
- Verified various combinations of AXI length and size transactions for multiple interfaces using virtual sequencer.