Sayantan Ghosh

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Professional Summary

Experienced Physical Design Engineer with 7 years in Physical Design and 3 years in Layout Design. Proven track record in successful Tape-Outs of multi-million gate blocks across diverse process technologies, methodologies, and collaborative teams.

Education

University of Minnesota, Twin Cities **January 2024 - Expected May 2025**

Master of Science in Electrical and Computer Engineering *GPA: 3.667*

West Bengal University of Technology (WBUT) **June 2012**

Bachelor of Technology in Electronics and Communication Engineering

Professional Experience

Physical Design Engineer, Technical Lead **May 2019 – August 2023**

Synapse Design Automation, Inc. *Client – Mediatek, Marvell/Global Foundries*

- Worked on TSMC 4nm ASIC design, handling a partition with 324 macros and 2 million plus standard cells.
- Orchestrated floorplanning, placement, clock tree synthesis (CTS), and routing stages for ASIC design, achieving signoff for timing, PDN, and PV across three tape-outs in 4nm and 7nm nodes.
- Provided technical leadership to a team of 7 junior engineers with issue resolution in block-level implementation, ensuring successful project execution through effective project planning and resource management.
- Conducted experiments to improve PPA and power efficiency of the high-frequency application processor in 4nm, along with improving congestion and density.
- Performed Static Timing Analysis, identifying critical timing paths and generating Engineering Change Orders (ECOs) in PrimeTime and Tweaker to resolve timing violations, ensuring Formal Equivalency effectively.
- Handled multiple partitions in 4nm, 7nm technology with more focus on pin optimization, and congestion analysis

Senior Physical Design Engineer **June 2016 – May 2019**

Pozibility Technologies *Client – Global Foundries, Western Digital/Sandisk*

- Performed Netlist to GDSII implementation of four Memory Controller (NAND Flash Interface Module) blocks in 14nm, each with over 1.2 million instances, utilizing synthesis and place and route flows.
- Optimized skew balancing through manual pre-placement and pre-routing during the initial design stage, ensuring critical clock distribution.
- Executed block-level implementation on 12FDX technology, ensuring timing closure for high-frequency clocks and completing physical verification. Minimized IR-Drop and EM effects for power and signal integrity.
- Collaborated closely with RTL and DFT designers to ensure high-quality design implementation.
- Implemented functional ECOs to optimize design performance, completed physical verification, and achieved full signoff closure including critical reset timing closure.
- Performed timing closure of a partition with 2M instances by understanding the design, and applying PD constraints like group path, bounds, NDR, false path, multi-cycle paths, and macro placement.

Layout Design Engineer **April 2015 – May 2016**

Tata Elxsi *Client – Qualcomm*

- Developed and optimized 10nm leaf cells, delivered SPEF-extracted RC for verification, implemented ECOs, created characterization cells, and ensured LVS clean-up, contributing to successful tape-outs.
- Performed EM/IR analysis, fixed Single Diffusion Break (SDB) errors, Density, Filling, ERC, Litho-Friendly Design Check, and DFM checks.

Graduate Engineer Trainee (Layout Design) **June 2013 – April 2015**

Synopsys, Inc

- Developed and optimized layout designs for High-Speed Dual Port Register File (HSRF2P) Compiler at 10nm and High-Density Single Port (HD1P) SRAM Compiler at 14nm, utilizing Galaxy Custom Designer.
- Designed and optimized Power Gating cells, X Decoder, and CAP cells. Created and validated characterization cells, performed LVS cleanup, and conducted parasitic extraction to ensure accurate modeling.
- Executed full physical verification and signoff processes at leaf and cluster levels, including DRC, LVS, ERC, EM/IR, Antenna checks, and Sanity checks.

Academic Projects

Design of Convolution and Max Pooling Module **April 2024**

- Designed a convolution and max pool module using RTL for a 4x4 image and 3x3 kernel; synthesized with Synopsys Design Compiler, and performed automatic PnR with Cadence Innovus.
- Performed DRC and LVS verification in Virtuoso using Calibre and executed timing sign-off with PrimeTime.

Static Timing Analysis (STA) Implementation **October 2024**

- Developed a tool to perform Static Timing Analysis (STA) on logical circuits present in the "ISCAS'85 and ITC'99 High-Level benchmark Models."
- Implemented modules for identifying functionalities like the critical path, load capacitance, arrival time, slew, and slack of every node using Non-Linear Delay Model (NLDM) based LUTs in C++ platform.

Analytical Placement of Standard Cells **November 2024**

- Designed and Implemented an Analytical Placement Engine for large-scale standard cell designs, based on the Quadratic placement approach with Cell Shifting technique and Hybrid Net Model.
- Achieved optimized wire length and congestion values across various chip sizes through the effective implementation of the engine and validated against IBM benchmark files to ensure accuracy and reliability.

Design and Layout of D-Flip Flop **January 2024**

- Implemented a positive Edge Triggered D-Flip Flop schematic and layout on Virtuoso and verified proper functionality pre and post-layout using HSPICE simulation and Cosmoscope.
- Optimized layout for minimal area, and maximum frequency and ensured DRC and LVS clean.

Research Work

- Contributing to the design and implementation of Heterogeneous SoC RISC-V with AI Accelerator in Intel 16nm under the supervision of Prof. Yu (Kevin) Cao in the Microelectronics Co-design Research Group.
- Executed block-level physical implementation and top-level integration of the accelerator core and RISC-V processor.
- Responsible for generating back-end design libraries (LIB, NDM, LEF) for all the collateral.
- Configured TSMC 28nm Memory Compiler on the research server for generating various memory configurations with different features.

Publication

- HW-SW Co-Design of A 28nm 2-Tier ViT Enabled by Advanced 3D packaging – Gopikrishnan Raveendran Nair, Emad Haque, Ziyao Yang, Sayantan Ghosh, Chaitali Chakrabarti, Yu Cao (Under Review)

Technical Skills

EDA Tools: Synopsys (IC Compiler, Fusion Compiler, Design Compiler, PrimeTime, TetraMAX, Formality, Library Compiler, ICV, VCS/Verdi, HSPICE, Tweaker), Cadence (Innovus, Genus, Virtuoso, Spectre, Pegasus), Siemens (Calibre, Modelsim), Xilinx (Vivado)
Programming/Scripting Languages: Makefile, TCL, Shell Script, UNIX utilities (sed, awk, etc.)
Technology Nodes/PDKs: 3nm, 4nm, 7nm, 12nm, 14nm, 28nm, 55nm, 65nm, 110nm, 130nm, 180nm
Areas of interest: Physical Design, Static Timing Analysis, Circuit Design, Low Power and VLSI CAD
Version Control System: Perforce, Git
Courses: VLSI Design, VLSI Design Lab, VLSI Design Automation

Teaching Assistant Experience

* Deployed and validated the TSMC 16nm AFDP (Academic Design Foster Package) PDK to ensure seamless accessibility for student use, resolving multiple PDK issues.
* Guided and supported 56 students in project implementation, assignment grading, and technical assistance for EE5323 VLSI Design I (Fall 2024) under the supervision of Prof. Yu (Kevin) Cao.
* Implemented three projects, i.e., TSMC 16nm Technology characterization, Delay Calculation and Optimization of a 3-Stage Logic, and Design of a 4-to-1 Integrate-and-Fire (IF) Neuron to enhance course understanding and created tutorial documents.
* Assisting and mentoring 44 students in EE5324 VLSI Design II (Spring 2025) under Prof. Yang Zhao by guiding projects, grading assignments, and providing homework support.
* Helped students learn layout design in TSMC 16nm.
* Led lab sessions, and provided hands-on assistance for EE2301 Introduction to Digital System Design under Prof. Ulya Karpuzcu (Spring 2025).