Keshava Reddygattu

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Experience

National Institute of Electronics & Information Technology (NIELIT) India **May 2024 - Aug 2024**

RTL Design Intern

- Orchestrated comprehensive functional verification workflows and conducted extensive static timing analysis, achieving a 10% reduction in design iterations across multiple projects, which accelerated overall project timelines by 20% and ensured the on-time delivery of critical systems.
- Led the implementation of advanced simulation techniques to enhance RTL designs, resulting in a significant increase in team productivity by 30%, thereby enabling a 15% faster development cycle and maintaining project completion rates within strict budgetary limits.
- Spearheaded cross-functional collaboration initiatives to streamline communication between design teams and management, leading to a remarkable improvement in project tracking efficiency by 25%, thus reducing time spent on status updates and enhancing overall project visibility.

Maven Silicon India

FPGA Hardware Acceleration Intern **Jan 2023 - Aug 2023**

- Spearheaded the design and implementation of FPGA-based accelerators, resulting in a 25% enhancement in processing performance across 10+ applications, while achieving a significant reduction in data processing times by an average of 40%, ultimately boosting project efficiency by 20%.
- Streamlined synthesis, place-and-route processes, and power constraints for multiple FPGA projects valued at $1.2 million, leading to a notable development time reduction of 30%, which accelerated project delivery timelines by three weeks.
- Collaborated with cross-functional teams to optimize hardware configurations and rigorously validate designs through comprehensive testing protocols, enhancing system reliability by 15% and enabling successful deployments across five major client platforms within tight schedules.

RTL Design & Verification Intern **May 2022 - Jan 2023**

- Engineered and deployed high-performance RTL-based digital circuits, enhancing system efficiency by 15% while accommodating over 50 integrated modules, resulting in a substantial improvement in overall project functionality across multiple product lines.
- Developed and implemented comprehensive UVM-based verification test benches that attained an impressive 98% functional coverage across diverse designs, decreasing post-silicon bug occurrences by around 30%, which significantly elevated product reliability metrics.
- Conducted detailed functional and gate-level simulations to refine debugging processes, achieving a notable reduction of debug time by 20%, thus accelerating project timelines for five key design validations and boosting team productivity by enhancing workflow efficiency.

Skills

Eda tools: Synopsys Design Compiler, Cadence Innovus, Cadence Virtuoso, Xilinx Vivado, Mentor Calibre, QuestaSim, ModelSim.

Verification: UVM, Functional Verification, Gate-Level Simulation (GLS), Assertion-Based Verification (ABV), Testbenches, Code and Functional Coverage Analysis, Formal Verification.

Digital design & rtl development: RTL Design, Low Power Design (Clock Gating, Power Gating, MTCMOS), Logic Synthesis, Static Timing Analysis (STA), DFT (Scan Insertion, ATPG), Equivalence Checking.

Physical design & timing analysis: Floor planning, Placement & Routing (PnR), Clock Tree Synthesis (CTS), IR Drop Analysis, Parasitic Extraction, Power/Timing Closure, DRC/LVS Verification.

Programming languages & scripting: Verilog, System Verilog, VHDL, Python, C, C++, Tcl, Perl, Shell Scripting, MATLAB.

Machine learning for vlsi: PyTorch, TensorFlow, FPGA-based ML Acceleration, HLS Optimization, Systolic Arrays.

Projects

RTL Design, Functional Verification, and Power Optimization for a 32-bit Arithmetic Logic Unit (ALU) **Dec 2024**

- **Engineered** a 32-bit **ALU** at the **RTL** level using **Verilog/System Verilog**, supporting **arithmetic**, **logical**, and **shift operations** with optimized **data path architecture**.
- **Deployed power optimization techniques** such as **Clock Gating**, **Operand Isolation**, and **Memory Splitting**, achieving a 25% reduction in **dynamic power**; verified through **synthesis** and **power analysis** in **Synopsys Design Compiler** and **Power Compiler**.
- Executed **functional verification** with **UVM-based test benches** in **QuestaSim/ModelSim**, ensuring **100% functional** and **code coverage**, followed by **Gate-Level Simulation (GLS)** post-synthesis for **timing** and **power validation**.
- Authored and verified **ALU layout** in **Cadence Virtuoso**, achieving **DRC** and **LVS clean layouts** with **parasitic extraction**; accelerated implementation on **FPGA** using **Xilinx Vivado** with **HLS pragmas** for performance optimization.

Education

Illinois Institute of Technology, Chicago ***May 2025***

Master of Science in Electrical and Computer Engineering (VLSI Design & Microelectronics) GPA: 3.6/4.0

Coursework: Advanced Computer Architecture | Analysis & Design of Integrated Circuits | Digital System-on-Chip Design | RF Integrated Circuit Design | High-Performance VLSI/IC Systems | Hardware/Software Co-Design | Advanced VLSI System Design | Hardware Acceleration for ML