Summary:

Neh Pratikkumar Patel, a Senior Silicon Design Engineer at AMD, is applying for the Senior CPU Microarchitecture & Logic Design Engineer role. He holds an MS in Electrical Engineering and has experience in SOC DFT. His skills include Verilog, SystemVerilog, C/C++, Python, and more. He has worked on projects optimizing an ALU for timing and power, and designing a high-performance cache controller.

Name: Neh Pratikkumar Patel

Email: nehpatel1797@gmail.com

Phone: 4153509081

Location: San Jose, California 95134

Country: USA

Position Category: Design: Logic design

Desired Job Role: Senior CPU Microarchitecture & Logic Design Engineer

University: San Jose State University, Gujarat Technological University

Degree: MS: Electrical Engineering, BE: Electrical Engineering

Graduation Year: 2021

Years Experience: 1

Notable Companies: AMD, Analog Devices

Top Skills: Verilog, SystemVerilog, C/C++, Python, DFT (Scan Chains, BIST, MBIST), DV (Testbenches, Assertions), Static Timing Analysis, Digital Logic Design, Vivado, Icarus Verilog, OpenROAD, Teradyne UltraFLEX, Waveform Tools, CMOS, Low Power Design, JTAG, Computer Architecture

Job Intention: full-time

Visa Status: --

Able: no

Subject: Application for Senior CPU Microarchitecture & Logic Design Engineer

Date Sent: 03-26-2025

Resume: Yes