Summary:

Tapas Sastry is a results-driven electrical engineer with over 7 years of experience in RTL design, integration, and optimizing execution through automation. He has worked at Intel Corporation for 8 years, starting as a Technical Intern and then moving on to become an SoC Design Engineer. He has a B.S. in Electrical Engineering from Portland State University.

Name: Tapas Sastry

Email: tapassas3@gmail.com

Phone: 503-750-0785

Location: Hillsboro, OR

Country: USA

Position Category: Design: Logic design

Desired Job Role: Senior Design Enablement Engineer

University: Portland State University

Degree: B.S. Electrical Engineering

Graduation Year: 2018

Years Experience: 8

Notable Companies: Intel Corporation

Top Skills: RTL Design + Integration, Scripting - Perl / Python / TCL / UNIX, Verilog / SystemVerilog, Tools / Flows / Methodology, Efficient Execution, Synopsys / Cadence Tool Suite, FE to BE Handoff, Gate-level Simulation

Job Intention: full-time

Visa Status: --

Able: yes

Subject: Working at AheadComputing

Date Sent: 02-21-2025

Resume: Yes