Summary:

Rajasekhar Narala is a Design Verification Engineer with over 10 years of experience, particularly in validating high-performance GPUs and accelerators. He is skilled in various technical areas such as UVM, System Verilog, C++, Perl, Python, and TCL. He has worked with notable companies like Intel and AMD.

Name: Rajasekhar Narala

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Phone: 520 906 1774

Location: Folsom CA

Country: USA

Position Category: Verification: Design verification

Desired Job Role: Senior GPU Design Verification Engineer

University: Arizona State University, BITS, Pilani

Degree: Master of Science in Electrical Engineering, BE Electronics and Instrumentation

Graduation Year: 2015, 2013

Years Experience: 10

Notable Companies: Intel, AMD

Top Skills: UVM, System Verilog, C++, Perl, Python, TCL, Git, perforce, JIRA, VCS, Verdi, Jasper Formal, OpenGL, DirectX, CUDA

Job Intention: full-time

Visa Status: --

Able: no

Subject: Logic Design/ Design verification full time opportunities

Date Sent: 02-20-2025

Resume: Yes