Ketan Thakur

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PROFILE

Dedicated and adaptable professional with a proactive attitude and the ability to learn quickly. As averification engineer, I have experience in various aspects of verification, including validation, GLS(Gate-Level Simulation), and formal verification. I possess a strong work ethic and effectivecommunication skills, eager to contribute to a dynamic team and support organizational goals.

EMPLOYMENT HISTORY

Mar 2024 — Present

Formal Verification Engineer, Accenture — Bangalore

Client: Samsung Worked as a Formal Verification Engineer specializing in NVMe memory controllers and validation utilizing JasperGold tool Implemented validation planning from unit takeover to formal sign off.

Implemented assertions, covers, and coverage sign off for complex control path units in FPV. Collaborated closely with designers to identify bugs early in the development cycle through debugging techniques such as waveform viewing or logic analyzers.

Sep 2020 — Feb 2024

Design Verification Engineer, Tech Mahindra — Bangalore

Project Name: Audio IP. Duration: 1 year. Client: Intel Project Description: Creating a verification environment. Writing test cases for I3C protocol verification.

Project Name: PVC, Lunar Lake. Duration: 1.6 years. Client: Intel Project Description: This project involves pre-silicon validation of graphics and throughput computing hardware engineering. Running coverage regression on GT model, reporting the regression result to the client. Fixing the failed tests after the regression. Worked on coverage-related task. Analyzing the regressions, syncing the passing tests in the ATS queue, and generating Excel. Worked on scripting-related task. Running full regression on AXE tool for different projects. Debugging of failing tests using the Verdi tool.

Project Name: CWF. Duration: 1 year. Client: Intel Project Description: Building GLS environment. GLS zero-delay simulation and debug.

EDUCATION

Aug 2019

Master of Science, Chandigarh University — Chandigarh

Aug 2015

Bachelor of Technology, Kurukshetra University — Kurukshetra

SKILLS

- Formal Verification
- Application Specific Integrated Circuits
- SystemVerilog
- Verilog
- Gate Level Simulation

LANGUAGES

English