Juan Luis Magaña Paz

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Summary

Pre silicon verification engineer with 3 years of experience in diverse ASIC verification areas.

Skills

Programming: C, C++, Python, Perl, Bash scripting, GNU Makefile, UVM

HDL: System Verilog, System C

Software: Synopsys, (VCS, Verdi), Cadence (Vmanager), Quartus, Eclipse DVT, Git, Linux, Windows

Experience

PRE SILICON VALIDATION ENGINEER | INTEL | FEB 2022 - NOV 2024 | 2 years 8 months

Memory controller for a new memory hierarchy.

- Helped in triage and debugging: identified RTL bug root causes and coordinated with the design team until close fixes.
- Helped in coverage gaps closure.
- Updated or/and fixed default CRs accesses, did it through RAL.
- Helped in creating and executing test plans from bring-up to coverage closure for different features.
- Ramped up and mentoring interns.

Power Management validation engineer for next generation X86 processor.

- Owned multiple functional and performance features, created and executed test plans from bring-up to coverage closure, **features** listed below:
    - Dynamic Voltage and Frequency Scaling features.
    - Core power management Watchdog error feature, basically triggers errors when power management FSM gets out of idle for long periods of time.
    - Core Idle states.
    - Core demoted idle states for extra power saving and increasing performance.
    - Always running SOC counter and Core counter features which keeps track of the timing as well that keeps synced SOC and core timing for core idle states as well deep sleep and wake up requests.
    - Power state feature which calculate and inform the current power state to core functional features for making information based decisions on which functional flows could run with the purpose of increasing performance as well reducing power losses due to Cdyn.
    - PLL shutoff in idle states to increase performance and power saving.
    - L2 cache features which involve reducing voltage and frequency when the core enters into deeper idle states for power saving but taking care of performance.
    - Core exit from deeper idle state based on the amount of snoops to L2 cache.
- Helped in triage and debugging: identified RTL bug root causes and coordinated with Arch and design team until close fixes.
- Helped in architecting and implementing from scratch a validation environment in SystemVerilog, UVM, C++, SystemC, Python and Perl for the power management unit and later integration into full chip environment.
- Integrated C++/SystemC code to SystemVerilog/UVM environment using DPI interfaces.
- Ported and integrated legacy RTL for SOC counter behavioral model into power management unit and full chip environment as well as made enhancements for better code readability and reusability.
- Owned a behavioral model implemented in C++/SystemC, (for emulation reuse purpose), which I integrated into the unit environment and later into full chip environment also maintained it and did several enhancements to legacy code.

- Gave support to errors or problems related to the systemC Behavioral Model to different teams in the project.
- Created and Implemented new methods for register randomization in the systemC Behavioral Model to replace obsolete old legacy methods.
- Co-owned Fuse Abstraction Layer.
- Fuse Abstraction Layer integration into power management unit and full chip environment
- Owned initial configuration fuses values distribution method.
- Coded scripts for automation of tasks like forcing fuses, run regressions, waive errors, creation of header files etc. using Perl, Python, C++, Bash.
- Coded SVA for assertions and cover properties.
- Integrated and implemented initial core boot flow brings up working closely with the design team.
- Co-owned CRs osxml reading and processing tool to generate header files as well as class definition files for different programming languages used along the project, (c, c++, python, SystemVerilog, verilog), with the purpose of reusability, encapsulation, easily writing and reading data from CRs and code good practices.
- Helped design team in the integration and bring up of a voltage regulator IP.
- Helped design team to find issues on the integration of a new PLL IP.
- Helped design team in the bring up of new voltage and reset signals.
- Ramped up and mentoring interns and new hires.

SENIOR PRE SILICON VALIDATION ENGINEER | NXP | NOV 2024 - Present | 4 months

Power Management IC

- Helped in triage and debugging: identified RTL bug root causes and coordinated with the design team until close fixes.
- Owned features of mixed signal Power Management IC for automotive industry.
- Testbench development.

Education

MECHATRONICS ENGINEER | AUG 2016 - JUL 2021 | TECNM CAMPUS COLIMA

Graduated of mechatronics engineering with specialization in mechatronics systems.

PRE SILICON VERIFICATION DIPLOMA | AUG 2021 - DEC 2021 | ITESO

Pre silicon verification diploma offered by ITESO.

Languages

- Advanced English