Ryan Buchner

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linkedin | personal github | work github

Summary

Results-driven engineer with a strong background in Risc-V, design verification, hardware design, and operating systems. Adept at working on automation and verification tools that help maximize designer efficiency.

Education

Master of Science - Computer Science **Sep 2022 - Dec 2023**
University of California, Davis *GPA: 4.0/4.0*

B.S. - Statistical Data Science, B.S. - Genetics and Genomics, Minor - Computer Science **Sep 2017 - Sept 2021**
University of California, Davis *GPA: 3.99/4.0*

Experience

Aril Inc **June 2021 - Present**
Design Verification Engineer *Los Gatos, CA*

- Led the design verification (DV) team, serving as the primary advocate in discussions with management and logic designers.
- Managed and enhanced a test automation tool allowing simulations to be reproducibly and efficiently run, achieving 99% license usage during Nightly regressions.
- Mentored three recent graduates, offering code reviews, design decision guidance, and engineering expertise.
- Developed a co-simulation tool for debugging FPGA builds on Amazon Web Services (AWS) using Integrated Logic Analyzers (ILAs), achieving over 100x speed improvements compared to the base simulation flow, all without requiring paid licenses.
- Created and maintained a SystemVerilog testbench to produce traces of memory access and registers writes for a RISC-V vector processing unit, allowing for the discovery of hundreds of RTL bugs via co-simulation.
- Implemented UVM test-benches for memory management unit structures (e.g. TLBs), producing stimulus using constraint based randomization to achieve greater than 95% coverage.

Logic Design Engineer

- Optimized RTL logic, achieving a 50% improvement in the timing of the integer unit hardware datapath by profiling to identify the critical path and implementing targeted performance enhancements.
- Engineered novel compression algorithms for storing page attributes in a translation lookaside buffer, achieving a 70% reduction in space per entry.
- Implemented RISC-V bit manipulation extensions (Zba, Zbb, Zbs), enhancing processor instruction efficiency for bitwise operations.

Kernel Software Engineer

- Implemented custom supervisor-binary interface (SBI) boot functions to achieve Linux boot.
- Developed custom extensions for the Linux perf utility, enabling FPGA benchmarking through custom hardware counters.

Quon Lab **August 2020 - July 2021**
Machine Learning Engineer- Computational Biology *Davis, CA*

- Trained a variational autoencoder in PyTorch on biological data with limited sample sizes, identifying a correlation ($R^2 = 0.5$) between transcriptional activity and drug efficacy.
- Designed a dimensionality reduction technique to enhance statistical power when analyzing large-scale genomic data (20-250 samples per trial, with over 5,000 dimensions per sample).

Free and Open Source Contributions

Berkeley RISC-V Spike **April 2022 - Present**
Software Engineer *Berkeley, CA*

- Made over 50 contributions, addressing bug fixes and implementing feature requests, to the RISC-V instruction set simulator.
- Upgraded the codebase to the C++20 standard, leveraging new features to enhance future maintainability and readability.
- Managed and enhanced a testing tool to ensure the quality of new merge requests.

Recent Personal Projects

Risc-V LLVM Optimization **January 2025-Present**

- Wrote LLVM optimization passes to identify loops vectorizable via the RISC-V fault only-first load instruction, enabled a 100x speedup (dependent on the hardware and input data).
- Tree LLVM considers these loops to not be vectorizable due to the lack of clear loop bounds.

Skills

Programming Languages SystemVerilog | C++ | Python | RiscV Assembly | Verilog | Bash | C
Developer Tools/Frameworks UVM | Git | LLVM | Slurm