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EDUCATION

Master's in Electrical & Electronics Engineering (GPA 3.71)
California State University, Sacramento. Sacramento, CA. (2017-2019)

TECHNICAL SKILLS

RTL Logic design & Verification : Verilog, System Verilog,
UVM. Scripting and Software development : Python, Perl, C, LabVIEW.
Tools : DVT,DVE,Verdi,Modelsim,VCS,Conformal,DesignVision,Vivado,Visio,Virtuoso,VCLINT,VCLP,UPF.

WORK EXPERIENCE

- Intel Corporation (Oregon, US)– Design and Verification Engineer. (June'21-Current)

- Pre-Silicon Verification of the IO design (DDRIO, SRAMIO) on test chips used for process learning. (14A, 18A,20A)
- Led the efforts to move from Custom schematic approach to more APR friendly digital on top approach for DDR IP on the test chip.
- Worked on removing the traditional scan chain based IO design with JTAG based IO design and verified the same on a test chip.
- Involved in writing integration level RTL for DDR and creating Behavioral models for custom analog blocks in System Verilog.
- Performing Functional equivalence checks on APR netlists with RTL and running GLS.
- Performing spice simulations for checking the quality of analog BMODs.
- Creating new test cases using SystemVerilog/UVM to formally validate the design.
- Worked on verifying PLL, DLL and PRBS within the IO design.

- Analog Devices (North Carolina, US)– Digital Test Development Engineer. (Transceiver Product Group) (Aug'19-June'21)

- Generating SCAN, Memory Bist and JTAG patterns using Cadence Modus running gate level simulations.
- Developing and debugging functional tests for digital blocks to test mixed signal IC on ATE platforms like National Instruments.
- Developing ARM based test, to populate all the data paths with pseudo random data and do MISR readbacks.
- Working on post silicon bring up and production test program development and debug.

- Analog Devices (North Carolina, US)– Digital Test Development Intern. (TPG) (Sept'18-Dec'18)

- Effectively completed digital characterization for SPI using ATE and bench evaluation. Developed tests using system Verilog and UVM and generated ASCII patterns and tested them using Teradyne Ultraflex.
- Developed a script to automate the whole process of functional pattern generation of SPI read/writes.

- Graduate Teaching Assistant. (California State University, Sacramento). (Jan '19–May'19)
  Assisting the professor for grading assignments in the graduate course of Hierarchical Digital Design methodology.

ACADEMIC PROJECTS

- Design and verification of a FIFO. (UVM & SV)
  Verified a FIFO design to understand the verification environment using UVM. Constrained random tests were developed to improve coverage.
- Design and Verification of PSI protocol. (SV and Python)
  Designed a PSI protocol using Verilog, wherein data packets are taken inside the PSI parallelly from DMA and stored in an asynchronous FIFO. (Gray coding was used). Each packet is appended with a Head of frame and End of frame delimiter and sent out serially. The design was verified using Verilog and Synthesized using Synopsys tools. Python was used to generate input data and expected output.
- Designed an Arcade game on Nexys 4 DDR Artix – 7 FPGA Dev board. (Verilog)

  Designed an Arcade game with VGA controller as an output and push buttons as the game controller. Developed an overlay algorithm to display multiple moving objects using multiple buffers. Implemented a two-level game with moving objects and multiple screens. Used Verilog HDL and Xilinx Vivado design suite.
- Transistor level designing of ALU using Cadence Virtuoso. (180 nm Technology)
  Designed schematic and layout of an ALU which can perform the following operations: Addition, Subtraction, Division, Multiplication and Shifting. Performed DRC and LVS of the layouts.

RESEARCH AND TRAINING

- Research paper titled 'Design and Implementation of VGA controller using FPGA' is published in 'VSRD International journal of Electrical, Electronics and Communications Engineering, Vol 5 issue August 2016'
- German language speaking course 'Level A1 & A2' from Goethe institute Max Mueller bhavan, Mumbai.

ACADEMIC COURSES: Micro Computer System Design, Hierarchical Digital Design Methodology, Digital Integrated Circuit Design, Advanced Static Timing Analysis, Advanced Semiconductor Devices, Analog & Mixed signal IC design, Advanced Analog & Mixed signal IC design, Machine Vision.