SRIRAM N

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PROFESSIONAL SUMMARY

Electrical Engineer with a passion bridging between bits and electrons, specializing in digital design, FPGA, semiconductors, and machine learning. Skilled in **RTL-to-GDSII**, **Formal verification**, and **Embedded programming** with a niche focus on where hardware meets AI.

EDUCATION

University of Texas - Dallas **August 2022 - May 2024**
Master's, Electrical Engineering *GPA: 3.4*

Osmania University **July 2017 - August 2021**
Bachelor's, Electrical Engineering *GPA: 3.2*

COURSEORK

Advanced Digital Logic, ASIC Design, Embedded systems, Wireless Sensors and Networks, Computer Architecture

PROFESSIONAL EXPERIENCE

holiday channel **Remote**
Machine learning engineer *August 2024 - Present*

- Prototyped an chatbot to recommend recipes by fine tuning bert.
- Containerized the development environment with Docker and Linux(Ubuntu), enhancing portability and reproducibility.
- Set up a github based continuous integration pipeline that streamlined processes and improved productivity by 30%.

PROJECTS & OUTSIDE EXPERIENCE

MSDAP PROCESSOR(RTL2GDS) *January 2024 - May 2024*
Worked on MSDAP for PNR implementation in 7nm

- Design, Verification and implementing micro-architecture and RTL for a Mini Stereo Digital Audio Processor (MSDAP).
- Orchestrated the final chip’s logic synthesis, Floor planning, Place and route via Cadence Genus and Innovus.
- Static Timing analysis and floorplan to design chip with minimal area, power, slack and high performance (PPA).

Protocol Programming Using MSP432P401R and Adafruit PCF8523 RTC | Embedded C *August 2023 - August 2023*

- Engineered and optimized SPI, I2C, and UART communication protocols on MSP432 microcontrollers, incorporating
- Implemented interrupt-driven strategies, fine-tuned baud rates, and optimized data buffering for enhanced performance and reliable data exchange in embedded systems

ASIC Flow automation and DFT *June 2024 - August 2024*

- Automated the synthesis and timing flow using Makefile and python
- Performed DFT, Automatic Test Pattern Generation (ATPG), Scan Test, number of stuck at faults, fault coverage.

SerDes(RTL implementation) *October 2024 - November 2023*

- Developed and implemented SerDes system with 8b/10b encoding, optimizing high-speed data transmission and reliability.
- Designed efficient Serializer and Deserializer modules, integrating parallel-serial data conversion while ensuring data integrity.

Formal Verification *October 2024 - October 2024*
Formal verification(Yosys - open source synthesis)

- Formally verified ALU, MUX, DFF, Counter, Busy Counter and lfsr for functional correctness with SymbiYosys.
- Performed Logic equivalence check to ensure functional correctness of ALU Design pre and post synthesis.
- Executed mutation coverage analysis to assess testbench effectiveness and identify coverage gaps.

SKILLS

Skills: C/C++, NumPy, Python, MATLAB, Tensorflow, Keras, Pytorch, Computer Networking, Git, Bash, cross-functionally