BINSY RAJENDRAN

Hillsboro,Oregon | Contact : (971)-407-7088 | binsyrajendran@gmail.com|
LinkedIn: www.linkedin.com/in/binsy2911

OBJECTIVE

Seeking an internship or PT/FT/Contract position as an RTL/IP/SoC Design or verification Engineer, leveraging expertise in low-power digital design, physical design and semiconductor technology starting June 2025.

EDUCATION

Masters of Science in Electrical & Computer Engineering September 2023 - June 2025
Portland State University, Portland **CGPA 3.71**

Courses : VLSI Computer Aided Design , ASIC Modelling and Synthesis, Physical Design of Digital ICs, Digital Integrated Circuits, Microprocessor System Design, SOC design with Programmable Logic.

Bachelors of Technology in Electronics and Communication Engineering
Kannur University**,** Kerala, India

- Graduated with distinction,demonstrating strong proficiency in Digital and Analog VLSI Design.

SKILLS

Languages: Python, C, SQL, TCL, SystemVerilog,MATLAB, RISC V

Technologies: Git,Cadence Virtuoso, LTSpice, Synopsys Design Compiler, ICC2,PrimeTime,Cadence Genus,Innovus,Conformal, Xilinx Vivado, Catapult Studio,Questa Sim

VLSI : Low Power Design, Physical Design, RTL design and verification, DFT, Digital Integrated Circuit design with circuit simulation, Static Timing Analysis, CMOS logic circuits, Standard cell circuit design

TECHNICAL PROJECTS

Implementation of Maze Navigation game using VGA : Integrated a Wishbone-interfaced VGA peripheral into the RVfpga-EL2 SoC including video animation along with number-to-pixel generation logic and multiple controller interfaces .

Design and Simulation of Last level cache with MESI protocol : Designed, debugged and verified a last level cache in a shared memory configuration.

PowerGrid Creation and EMIR drop analysis : Created different types of power grid patterns and conducted ElectroMigration and Voltage drop analysis using icc2 in ORCA_TOP design floor plan.

Low Power Design with UPF : Designed RTL with power management techniques such as level-shifters, isolation cells, and retention cells to optimize energy efficiency.

APB Interface Based Memory Controller : Implemented a Microcontroller for managing read and write operations to two memory arrays with APB3 protocol specification.

K-L Partitioning Algorithm : Developed and verified an algorithm for circuit partitioning to optimize interconnect delays and area.

MOSFET Characterization : Conducted behavior analysis of Drain voltage and current in subthreshold region of MOSFETs.

EXPERIENCE

Graduate Engineering Intern at **Indian Space Research Organisation** | India April 2016 – March 2017

- Implemented circuit level power optimizations and RTL design for digital signal processing applications.
- Performed data analysis and executed vibration testing of launch vehicles to ensure structural integrity and mission readiness.
- Worked on noise detection and correction of the power amplifier module.

Assistant Lecturer at **Universal Group of Institutions** | India August 2014 –January 2016

- Delivered lectures and guided labs in Digital Circuits, Microprocessor Design, and VLSI Fundamentals, ensuring strong foundational understanding for undergraduate students.