MALLIKARJUN KASHA

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OBJECTIVE

Looking for Full Time opportunity in the field of VLSI as an RTL/ASIC Design, Verification or Validation Engineer.

TECHNICAL SKILLS

Programming Languages: Verilog, System Verilog, Linux, C, C++, SQL, Python, Assembly language.
Skills: ASIC Design, Pre-Silicon Validation, FPGA Design, Computer architecture, VLSI, Digital Logic Design, RTL Design, CPU verification, Assertions, Code/Functional Coverages.
Concepts: UVM, Object Oriented Programming (OOP), FSM, DDR4, Clock Domain Crossing, Low Power Design, Formal Verification, DRAM design, Cache replacement policies.
Tools/Software's: Cadence Virtuoso, Mentor Graphics (Questa-sim), ModelSim, Synopsys VCF, Vivado, Cathode Ray Oscilloscope, Signal generator, PCBA, multimeter, source meter.
Computer Architecture: MIPS, Virtual Memory & Paging, Pipelining & Scheduling, Automation, 8086 Microprocessor.
Protocols: APB, AHB, MESI, UART, I2C, Cache protocol.

EDUCATION

Master of Science - Electrical and Computer Engineering (Jan 2023 – March 2025) **GPA: 3.83/4.00**
Portland State University, Portland, OR, USA.

COURSE WORK

Graduate Courses: Digital Integrated Circuits Design, Microprocessor System Design, Computer Architecture, Formal Verification, System Verilog, Advanced Computer Architecture, Pre-Silicon Validation, Very Large-Scale Integration (VLSI), Electrical Devices and Circuits, Digital systems, circuit design.

Bachelor of Technology – Electronics and Communication Engineering (April 2016 - May 2019) **GPA: 8.0/10.0**
VNR Vignana Jyothi Institute of Engineering and Technology, Hyderabad, India

TECHNICAL PROJECTS

System Verilog Design and Verification of an I2C based memory subsystem:

- Worked in a team of 4 to design an I2C interface with an FSM for data streaming via SDA and SCL lines, including ACK signal handling.
- Responsible for addresses and memory interface/controller, converting SDA data into memory addresses, and integrating an FSM and ALU for efficient storage and retrieval.

System Verilog Simulation of Single Level L-1 split Cache:

- Worked in a team of 2 people to simulate a single-level L1 split cache for a 32-processor system with shared memory, using the MESI protocol for cache coherence.
- Prepared trace files and collected statistics on cache misses, hits, reads, writes, and hit ratio.

UVM based Design and verification of FIFO Circular Buffer:

- Created a UVM verification plan with components like Driver, Monitor, Agent, Sequence, Sequencer and Scoreboard with the help of my friend.
- Utilized System Verilog assertions and cover groups for validation and functional coverage.
- Developed constrained-random and directed tests, achieving 100% code and functional coverage.

Python Simulation of 5-stage Pipeline MIPS Lite Architecture:

- Led a team of four to simulate a 5-stage Pipeline MIPS Lite Architecture under two configurations: one with forwarding and one without.
- Utilized already prepared memory trace files to evaluate the architecture's functionality and performance. The results were compared to assess the impact of forwarding on system speed and efficiency**.**

PROFESSIONAL EXPERIENCE

Design Verification Apprentice, Maven Silicon, India (Jan 2022-Dec 2022)

- Verified a 16-bit RISC Processor using System Verilog(RTL Design) and UVM, ensuring functionality, performance, and compliance with design specifications.
- Developed a UVM-based testbench including monitor, agent, driver, scoreboard, and functional coverage model.
- Implemented System Verilog Assertions and random stimulus generation, achieving high functional coverage through simulations and we have achieved 98% functional coverage with efficient coverage plan by generating random stimulus.

Assistant System Engineer, Tata Consultancy Services, India (June 2019-Jan 2022)

- Worked as a Talend Developer for Walgreens client using Talend open studio, SQL, Java, Linux, GIT and MANGO db.
- Worked as an Orchestration Talend Developer and support role for British American Tobacco client using Talend open studio, SQL Server, ServiceNow, SQL, Python, Java and C.

HONORS AND ACTIVITIES

- I was the captain of my team and led them to win first place in the inter-college cricket tournament.