Harshith Reddy Surakanti

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INDUSTRY EXPERIENCE

Integrated Test Range, DRDO — **Balasore, India**
Hardware Design Engineer — 12/2019 – 11/2022

- Designed and verified RTL/IP modules with a focus on FPGAs and SoCs, integrating IPs and hardware accelerators with Python running on embedded ARM cores with interfacing DMA and DDR4 memory through AXI4 bus, achieving a 40% reduction in latency.
- Automated FPGA workflows, EDA tool automation using TCL scripts and python for front-end and back-end flows. Performed linting, STA, PnR, CDC and Routing checks.
- Validating IO interfaces and signal integrity debugging and Testing using Oscilloscope/ logic analyzer.

NTT Data GDS — **Bangalore, India**
Senior Software Development Engineer — 06/2019 – 12/2019

- Revamped data extraction ETL scripts from SQL Server, increasing data integration efficiency by 20%. Worked with ETL scripting pipelines involving SQL and Python in Windows environments using PowerShell for automation and task scheduling.
- Designed, implemented, and maintained high-performance ETL workflows to ensure efficient data handling, robust data integrity and data process automation across multiple sources.

EDUCATION

Purdue University Indianapolis — **Indianapolis, IN**
MS in Electrical and Computer Engineering (VLSI) — Graduation Date: 12/2024

Coursework: SoC Design, MOS VLSI Design, ASIC Design Laboratory, Computer Architecture, Energy Conversion, Communication systems, Semiconductor TCAD (SILVACO).

ENGINEERING & DESIGN EXPERIENCE

SoC Custom IP Design and Hardware Acceleration | Verilog, Python, IP design & Integration

- Developed custom image processing IPs using Verilog and accelerated visual datasets MNIST, CIFAR and Lite-YOLO by offloading compute to PYNQ SoC with integration over AXI4 and DMA engines.
- Implemented modules for live edge detection using Sobel, moving object tracker, Image resizer overlay, and dynamic block motion were integrated through static IP connected Jupyter Notebook using python.
- Creating reconfigurable logic with DPR technique and Automation through TCL commands.

MIPS Pipelined Processor with RAW hazard Resolution | ASIC Physical Design, Openlane

- Developed a 5-stage 32-bitpipelined MIPS processor in Verilog HDL. Implemented instruction-level parallelism and Integrated forwarding unit for resolving RAW data hazards.
- A custom DRC rule deck built using TCL and Linting using Verilator, Yosys synthesis, openSTA, TritonCTS,openROAD for Floorplanning, Placement, Routing, Signoff,GDSII file generated for Tapeout.

32-bit RISC-V processor with RV32I instruction set | Computer Architecture, RISC-V, Cadence

- Performed physical design of a 32-bit RV32I processor targeting 1.2 GHz at 14nm using Cadence tools.
- Verified RTL functionality with Xcelium, synthesis using Genus with DFT scan chain and floorplanning, power grid generation, CTS, routing using Innovus. Conducted STA, DRC/LVS and IR-drop analysis
- Achieved <5% skew, ~70% area utilization, and no signoff violations, generating tapeout-ready GDSII.

FinFET Process and Device Simulation using Silvaco TCAD

- Modeled advanced FinFET fabrication flow using Silvaco Victory Process and Device (2D_XZ, 2D_YZ, and 3D simulations). Simulation of lithography, etch, regrowth, annealing, and S/D epitaxy processes.
- Tuned lithography bias to optimize mask alignment, impact of lateral etch variations on junction formation and device control. Replaced high-k nitride spacers with low-k PSG+nitride stacks to reduce gate-to-S/D parasitic capacitance in 3D simulations., calibration of anneal time vs effective Junction length.

Karatsuba Multiplier | Github

- Designed a 8x8 Karatsuba multiplier with True Single-Phase Clock (TSPC) logic in Cadence Virtuoso 45nm technology. Layout, DRC, LVS and Static Timing Analysis using NanoTime were performed.
- Documented the performance metrics with power dissipation of 242.556 uW and propagation delay of 796.886 pSec at 1GHz. Used 4486 transistors (1733 PMOS and 2752NMOS) resulting compact Layout.

8-Bit Manchester Adder | Github

- Implemented an 8-bit Manchester adder with pass transistor logic achieving significant improvements in propagation delay of 411.099 pSec and a power dissipation of 17.591 µW.
- Focused on a minimalist approach, using only 208 transistors (26 per 1-bit adder) to lower Area and Power Consumption. STA, AC/DC/Trans analysis, Monte-Carlo simulation for Post Layout were performed.

SKILL SET

- **Technical Skills:** Verilog, SystemVerilog, Lint, VHDL, Linux, CUDA, TCL, Git, MATLAB, Python, C, SQL.
- **Script Languages:** Python, TCL, Bash(Ubuntu), PowerShell, JavaScript
- **Design Skills**: Cadence tools – Xcelium, Genus, Innovus, Modus DFT, Virtuoso; OpenLane, Altium PCB Design, Xilinx ISE, Modelsim, Simulink and SILVACO TCAD.
- **Protocols:** I2C, SPI, AXI4, UART, USB and Ethernet.