Harshith Reddy Surakanti

Dublin, CA | harshith.surakanti@gmail.com | https://www.linkedin.com/in/harshith7/ | https://github.com/HarshithR7

SUMMARY

- Hardware Design Engineer with 3+ years' experience in the industry with Proficiency in Verilog, and SystemVerilog for digital design and verification, with expertise in RTL/IP, subsystem design and integration.
- Skillful in TCL automation and Python for SoC development. I have worked with Xilinx Zynq-7000 and MIPS, RISC-V, FPGA/SoC architectures and multiple on-chip and inter-chip serial communication protocols.

EDUCATION

Purdue University Indianapolis — **Indianapolis, IN**
MS in Electrical and Computer Engineering (VLSI) — Graduation Date: 12/2024
Coursework: SoC Design, MOS VLSI Design, ASIC Design Laboratory, Computer Architecture, Energy Conversion, Communication systems, Semiconductor TCAD (SILVACO).

WORK EXPERIENCE

Integrated Test Range, DRDO — **Balasore, India**
Hardware Design Engineer — 12/2019 – 11/2022

- Designed and verified RTL/IP modules with a focus on FPGAs and SoCs, integrating IPs and hardware accelerators with Python running on embedded ARM cores, achieving a 40% reduction in latency.
- Automated FPGA workflows using TCL scripts, with good experience in both front-end and back-end tools. Performed linting, applied low-power design techniques, and STA, PnR, CDC and Routing checks.
- Successfully completed 3 tape-outs.Debugging and Testing using Oscilloscope/ logic analyzer.

NTT Data GDS — **Bangalore, India**
Senior Software Development Engineer — 06/2019 – 12/2019

- Revamped data extraction ETL scripts from SQL Server, increasing data integration efficiency by 20%.
- Designed, implemented, and maintained high-performance ETL workflows to ensure efficient data handling, robust data integrity and data process automation across multiple sources.

PROJECTS

SoC Custom IP Design and Hardware Acceleration | Verilog, Python, IP design & Integration

- Developed custom IPs for Image filters, Image Resizing, Morphological operations and dynamic visual systems like moving block over background image.
- Accessing Hardware designs through Jupyter Notebook using python. Training visual datasets (MNIST, CIFAR) using ARM9 processing system speeding up the data processing 4x faster than software design.

Dynamic Partial Reconfiguration of Image Filters on Pynq SoC Board | DPR, DSP filters, TCL

- Implemented Sobel, Sharpen, and Blur image filters on Pynq SoC using Verilog for PL and python for PS, creating reconfigurable logic with DPR technique.
- Automated the configuration process with TCL commands. Used python to enable seamless switching between filter configurations improving efficiency and studied bitstream manipulation techniques.

MIPS Pipelined Processor with RAW hazard Resolution | ASIC Physical Design, Openlane

- Developed a 5-stage 32-bitpipelined MIPS processor in Verilog HDL. Implemented instruction-level parallelism and Integrated forwarding unit for resolving RAW data hazards.
- A custom DRC rule deck built using TCL and Linting using Verilator, Yosys synthesis, openSTA, TritonCTS,openROAD for Floorplanning, Placement, Routing, Signoff,GDSII file generated for Tapeout.

32-bit RISC-V processor with RV32I instruction set | Computer Architecture, RISC-V, Cadence

- Performed physical design of a 32-bit RV32I processor targeting 1.2 GHz at 14nm using Cadence tools.
- Verified RTL functionality with Xcelium, synthesis using Genus with DFT scan chain and floorplanning, power grid generation, CTS, routing using Innovus. Conducted STA, DRC/LVS and IR-drop analysis
- Achieved <5% skew, ~70% area utilization, and no signoff violations, generating tapeout-ready GDSII.

SKILLS SET

- **Technical Skills:** Verilog, SystemVerilog, Lint, VHDL, CUDA, TCL, Git, MATLAB, Python, C, SQL.
- **Design Skills**: Cadence tools (RTL2GDSII), genus, OrCAD, Allegro, virtuoso, Innovus, Altium, Xilinx ISE, Modelsim, Simulink and TCAD.
- **Protocols:** I2C, SPI, AXI4, UART, Ethernet.