Hi there,

Hope you are doing well. I learnt about your company from various media and following Debbi's departure from Intel.

I work in the Atom core (E-core) PnP validation team. It is a post-silicon team for power management validation and performance estimation. However, I worked previously in a pre-silicon team, and I often utilize my pre-silicon expertise to reproduce post-silicon failure in the Emulation and pre-silicon domain and debug it in waveform or using trackers.

My academicwork is in computer architecture for power and performance efficiency, where I implemented instruction profiling-based throttling in RISC-V BOOMv2 processor in RTL level.

I started working for Intel as a PhD intern in 2015 and received a full-time job in 2018 in grade 6 when I was still working full-time for my PhD (in All But Defense stage). I got promoted to grade 7 in 2022, and I also receivedmy PhD in the same year.

I believe my full potential lies within computer architecture, and I want to work as a pipeline designer in front-end, preferably in fetch decode or in ARR. I found there are a few openings in those areas, but it seems it requires a few years of experience. I do have experience in validation and in RTL debug, but I do not have experience as a designer. Still, I am passionate about the following roles and wanted to check if you find me a good fit and are interested in evaluating me. My resume is attached for your kind consideration.

Lead CPU Microarchitecture, Fetch Decode | AheadComputing

Senior CPU Microarchitecture ... (Item) | AheadComputing

Thanks,

-owahid