Hi,

I came across your startup on Google News and was impressed by your innovative venture.

As someone passionate about developing novel microarchitecture and RTL design, I'm excited about the possibilities offered by RISC-V. Its flexibility aligns with my interests in instruction fetch, prefetch, branch prediction, and cache design.

In my personal time, I've explored general-purpose CPU microarchitecture projects, focusing on enhancements such as:

Re-orchestrating branch prediction for improved instruction prefetch

Instruction fetch region prediction for block prefetching

Filtering mechanisms to optimize correct path prefetch bandwidth

Pathmarking branches for timely and accurate prefetches

Hot set predictions to enhance cache capacities using victim caches

Event/token/queue-based sequencing of execution from fetch to retire as a better alternative to complex fixed pipeline based superscalar o-o-o executions.

In the past, these kinds of ideas weren't considered necessary for industry projects due to the dominance of Intel, AMD, and ARM in the CPU space, and they didn't have to do anything disruptive to maintain the market share.

However, RISC-V offers the startup level innovatorsa unique opportunity for innovation and disruption.

Currently, I work in the industry on non-CPU compute design, but I'm eager to continue exploring CPU-related projects in my personal time. I'd appreciate the chance to discuss collaboration opportunities with your startup.

If there's interest, I'd be excited to contribute to microarchitecture development during the pathfinding stage. I've attached my resume for reference.

Thank you.

Best regards,

Johnsy Kanjirapallil John

Phone: 201-532-0032