Martin Roberto Linares Altamirano
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WORK EXPERIENCE

- Sr. Verification/SoC Engineer – Synopsys
  12/2022 – ongoing
  Perform Pre-Si SoC verification using UVM based testbenches, doing TB development, VIP integration, coverage and test cases creation and supported regression management and infrastructure. Support RTL integration and stitching as well as IP configuration and integration for ASIC and FPGA on emulation/prototyping platforms.

- *Software Developer* – Intel Guadalajara Design Center.
  12/2020 – ongoing
  Developed and supported software and hardware modules, transactors, that implemented several communication protocols and debug interfaces used in emulation environments to test IPs and SoCs during Pre-Si verification phases of CPUs and chipsets.

- *FPGA Intern* – Intel Guadalajara Design Center.
  05/2018 – 11/2020
  Developed verification and test environments for FPGAs designs using mostly UVM. Automated building and execution of tests. Designed digital modules for an FPGA implementation on server boards.

EDUCATION HISTORY

- *ITESO* – Instituto Tecnológico de Estudios Superiores de Occidente
  Master's Degree: Electronic Design – Aug/2020 – Ongoing

- *ITESO* – Instituto Tecnológico de Estudios Superiores de Occidente
  Bachelor's Degree: Electronics Engineering – Aug/2015 – Dec/2019

- *CETI* – Centro de Enseñanza Técnica Industrial
  Associate's Degree: Automation and Instrumentation Technologist – Aug/2011 – Jun/2015

SKILL SET:

- Hardware: FPGA Design, testbench development with UVM, RTL design.
- Tools: VCS, Verdi, Protocompiler, Virtualizer, QuestaSim, Quartus, Git, scripting.
- *Software:* C/C++, SystemC, Python and Java. Embedded Software. Linux

EXTRA INFO:

- *Languages:*
  Spanish – Native.
  English – Fluent, native like.