RAJASEKHAR NARALA

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SUMMARY

- Design Verification Engineer with 10+ years of experience validating high-performance GPUs and accelerators.
- Skilled in developing testbenches using UVM and System Verilog.
- Expert in verifying GPU features such as shader subsystems, rendering pipelines, compute units, and graphics APIs.

TECHNICAL SKILLS

Verification Methodologies	UVM, System Verilog and Verilog HDL
Programming Languages	C++, Perl, Python and TCL
Version Control & Collaboration	Git, perforce, JIRA
Simulation and Debug Tools	VCS, Verdi and Jasper Formal
Graphics API	OpenGL, DirectX, CUDA

PROFESSIONAL EXPERIENCE

Staff GPU Design Verification Engineer ***Intel, Folsom CA*** *Nov 2021 – Present*

Shader (GPU/ML Core) Subsystem

- Led design verification for a sub-system involving SIMD dispatch and instruction execution in the GPU pipeline.
- Co-owned testbench migration to UVM, enhancing configurations and setting up automated regressions.
- Collaborated with hardware architects to define verification plans and coverage strategies for new features.
- Served as the primary contact for GPU core simulation triages and post-silicon bug reproduction.
- Partnered with the PPA team to improve the testbench for power and performance micro tests.
- Developed end-to-end checks on silicon performance events to identify functional, and connectivity issues.

MTS GPU Verification Engineer ***AMD, Orlando FL*** *Jan 2020- Oct 2021*

Performance analysis via HW EMU

- Identified key game frames and executed them in hardware emulation (HW EMU) to resolve functional and performance issues, ensuring successful left shift validation.
- Assisted in running compute workloads across the graphics core and generated perf data for the MI200 Platform.
- Captured perf data and debugged firmware Ucode to ensure next gen graphics command processor adopted RISCV.

Design Verification of Geometry Sub-system (RDNA3)

- Developed test content (C++ based) to verify new features, including test plan development and coverage analysis.
- Updated fixed-function shader test suites to align with the next-gen ISA for testing the new geometry pipeline.

Senior GPU Design Verification Engineer ***Intel, Folsom CA*** *Jul 2015 – Dec 2019*

RTL Design: Pixel Shader Scheduler

- Co-owned micro-architectural changes to the unit, interface definitions and implementation details in design spec.
- Experience in pipeline design, data synchronization, data path muxing, assertion, and observation architecture.
- Implemented logic solutions to achieve timing convergence by analyzing synthesis reports.
- Developed unit-level clock gating and formally verified it (SEC) through assertions, assumptions, and black-boxing.
- Enhanced clock gating efficiency by creating power states and analyzing power data.
- Collaborated with the physical design team on partition runs, placement, routing congestion, and gate savings.

Design Verification: Pixel Front end sub-system

- Conducted functional verification and debugged failures in the Pixel front end, ensuring specification compliance and resolving critical design issues.
- Created test plans, RTL trackers, C++ checkers, and developed functional coverage from scratch for a new unit.
- Developed Perl subroutines to auto-randomize register programming and generate tests based on changes.
- Boosted compilation and simulation speed by optimizing log dumping and coverage bins.
- Managed weekly regression runs and maintained automation scripts for large-scale testing and logging during runs.

PROJECTS AND ACHEIVEMENTS

- Published a verification methodology at Intel *"Design for Test and Technology Conference" (DTTC)* 2019.
- Contributed to design verification of industry features like Variable rate shading and Variable registers per thread.

EDUCATION

Master of Science in Electrical Engineering *Arizona State University, Tempe* *Aug 2013 – May 2015*

BE Electronics and Instrumentation *BITS, Pilani* *Aug 2009 – May 2013*