SERGE CHRISTIAN IBALA

CONTACT INFORMATION

Address: 283 ICEHOUSE LANE KETCHIKAN AK 99901 USA

Phone: 347-773-9536

E-mail: christian.ibala@gmail.com

EDUCATION

University: University of Limerick, Limerick, Ireland

Degree: Ph.D. in Electrical and Computer Engineering Feb 2014

Thesis: Exploring FPGA Dynamic Reconfiguration for Sound Source Localization and Tracked Algorithms

RESEARCH WORK

CXL/PCIE: Workload distribution from host to endpoints for AI inference computation on FPGA.

- ➤ AI MODELS (Transfomers/CNN/LLM/LMM): Analyzed AI model architectures for optimized inference deployment on hardware platforms (ASIC/FPGA). Application: Video/Text Correlation
 - Papers Published: "Intel AI guided ultrasound homecare and analysis with digitalized images for cyst detections. SPWC 2021"
 - "Data Extraction and Preparation for AI Inference in a Distributed Computation Load Based FPGA Design" MIXDES 2023 (RTL Coding: Floating Points)
- > **DV:** Exploring the Integration of AI with Python based Design Validation flow using PYUVM and Cocotb

PROFESSIONAL EXPERIENCE

Artificial Intelligence Engineer at Alpha Analytic Solution (Dec. 2024 – Present)

- Developing coarse-grained configuration array (CGRA) for acceleration of dense linear algebra applications, such as machine learning, image processing and computer vision for the automotive industry.
- Video and sound processing for entertainment and driving safety.

Hardware Logic Design Engineer, Intel Corporation, Hillsboro, OR (ASIC/FPGA) (Sept. 2020 – Nov 2024)

- **Design/Integration/Validation** of Soft IPs (On-Chip Memory, GIC, USB3.1, SPI, etc.): Conducted design and integration (RTL/Firmware), pre-silicon validation, and performed RTL collateral checks (LINT, CDC, VCS) to ensure quality and functionality. RTL Micro Architecture. **Interface**: **APB, AHB, AXI (DMA)**
- Paper Published: From Documentation to Automatic IPs Generation and Validation (AE2024)

Hardware/Software/Integration Engineer, Intel Corporation, Hillsboro, OR (FPGA) (Sept. 2018 – Sept. 2020)

- **IP Prototyping:** Integrated and validated Audio and Video Systems IPU (Image Processing Unit) for pre-silicon system validation on Tiger Lake Intel Core using HAPS80/FPGA/Virtex Ultrascale XCVU440/Protocompiler.
- CAD tools development and flows research to automatize and accelerate RTL IP implementation and validation.
- Papers Published:
 - > Reducing FPGA prototyping and Debug time to speed up time to market (DTTC 2019)
 - > Improving validation flow to reduce the cost of late bugs discovery (TECHNOVATE 2022)

Research and Development Engineer, RDPHYS, Ashtabula, OH

(Oct. 2014 – Aug. 2018)

- Worked on a low-cost, web-based, real-time tracking application to track vehicles and merchandise concurrently.
 - A web-based interface is used to display tracking data (Position, Route, Speed, Time etc..).
 - o The data were collected via a cellular network and GPS using a ARM processor.

Research Fellow, University of Limerick, Ireland and Mons Belgium

(Jan. 2010 – Sept. 2014)

Our research interests were in object tracking using wideband signals analysis, classification tasks and distributed computing in embedded multi-agent systems.

 Main area of work is on voice recognition algorithms to locate a particular speaker in a restricted area with multiple other speakers.

Product Application Engineer, Xilinx Europe (FPGA)

(Jan. 2003 – Sept. 2009)

- Main expertise hardware validation and synthesis (Netlist, Timing issue, Design Floorplanning)
- Support of Partial Reconfiguration and Multibooting flow (Using ISE/Vivado)

PUBLICATIONS

• Artificial Intelligent (AI) Papers:

- S. C. Ibala, J. G. de la Mora, A. Muralidharan and C. Y. Tan Lee, "Data Extraction and Preparation for AI Inference in a Distributed Computation Load Based FPGA Design," 2023 30th International Conference on Mixed Design of Integrated Circuits and System (MIXDES), Kraków, Poland, 2023, pp. 100-104, doi: 10.23919/MIXDES58562.2023.10203270
- > Satoshi Suzuki, Serge Ibala and al. "Intel AI guided ultrasound homecare and analysis with digitalized images for cyst detections. SPWC 2021

• CAD Tools/Flow (Partial Reconfiguration) Papers:

- > Ibala, Serge Christian, and Chee Yoong Tan Lee. "From Documentation to Automatic IPs Generation and Validation." 2024 International Conference on Applied Electronics (AE). IEEE, 2024.
- > Serge C Ibala, Tan Lee Chee Yoong "Improving validation flow to reduce cost of late bugs discovery "Technovate 2022 Penang Malaysia Nov 15-17
- S. C. Ibala, D. R. Valdes, J. M. Eugenio "Reducing FPGA prototyping and Debug time to speed up time to market," In Proceedings of *Design and Test Technology Conference (DTTC)*, Portland, Oregon, May 2019.

• <u>DSP (Digital Signal Processing) Papers:</u>

- S. C. Ibala, S. Astapov, F. Bettens, C. Valderama, "Combining Multiple Sound Source Localization Hybrid Algorithm and Fuzzy Rule Based Classification for Real-time Speaker Tracking Application," In Proceedings of International of Mathematics and Computer Science, Vol. 4, No. 1, pp. 12-25, 2013.
- F. Escobar, X. Chang, S. C. Ibala, "Fast accurate Hybrid Algorithm for Sound Source Localization in Real-Time," In Proceedings of International Journal of Sensor and Related Networks, Vol. 1, Issue 1, Feb. 2013
- S. C. Ibala, F. Escobar, X. Chang, C. Valderama, "Hybrid Algorithm Computation Methodology to Accelerate Sound Source Localization," In Proceedings of International Journal of Microelectronics and Computer Science, Vol. 3, No. 3, 2012 pp. 99-110. ISBN. 2080-8755
- S. C. Ibala, J. Vachaudez, C. Valderrama, "Novel interface drivers to combine real-time localization and tracking algorithms," *In Proceedings of Applied Electronics*, Czeck Republic, Sept. 2012
- S. C. Ibala, J. Vachaudez. C. Valderrama, "Combining Sound Source Tracking Algorithms Based on Microphone Array to Improve Real-Time Localization," *In Proceedings of MIXDES*, LODZ Poland pp. 24-29, May 2012.

TOOLS

- AI Frameworks: Reviewing TensorFlow, PyTorch, Keras and Hugging Face, LMM, MLLM, LLM
- **Hardware Tools:** AMD/Xilinx Chipscope, Vivado, Intel/Altera Signal TAP, Quartus, SystemVerilog, C/C++, Matlab, Simulink, LabView (FPGA), Modelsim, VCS, Spyglass, Python (FPGA, ASIC)
- Software Tools: Skilled in PYUVM (UVM RTL Validation) JavaScript, HTML, CSS, NodeJS, SQL

LANGUAGE SKILLS

Fluent in English, French and Lingala.

RESEARCH INTERESTS

• Computer Vision and Pattern Recognition Statistics, Machine Learning, Algorithm optimization, Cyber Security, Database, Human Computer Interaction, Internet of Things, Games, Robotics