Joey Rudek (he/they) Email: rudek.joseph@gmail.com

Education

- **University of California, San Diego** — San Diego, CA
  M.S. Computer Science; Advisor: Dean Tullsen; GPA: 3.74 — *Spring 2025*
- **University of Virginia** — Charlottesville, VA
  B.A. Computer Science, Mathematics; Advisor: Ashish Venkat; GPA: 3.86 — *May 2021*

Experience

- **Intel Corporation** — Santa Clara, CA
  Security and Privacy Research Intern — *June 2023 - September 2023*
  - Developed a gem5 implementation of **Cryptographic Capability Computing** (LeMay et al.) as part of the DARPA HARDEN program.
- **Rivos Inc.** — Mountain View, CA
  Software Intern — *June 2022 - September 2022*
  - Developed RISC-V designs for low-overhead hardware-level memory isolation and control flow integrity, then implemented both in the gem5 architectural simulator.

Teaching Experience

- **University of California, San Diego** — San Diego, CA
  Teaching Assistant — *Winter 2023, Fall 2024*
  - Sole TA for graduate **Teaching Methods in Computer Science** (Fall 2024). Responsibilities included all grading in the course, almost all logistics, meeting with students to workshop every in-class presentation, and acting as liaison between the class and the professor through staff meetings.
  - Structured and led weekly discussion sections for undergraduate **Introduction to Computer Architecture** (Winter 2023). Also graded student assignments, held office hours, and participated in weekly staff meetings.
- **University of Virginia** — Charlottesville, VA
  Undergraduate Teaching Assistant — *September 2018 - May 2021*
  - Recipient of the 2021 **Louis T. Rader Undergraduate Teaching Award**.
  - Instructional staff for Computer Architecture (one semester), Theory of Computation (three semesters), and Introduction to Programming (four semesters).

Selected Publications

- **Going Beyond the Limits of SFI: Flexible and Secure Hardware-Assisted In-Process Isolation with HFI** *(ASPLOS 2023)*
  - *S. Narayan, T. Garfinkel, M. Taram,* ***J. Rudek****, D. Moghimi, E. Johnson, C. Fallin, A. Vahldiek-Oberwagner, M. LeMay, R. Sahita, D. Tullsen, D. Stefan*
  - Hardware extension for low-overhead memory safety and Spectre-proofing guarantees in WebAssembly.
- **Regex+: Synthesizing Regular Expressions from Positive Examples.** *(SYNT 2022)*
  - *E. Pertseva, M. Barbone,* ***J. Rudek****, N. Polikarpova*
  - Quick and sound regular expression synthesis from very few positive examples.

Selected Projects

- **Single-Instruction Loop Fuzzer**: An extension of the fadec x86 en/decoder to generate workloads consisting of one instruction repeated many times in a loop, for ISA and hardware exploration.
- **Branch Predictor Framework**: A Python framework for writing and benchmarking different branch predictor models. Includes predictor primitives and some state-of-the-art predictor implementations.
- **BrainFunc**: An optimizing BF interpreter written in Haskell.
- **KelpChip**: A CHIP-8 emulator written in C++ using SFML.

Skills

- **Languages**: C, C++, Python, SQL, Haskell, x86, MIPS32, RISC-V
- **Languages (spoken)**: English, Japanese, Spanish
- **Technologies**: gem5, git, UNIX, Microsoft Office, Google Workspace, LaTeX, Gradescope