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SUMMARY

Pre-Si verification engineer with 15 years of experience. Proficient in leading engineers on all stages of the validation, as well as providing coaching for professional growth. Capable of switching contexts and can work on multiple areas of the project, as well as collaborating across teams to achieve milestones.

EXPERIENCE

Intel Tecnologia de Mexico S.A. de C.V. Zapopan, Jalisco, Mexico
CPU Design Engineering Manager Aug 2023 to date
Leading engineers working on x86 verification at the CPU level and microcode level with contribution on x86 features bring up, test plan, content development, debug and coverage closure; also, verification environment development and maintenance using UVM at CPU level.

Engineering Manager May 2020 to 2023
Continued leading IP integration and verification on new generation of controller for second level memory and got in charge of more engineers. Responsibilities increased to Security IP verification; GLS verification leading (booting and scan); SMBUS verification leading.

Pre-Si Valid/Verif Engineer May 2018 to 2020
Worked on verification of memory controller for second level memory technology with UVM. Led a team of three engineers working on IP integration and verification at unit, cluster and full chip level. IPs were the configuration register access fabric (full chip and cluster); CPU & DMAs (unit level and full chip) and I3C (full chip). Owned integration and support of third party register access fabric and I3C BFMs in all environments needed. Became the point of reference for debug on those areas with strong contribution on the bring up phase.

Graphics Hardware Engineer May 2015 to 2018
Worked on verification of Display IP, initially responsible for shutdown and bring up flows, Cyclic Redundant Check (CRC) verification and support; later Wireless Video verification including unit level test bench created in UVM and messenger unit level verification initially done with a UVM environment and later switched to Formal Property Validation (FPV).

Hardware Engineer May 2010 to 2015
Worked on standardized methodologies that supported common and robust on-die DFx features. Verified DFx logic for High-Speed IO serial interfaces (PCIE express, Serial ATA, USB and MIPI MPHY); used OVM, Saola and UVM at the end. Provided training and support to post-Silicon engineers.

Contractor for Intel Zapopan, Jalisco, Mexico
Hardware Engineer April 2009 to April 2010
My role was to provide support for RTL of embedded RAM memory controller and two functional units in ASIC. I also did functional verification, debug, bug fixing, lint RTL code, synthesis and formal equivalence verification. The verification methodology followed in this project was VMM (Verification Methodology Manual).

EDUCATION

2009 to 2010 Specialty program in Integrated Circuit Design
Instituto Tecnologico y de Estudios Superiores de Occidente
Tlaquepaque, Jalisco, Mexico

2003 to 2008 Bachelor of Electronics and Communication Engineering
Universidad de Guadalajara
Guadalajara, Jalisco, Mexico