

Summary:

Nilesh Suryavanshi is a final-year MS Computer Engineering student at the University of Texas at Dallas with experience in RTL design and verification, CPU microarchitecture, and performance optimization. He has developed a UVM-based testbench to verify RISC-V pipeline stages and has hands-on experience with Verilog/SystemVerilog, Synopsys & Cadence tools, and static timing analysis (STA). He is seeking Internship/Full-Time opportunity in silicon verification, validation, and Design for Testability(DFT).

Name: Nilesh Suryavanshi

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Phone: +1 945-527-4828

Location: Austin, Texas, 78736

Country: USA

Position Category: Design: Logic design, Verification: Design verification

Desired Job Role: Silicon Verification Engineer

University: The University of Texas at Dallas, University Of Mumbai

Degree: Master of Science, Computer Engineering, Bachelor of Engineering, Instrumentation

Graduation Year: 2025

Years Experience: 3

Notable Companies: Bosch, Tata Consultancy Services Limited

Top Skills: Verilog, SystemVerilog, Python, C, C++, UVM, Static Timing Analysis, Synopsys, Cadence

Job Intention: Internship/Full-Time

Visa Status: --

Able: No

Subject: Interested to join Ahead Computing.

Date Sent: 03-18-2025

Resume: Yes