Felipe Muñoz López, PhD

Chip Engineer

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PhD in **Computer Architecture** and **High Performance Computing** with over **5 years of research experience in computer architecture** and **1 year in hardware design**. Currently contributing at INNOVA IRV Microelectronics, focusing on advanced **RISC-V** and **UCIe** System-in-Package (**SiP**) solutions for **real-time**, **ultra-low-power** applications.

WORK EXPERIENCE

Chip Engineer Apr 2024 – Present

INNOVA IRV Microelectronics

- Contribute to the RISCcom poject.
- Leading a team of five engineers.
- Research RISC-V instruction sets, extensions, and **hardware security**.
- Conduct testing and validation to ensure reliability and compliance with industry **standards** and security **certifications**.
- Design custom hardware solutions using **FPGAs**, employing **Verilog** and **VHDL** for **RTL** design.
- Design hardware secured systems for **IoT** and **datacenter** applications.

Research Assistant (FPU fellowship) Dic 2021 – Apr 2024

Dept. of Computer Architecture (University of Málaga)

- Awarded a Spanish Government FPU Research Fellowship.
- Contributed to the CooTSIoT and MArEA projects.
- Proposing improvements at various software levels (programming and runtime models) to improve productivity and **performance/watt** portability, with a focus on ultra-low power architectures (**RISC-V** and **ARM**).
- Contributed to the project by exploring **machine learning** algorithms and **decision trees**, with a focus on improving performance through optimized **memory** usage and algorithmic improvements.
- Leveraging technologies such as **OpenCL 3.0**, Unified Shared Memory (**USM**) from **oneAPI**, and Heterogeneous System Architecture (**HSA**)
- Design and implement kernels for **Altera FPGAs** to accelerate software computational hotspots.
- Worked with the supercomputer **Picasso** (Málaga)

Cloud Migration & Implementation Associate Apr 2021 – Dic 2021

Accenture (Málaga)

Working in the **security**, anti-virus and MDM team. My main objectives were:

- Implement high performance solutions that deliver operational efficiencies.
- Improve performance and meet dynamic business demands.
- Provide detailed assessment of existing solutions and implement new technology leveraging next-gen IT models and agile, scalable architectures.

Research Assistant Dic 2019 – Apr 2021

Dept. of Computer Architecture (University of Málaga)

- Contributed to the ADAHE project..
- Focused on the **architectural** aspect of the project, including **data structure** optimization and **parallel** implementation.

- Designed and implemented **architecture-aware** algorithms and techniques to improve system **performance** and **energy** efficiency.
- Worked with High Bandwidth Memory (**HBM**) to boost performance and improve energy efficiency.
- Worked with the supercomputer **ARCHER II** (Edinburg)

Internship contract Mar 2020 – Jun 2020

Grumpy Cat Software S.L.

- I worked on reducing the size of **time series** data for visualizing and analyzing large datasets generated by Internet-of-Things (IoT) sensors.
- I focused on the Visvalingam-Whyatt algorithm, which is considered the state-of-the-art in this field, and proposed several optimizations and parallel implementations.
- I worked mainly at the architectural level, and I am proficient in **parallel patterns** and parallel_for constructs using Intel **oneTBB**.

CiTIUS Summer Scholarship Jun 2019 – Jul 2019

University of Santiago de Compostela

- Conducted research focused on the efficient obtaining of terrain seed points to determine the Digital Terrain Model in **LiDAR** point clouds.
- Developed a parallel implementation in **CUDA** and **oneAPI**, making use of the latest technology for efficient processing.
- Contributed to the project by designing and implementing optimized solutions for processing large point clouds, optimizing the data structure (octree) used to store the LiDAR point cloud, leading to a remarkable improvement in **memory performance** and significantly reducing processing time.
- Worked with the supercomputer **Finisterrae II** (Galicia)

Department Collaboration Scholarship (MEFP) Sep 2018 – May 2019

Dept. of Computer Architecture (University of Málaga)

- Contributed to the **implementation** CUDA nodes for the **Flow Graph** interface in the Intel **TBB** Library, utilizing OpenCL 2.0 technology.
- Improved the support for heterogeneous architectures in the library by introducing new features from OpenCL 2.0, particularly fine-grained Shared Virtual Memory (**SVM**).
- Demonstrated improved **heterogeneous** execution times by simplifying **cache coherence** management.

EDUCATION

Ph.D in High Performance Computing Oct 2021 – Dec 2024

University of Malaga, Málaga, Spain

Title: "Accelerating Massive Sensor-Based Analytics"
Grade: Cum Laude distinction

Master in High Performance Computing Oct 2019 – Jul 2020

University of Santiago de Compostela, Santiago de Compostela, Spain

GPA: 9,75

Degree in Telecommunications Systems Engineering Oct 2014 – Sep 2019

University of Malaga, Málaga, Spain

GPA: 8,31

PUBLICATIONS

PaFESD: Patterns augmented by Features Epileptic Seizure Detection 2024
IEEE Transactions on Biomedical Engineering, DOI: 10.1109/TBME.2024.3441090
Felipe Muñoz, Angeles Navarro and Rafael Asenjo

CPU and GPU oriented optimizations for LiDAR data processing 2023
Journal of Computational Science, DOI: 10.1016/j.jocs.2024.102317
Felipe Muñoz, Angeles Navarro, J. Carlos Cabaleiro and Rafael Asenjo

COVID-19: Estimation of the transmission dynamics in Spain using stochastic simulator Sep, 2021
Computer Methods and Programs in Biomedicine, DOI: 10.1016/j.cmpb.2021.106399
Marcos Matabuena, Pablo Rodríguez-Mier, Carlos García-Meixide, Victor Leborán

OpenCL 2.0 support for Intel TBB Sep, 2019
Edition of the Conference on Parallelism (JP'19), ISBN 9788409121274, págs. 334-343, Link
Felipe Muñoz, José C. Romero, Alejandro Villegas, Ángeles Navarro, Andrés Rodríguez and Rafael Asenjo

LECTURES

Optimisation of the Visvalingam-Whyatt algorithm to reduce time series in real time Sep 22-24, 2021
XXXI Edition of the Conference on Parallelism (JP'21/22), Málaga
Felipe Muñoz López, Antonio Vilches Reina, Angeles Navarro and Rafael Asenjo

SkyFlow: Heterogeneous Streaming for skyline calculation using FlowGraph & oneAPI Sep 22-24, 2021
XXXI Edition of the Conference on Parallelism (JP'21/22), Málaga
Jose Carlos Romero, Felipe Muñoz, Antonio Vilches, Andres Rodriguez, Angeles Navarro and Rafael Asenjo

oneAPI implementation of the OWM algorithm for DTM seed points detection July 22-27, 2021
Conference on High Performance Computing (CHPC'21)
Felipe Muñoz, Rafael Asenjo, Ángeles Navarro y J. Carlos Cabaleiro

Using Intel oneAPI to improve the productivity of heterogeneous programming Feb 6-7, 2020
XI Winter Seminar CAPAP-H, Universitat Autònoma de Barcelona
Felipe Muñoz, José C. Romero and Rafael Asenjo

PROJECTS

RISCcom Apr 2024 - Present

INNOVA IRV Microelectronics

"Sistema multipropósito seguro de bajo consumo basado en RISC-V para comunicaciones inalámbricas"

CooTSIoT Dic 2022 – Apr 2024
Dept. of Computer Architecture (University of Málaga)

"HW-SW co-design and optimization of Time Series based applications for IoT ultra-low power embedded devices"

MArEA Dic 2021 – Apr 2024
Dept. of Computer Architecture (University of Málaga)

"Programming Models for Analytics Applications in Emerging Architectures"

ADAHE Dic 2019 – Apr 2021
Dept. of Computer Architecture (University of Málaga)

"Accelerating Data Analytics on Energy Efficient Heterogeneous Architectures"

AWARDS & SCHOLARSHIPS

"Formación de Profesorado Universitario" (FPU) grant 2021
Ministerio de Educación y Formación Profesional

Best Master's thesis of the High Performance Computing Master 2021
ETSE University of Santiago de Compostela

Best academic record of the High Performance Computing Master 2021
ETSE University of Santiago de Compostela

HPC-Europa3 Transnational Access programme grant 2020
University of Edinburgh (EPCC) - Rosa Filgueira Vicente (Host)

Best End-of-Study Project Award for the 2018/2019 academic year 2020
ETSIT University of Málaga

Best End-of-Study Project Award for the 2018/2019 academic year 2019
Colegio Oficial de Ingenieros de Telecomunicación AORM

CiTIUS Summer Scholarship 2019
Centro Singular de Investigación en Tecnoloxías Intelixentes (CiTIUS)

Department Collaboration Scholarship 2018
Ministerio de Educación y Formación Profesional (MEFP)

LANGUAGES

Spanish (native)

English (advanced)

HARD SKILLS

Programming: C++, C, System-Verilog, VHDL, RISC-V Assembler, CUDA (C, Python & Fortran), OpenCL, SYCL, Intel oneAPI, MPI, OpenMP, Python (Numba & RAPIDS), R, Matlab/Octave, GIT, Cmake, GDB, LaTeX
OS: Ubuntu, Debian, Kali and other Linux, Windows, FreeRTOS
Miscellaneous: Slurm, Docker, Kubernetes, Intel Parallel Studio, NVIDIA Nsight, BSC Tools (Extrae, Paraver, Dimemas), Visual Studio Code

SOFT SKILLS

Communication, Creativity. Teamwork, Adaptability, Problem-solving, Committed

INTERESTS

Hardware design; Complex Systems; Machine Learning and Artificial Intelligence; Big Data; HPC and HTC; Heterogeneous Computing; Irregular Data Structures; Algorithm Parallelization; Modeling and Simulation of Physical Phenomena; Cybersecurity; Quantum Computing.