Shweta Sarap

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SUMMARY

Enthusiastic and motivated engineer seeking an entry-level role in Formal Verification to develop expertise in applying formal methods for design verification. Passionate about logic, automation, and verification techniques, with a keen interest in learning model checking, theorem proving, and abstraction to ensure system correctness. Eager to work on real-world verification challenges, collaborate with experienced professionals, and continuously expand my knowledge in the field. Adaptable, detail-oriented, and committed to growing as a formal verification engineer.

PROFESSIONAL EXPERIENCE

QA Associate January 2022 – May 2024
TIAA Pune, IN

- Led cross-functional defect triage sessions, identifying and isolating bugs, and assisting developers with root cause analysis.
- Tracked defects using JIRA and ALM, improving defect resolution by 50%.
- Conducted functional, end-to-end, regression, and exploratory testing.
- Integrated automated test cases into Continuous Integration/Continuous Delivery (CI/CD) pipelines with Jenkins and Git, optimizing parallel test execution using Selenium Grid for faster delivery.
- Collaborated with cross-functional teams, ensuring alignment of priorities, knowledge transfer to new team members, and timely delivery of quality products.

Associate Consultant November 2018 – Jan 2022
Atos Syntel Pune, IN

- Developed and executed verification plans to ensure functional correctness of systems.
- Contributed to the analysis and debugging of verification results to identify potential design flaws.
- Utilized Model Checking tools to write System Verilog Assertions (SVAs) for checking the functionality and correctness of designs.
- Wrote modelling code to support formal verification and validate design functionality.
- Established regression methodology and automated reporting for failure and regression statistics.
- Assisted in the development and maintenance of verification scripts
- Applied formal techniques such as Abstractions and Design Reductions
- Worked on standardizing Formal Verification (FV) infrastructure to streamline processes and improve efficiency.
- Created detailed documentation of verification processes, test results, and known issues for future reference.

SKILLS

Application Software – JasperGold FPV App, Coverage App, SEC App, Postman, JIRA, GIT, JENKINS, Selenium
Formal Verification – Counter Abstractions, Preloading (IVAs), Non-deterministic Variables, Jasper Data Scoreboards, Engine Optimizations
Programming Languages –System Verilog Assertions, System Verilog, C/C++, Python Scripting, Java

EDUCATION

Arizona State University Online
Master of Science in Software Engineering GPA: 4/4

University of Pune, IN May 2021
Master of Technology in Computer Engineering GPA: 3.3/4

University of Pune, IN May 2018
Bachelor of Engineering in Computer Engineering GPA: 3.12/4