Gayatri Sridhar

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EDUCATION

University of Southern California, *Los Angeles, California*
Master of Science Electrical Engineering *Aug 2023 - May 2025*
Coursework: Computer Systems Organization, MOS VLSI Circuit Design, VLSI System Design 1, Nanotechnology for Electronics & circuits, VLSI System Design 2, Computing principles for Electrical engineers, Hardware Foundations of ML (GPU/CPU)

IP University, *Delhi, India*
Bachelor of Technology in Electronics & Communications Engineering *Aug 2017 - June 2021*

SKILLS

Tools	Cadence Virtuoso, MentorGraphics ModelSim, Custom Compiler, Vivado, HSPICE, Vivado
HDL/Programming Languages	Verilog, TCL, System Verilog, UVM, Python, SVA, C++, Object Oriented Programming, Pytorch
Additional Skills	RTL Design, ASIC flow, Clock Tree Synthesis, Clock Distribution, CPU, GPU & TPU architectures

EXPERIENCE

AMD, San Jose, CA
Circuit Design Intern (Clock Design Team) *May 2024 - Aug 2024*
- Conducted PVT-based timing analysis for advanced technology nodes, evaluating performance variations under different process, voltage, and temperature conditions
- Performed linear and cut-off current analysis to assess reliability across PVT scenarios
- Automated capacitance calculation post-extraction using Python & Bash scripts, improving efficiency by 30%
- Researched clock architecture in Vivado to understand design trade-offs

Accenture, Delhi, India
Application Development Associate *Aug 2021 - June 2023*
- Automated system monitoring & data validation using Java and SQL reducing manual intervention by 60%
- Developed & maintained detailed technical documentation thereby improving team's efficiency by 40%

PROJECTS

Chip Multiprocessor system based on Cardinal NOC *Aug 2024 - Nov 2024*
VLSI System Design 2
- Designed Processing Element containing CPU & ALU, 4X4 Router, Arbiter & Network interface component using RTL design
- Performed testing and verification using test benches, integrated all components into NOC & ensured each is synthesizable

512-Bit SRAM (6T Cell Design) *Feb 2024 - May 2024*
VLSI System Design 1
- Designed a 512-bit SRAM in Cadence Virtuoso, comprising 4 banks of 128 bits each
- Designed a 6T SRAM cell and peripheral circuits in Virtuoso, ensuring DRC/LVS compliance
- Conducted functional testing of the circuit, ensuring compliance with RSNM & WSNM levels, & verified waveforms
- Final design metrics- Power: 160µW, Area: 966 mm2, read delay:2.5ns and write delay: 2.08ns

MIPS 5-Stage Pipelined CPU *Aug 2023 - Nov 2023*
Computer Systems Organization
- Developed a MIPS 5-stage late branch pipeline CPU in Verilog and verified functionality in ModelSim
- Implemented a Hazard Detection Unit to resolve Read-After-Write dependencies and improve pipeline efficiency

Basic FIFO Design *Aug 2023 - Sep 2023*
Computer Systems Organization
- Programmed a Single Clock 8 locations FIFO with Read and Write pointers using RTL coding in Verilog for buffer management
- Verified FIFO functionality using RTL simulations, ensuring correct EMPTY/FULL flag behavior

Full Custom Arbiter Design Aug 2023 - Nov 2023
MOS VLSI Circuit Design
- Created schematic and layout for a Multiplier, Divider, and Arbiter in Virtuoso for resource optimization
- Accomplished clean DRC & LVS checks and obtained the following results- Area: 2001 µm2, freq: 700MHz & power: 140µW

ONLINE TRAININGS

VLSI Design Flow: RTL to GDS *Nov 2024 - Dec 2024*
HDL Fundamentals for Digital Design, Verification, FPGA Prototyping, Test Bench and STA *Nov 2023 - Dec 2023*