ADWAIT JOSHI

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OBJECTIVE

A Master's student in Computer Engineering at North Carolina State University, seeking internship opportunities for Summer 2025 in Modeling, RTL Design, and Verification for CPU, GPU, SoC, and IP domains. Eager to apply my technical expertise and collaborate on cutting-edge projects that drive innovation and performance improvements.

EDUCATION

Master of Science in Computer Engineering **Aug 2024 - May 2026 (Expected)**
North Carolina State University *GPA: 3.88/4*
Coursework: ASIC Verification, ASIC & FPGA Design using Verilog, Microprocessor Architecture, Architecture of Parallel Computers, Advanced Microarchitecture

Bachelor of Engineering in Electronics and Telecommunication **Aug 2019 - Jun 2023**
Xavier Institute of Engineering *GPA: 9.44/10*

SKILLS

Programming Languages: C++, Verilog, SystemVerilog (basic)
RTL Design: Static Timing Analysis, Clock Domain Crossing
Computer Architecture: Cache, Pipeline Hazards, Out of Order Execution, Coherence vs Consistency

PROJECTS

Scaled Dot Product Attention Mechanism for Transformer Model **Verilog, Modelsim**
- Designed the Scaled Dot Product Attention mechanism of the Transformer Model, optimizing matrix multiplications for Query, Key, Value projections, calculating Score and Attention with SRAM interfaces for data handling
- Achieved a processing cycle count of 3150 at a clock period of 10ns with a performance/area metric of $3.73\times10^{-9}ns^{-2}.\mu m^{-2}$ and an area usage of 8506 μm^2

I2C Master Bridge (I2CMB) Functional Verification **SystemVerilog, Questasim**
- Wrote an I2C Slave interface with tasks for capturing transfers, providing read data, and monitoring bus activity, then connected it to an I2C Master Bridge with Wishbone interface and verified bidirectional data transfers
- Currently devising a layered testbench for I2CMB verification, implementing structured verification components such as drivers, monitors, and scoreboards to enhance test automation and functional coverage.

Performance Modeling of Out of Order Superscalar Microprocessor **C++**
- Built a nine stage superscalar microprocessor simulator with configurable ROB size, RS capacity, RMT, and execution width, incorporating cycle tracking to accurately calculate IPC for various execution widths
- Evaluated the impact of RS and ROB sizes on IPC for gcc and perl traces, determining the minimum RS size that achieves within 5% of peak IPC (using RS size = 256) for each execution width (1, 2, 4, 8)

Cache Memory Hierarchy & Coherence Simulators **C++**
- Developed a flexible cache hierarchy simulator for a single core with L1+L2+Prefetcher configurations and LRU and WBWA policies, analyzing Miss Rate and calculating AAT utilizing CACTII data
- Implemented MESI and MOESI coherence protocols for a 4 core system with processor side and bus side finite state machines, tracking Memory Writebacks, Invalidations, Flushes, and Execution time

Branch Prediction Simulator **C++**
- Implemented bimodal, g-share, and hybrid predictors with 2-bit counters, global history indexing, and a chooser table for dynamic selection
- Analyzed misprediction rates across predictor configurations, showing g-share reduces misprediction to 6.37% compared to bimodal's 11.17% while the hybrid predictor further improves accuracy through dynamic selection

EXPERIENCE

Assistant Manager **Oct 2023 - Jul 2024**
Jio Platforms Limited *Navi Mumbai, India*
- Validated Jio Bharat Phones and Media Apps (JioSaavn, JioTV, JioCinema, JioSphere) by developing checklists, test scenarios, and test cases to ensure high product quality
- Oversaw functional testing across SIT, Pre-production, and Production environments, resolving bugs through Azure DevOps and ensuring no product was launched without final team approval