Amirfarhad Nilizadeh

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| **U.S. Green Card Holder** (No Sponsorship Needed)

Specialized in: Formal Verification in Hardware & Software | Developing, Testing and Debugging

Professional Experience

AMD | Orlando, FL

Member of Technical Staff, Hardware Formal Verification
Jan 2022 - Present

GPU Formal Verification

- Working with advanced formal verification tools including JasperGold and VC Formal, adept at leveraging their capabilities for comprehensive and effective verification.
- A complete end-to-end FPV (full proof) performed to ensure the correctness of six GPU blocks:
  - Used a range of reduced-complexity techniques, including Assume-Guarantee Reasoning, Symbolic Variables, Behavioral Modeling, Abstractions (Counters and Memories), Semi Formal, Black Boxing, Cut Point, Case Splitting, Parameters and Size Reduction, and Scoreboard Integration (Assertion IPs).
  - Detected 22 critical RTL bugs in control logics, including one that caused system starvation and another in RTL IP.
  - Identified four RTL issues affecting design performance.
  - Achieved high formal and functional coverage for FPV sign-off, proving the correctness of all tested blocks. Also, establishing reliable bounds for challenging properties.
- Executed SEC (Sequential Equivalence Checking) verification for a critical GPU block:
  - Verified the clock gating behaviors for accurate power management.
  - Reduced complexity, significantly using single side cut point and hierarchical SEC. (Improved bound from 30 to 75).
- Proved the correctness of several new sub-block designs using FPV (Bug Hunting). (Arbiters, FIFOs, credit/debit)
  - Detected several RTL and performance bugs.
- Performed connectivity checks for three major GPU blocks, ensuring interconnection accuracy.
  - Detected numerous RTL and RDL mismatches (more than a hundred RDL issues).
- Co-authored a paper (related to Post-silicon FV) selected as "Best Paper" at an internal AMD conference.

Formal Methods Lab, UCF | Orlando, FL

Graduate Research Assistant (PhD), Software Formal Verification
2016 – 2021

Publications and Presentations:

- 14 publications (13 as the first author) and 9 presentations in top-tier conferences and journals. (Google Scholar)
- Finalist in UCF's 3MT competition (2021) for research contributions. (Video) (Final Presentation Video)

Main Project: Formal Methods in Dynamic Automated Program Repair

- Demonstrated formal verification's effectiveness in detecting overfitted patches with 100% success. (GitHub) (Paper)
- Developed JMLKelinci, a tool leveraging lightweight specifications to discover bugs. (GitHub) (Paper1) (Paper2)
- Created a prototype tool to convert SMT solver-generated complex counterexample traces into input tests. (Paper)
- Published the first public Java dataset with complete formal specifications, verified by OpenJML's extended checker. (GitHub)

Secondary Project: Evaluating Test Suite Characteristics for Automated Program Repair

- Enhanced test suite efficacy in automated program repair by incorporating SMT solver counterexamples, achieving 87% improvement. (Paper)
- Investigated the impact of coverage metrics beyond branch coverage using formal verification to guide program repair. (Paper)

Side Projects: Image Steganography Tool Development

- Designed and developed an image steganography method to securely hide and transfer digital data through unsecured public networks. (GitHub) (Paper1) (Paper2)

AMD | Orlando, FL

Internship at AMD
Fall 2021

- Conducted comprehensive connectivity checks using VC Formal to validate interconnections within a complex hardware architecture, identifying multiple RTL and RDL mismatches.

Google | Remote

Google Summer of Code
Summer 2021

- Designed and developed a tool leveraging lightweight behavioral specifications, guided fuzzing, and symbolic execution to identify behavioral and security vulnerabilities in Java applications. (Google Code)

CyLab Security & Privacy Institute, CMU| Mountain View, CA

Internship at CyLab Security & Privacy in CMU (NASA Ames Research Center) Summer 2018

- Applied software analysis techniques with a focus on fuzzing tools to identify space-time vulnerabilities (side channels) in code.
- Selected for DARPA Live Engagement 6, contributing to advanced cybersecurity research in Space/Time Analysis. (DARPA)

Azad University | Esfahan, Iran

University Lecturer | Computer Science and Computer Engineering 2013 – 2016

- Delivered undergraduate courses in Computer Science and Computer Engineering, focusing on foundational and advanced topics.

Educational Background

Doctor of Philosophy, Computer Science — University of Central Florida (UCF) | Orlando, FL Dec. 2021

Master of Science, Computer Science — University of Central Florida (UCF) | Orlando, FL Dec. 2018

Master of Engineering, Computer Architecture — Arak University | Arak, Iran Feb. 2013

Bachelor of Engineering, Hardware Engineering — Isfahan University | Isfahan, Iran Sep. 2009

Technical Proficiencies

Hardware Formal Verification — Expertise in JasperGold, VC Formal, FPV, FEV (SEC), Bug Hunting, Complexity Reduction, Formal Coverage, Sign-off, Semi-Formal, Connectivity Check and AEP. Familiar with Post-silicon, Xprop, FEV (CEC), Data Path and Control Register Formal Verification.
Software Formal Verification — Proficient in Java Modeling Language (JML), OpenJML, Java PathFinder (JPF), SMT Solver and Symbolic and Concolic Execution. Familiar with Dafny and Coq.
Hardware Description Languages — Skilled in Verilog, SystemVerilog, SystemVerilog Assertions. Familiar with VHDL.
Hardware Design Verification — Familiar with UVM, constraint-random testing, coverage-driven verification.
Programming Languages — Skilled in Java, C, MATLAB, and Phyton. Familiar with C++, Haskell, and Assembly 8086.
Version Control — Experienced in using Perforce and GitHub for code management.
Scripting — Experienced in writing and manipulating TCL scripts for formal verification tasks.
Fuzzing and Software Testing Tools — Hands-on experience with Mutation, AFL, Junit, PITest, Randoop, EvoSuite, Kelinci, Kelinci-WCA, JMLKelinci, Diffuz.

Certificates

- Cadence Design Systems.
  - SystemVerilog Assertion
  - JasperGold Formal Fundamentals
  - JasperGold SEC
  - Jasper Formal Coverage
- AMD advanced formal verification and sign-off training.
- Seventh and Eighth Summer School on Formal Techniques by SRI, 2017 and 2018.

Selected Publications (Further works available on Google Scholar)

- A co-author, **A. Nilizadeh**: Formal Verification: An Essential Methodology for Post-silicon, 4th Annual AMD Conference, 2023.
- **A. Nilizadeh,** G. T. Leavens, C. Pasareanu, Y. Noller, JMLKelinci+: Detecting Semantic Bugs and Covering Branches with Valid Inputs using Coverage-Guided Fuzzing and Runtime Assertion Checking, Formal Aspects of Computing, ACM, 2024.
- **A. Nilizadeh,** M. Calvo, G. T. Leavens, D. R. Cok, Generating Counterexamples in the Form of Unit Tests from Hoare-style Verification Attempts. IEEE/ACM 10th International Conference on Formal Methods in Software Engineering, IEEE, 2022.
- **A. Nilizadeh**, G. T. Leavens, X. D. Le, C. Pasareanu, D. Cok, Exploring True Test Overfitting in Dynamic Automated Program Repair using Formal Methods. 14th IEEE Conference on Software Testing, Verification and Validation (ICST), IEEE, 2021.

Awards and Honors

- **Paper Review** in several IEEE, ACM, Springer, and Wiley journals. Jan 2019 - present
- **Google Summer of Code Student Grant.** Summer 2021
- **DARPA Grant for Internship and** live engagement 6, Space/Time Analysis for Cybersecurity**.** Summer 2018
- **NSF Grant** for RA position and travel grant for conferences and formal verification summer school. Aug 2016 - Aug 2017

Chess Achievement

- International Chess Player, FIDE chess code: 12531600. World chess rating: 1797
- Among the top 10% of expert chess players in FL and in the USA. (Feb 2025)

* References are available upon request.