Summary:

Verification engineer with 3.5+ years of experience in VLSI Design Verification. Strong expertise in UVM, System Verilog, and Verilog. Experienced in PCIe gen4, USB 3.2, AXI, and APB protocols.

Name: M S Sai Kamesh

Email: sai.ss.682@gmail.com

Phone: 8790460360

Location: --

Country: --

Position Category: --

Desired Job Role: PCIe Verification Engineer

University: --

Degree: B Tech in Electronics and Communication Engineering

Graduation Year: 2021

Years Experience: 3.5

Notable Companies: Green Wave Radios, Excel Vlsi technology (client: Intel)

Top Skills: UVM, System Verilog, Verilog, PCIe gen4, USB 3.2, AXI, APB

Job Intention: --

Visa Status: --

Able: no

Subject: Working at AheadComputing

Date Sent: 02-26-2025

Resume: Yes