LOKADITHYA REDDY YADAMAKANTI

(+1) 919-985-0585 lyadama@ncsu.edu linkedin.com/in/lokadithya-reddy Raleigh, NC

EDUCATION

North Carolina State University, Raleigh, NC Aug 2022 - May 2024
Master of Science in Computer Engineering GPA: 3.6
Coursework: Advanced Microarchitecture; Advanced Computer Architecture - GPU; ASIC Verification; Architecture of Parallel Computers; Microprocessor Architecture; ASIC and FPGA Design with Verilog; Neural Networks

Mahindra Ecole Centrale, Hyderabad, India August 2017 - June 2021
Bachelor of Technology in Electrical and Electronics Engineering

SKILLS

Programming Languages	C++, Python, Verilog, SystemVerilog, TCL
Software & Tools	Synopsys Design Compiler, Xilinx Vivado, ModelSim, GPGPU Sim, Git, Linux, GDB, Vim, Makefile
Methodologies	Microarchitecture, GPU Architecture, Cache Coherence, Virtual Memory RTL Design, Timing Analysis, Performance Analysis, Design Verification, UVM Object-Oriented Programming, Scripting, Data Analysis

ACADEMIC PROJECTS

Out-of-Order Superscalar Processor Simulator **C++**

- Developed an out-of-order (OOO) superscalar processor simulator with multi-instruction fetch and issue per cycle, utilizing Tomasulo's algorithm, under assumptions of perfect caches and perfect branch prediction.
- Analyzed performance metrics (IPC) by tuning issue queue size, reorder buffer size, and pipeline width, demonstrating expertise in CPU architecture and performance optimization.

Performance Analysis of Stride Value Predictor for Superscalar Processors **C++**

- Integrated a Stride Value Predictor with a Value Prediction Queue into an out-of-order processor simulator, optimizing configurations for performance enhancement.
- Evaluated benchmarks to measure IPC, prediction accuracy, and instruction correctness, contributing to advanced CPU performance modeling.

Shared Multiprocessor Simulator for Cache Coherence Protocols **C++**

- Developed a trace-driven 4-processor simulator with bus-based coherence, and its corresponding peer caches, and maintained coherence across them by applying MSI, MSI + BusUpgr, and MESI coherence protocols.
- Analyzed IPC trends by analyzing parameters such as cache hits, misses, and memory transactions.

Cache Memory Hierarchy Design **C++**

- Designed and implemented a two-level trace-driven cache simulator in C++ that incorporated the LRU (Least Recently Used) replacement policy and a write-back write-allocate approach.
- Analyzed trends in miss rate and average access time varying associativity, cache size, and block size.

2-Stage Neural Network Hardware Accelerator Logic Design using Verilog **Verilog**

- Developed a two-stage pipelined neural network that features a convolution layer with the ReLu activation function and max-pooling layers.
- Conducted simulations using ModelSim, and achieved performance optimization through synthesis using Design Vision, resulting in optimized Area, Power, Performance, and Total Delay.

Terrain Classification Model Development using Deep Learning **Python**

- Developed a terrain classification model to classify human activities using deep learning algorithms involving Data Preparation, Data Windowing, Model Building, and Model Training and Evaluation.
- Performance was analyzed using accuracy, precision, recall and F1 score metrics and achieved an accuracy of 93%.

WORK EXPERIENCE

Research Assistant, North Carolina State University, Raleigh **Sept 2024 - Present**

- Developed memory-efficient Python scripts to process large-scale datasets, ensuring optimal performance and scalability for data-intensive tasks.
- Implemented NLTK-based text preprocessing and tensor conversions, resolving data loss issues and enabling robust data analysis and tensor dimension extraction for actionable insights.