Shreesha T P

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Education

Ramaiah Institute of Technology Bangalore
B.E in Electronics and Communication , CGPA:8.85 *December 2021 - June 2025*

Indian Institute of Technology Madras
B.S. Data science and Programming *August 2022-June 2025*

Work Experience

Samsung R&D - Intern October 2023 - August 2024
Input enhancement for Intra prediction for generic video codec

- Implemented neural networks to deform images for enhanced compression within a video codec framework, optimizing bitrate and Structural Similarity Index (SSIM) metrics using advanced deep learning techniques, achieving a 20% reduction in bitrate while maintaining the same PSNR.

S.T.A.R.D.U.ST February 2023 - Present
Head of Avionics

- A student-led club dedicated to participating in rocketry and satellite-building competitions and workshops. Advanced to the final round of the 2023 CANSAT Competition held by ISRO. Also competed in IRoC-U, a Rover Building Competition organized by URSC in 2023.

Projects

RISC-V based Hardware Accelerator for k-NN GitHub Link
Verilog, SystemVerilog, Vivado

- Designed a 32-bit single-cycle RISC-V hardware accelerator for multi-class classification using k-NN, designing a custom processor with base integer set instructions and floating-point extensions for optimized 32-bit single-precision operations.
- Customized the ALU and restructured specific instructions for efficient and accurate predictions, conducted RTL synthesis, reducing resource usage by 20%, and generated utilization reports to analyse performance and resource allocation.

Design of Verification Environment for testing of Communication Protocols GitHub Link
SystemVerilog, EDA Playground

- Developed a comprehensive verification environment on EDA Playground for testing the UART protocol.The environment includes a generator, driver, monitor, and scoreboard to ensure thorough verification of the design, successfully verifying the UART protocol.

LPC2148-Based Morse Code Transmitter GitHub Link
Proteus, Keil

- Developed an embedded system using LPC2148 microcontroller to generate Morse code for hex numbers (0-F) based on keypad input, displaying the input/output on 40x2 LCDs via I2C protocol and implementing LED blinking to visually represent the Morse code.

Exploring Sorting Algorithm's Efficiency via Cadence Genus and NC Launch GitHub Link
Verilog, Cadence

- Sorted 8-bit unsigned numbers using various algorithms, leveraging Cadence for synthesis and simulation. Analyzed power and timing reports, and created gate-level circuitry.

Skills

Programming Languages: Verilog, SystemVerilog, Python, MATLAB, C/C++
Tools & Softwares : Vivado, Cadence, EDA Playground, Proteus, IAR Workbench, Keil, MATLAB, Simulink,Git,GitHub
Hardware Skills : Computer architecture, ARM architecture, RTL design, Digital Design, Design verification
Soft Skills: Innovative, Reliability, Focused, Decision-making, Leadership

Publications

- "RISC-V Architecture based Hardware Accelerator for kNN" - IEEE I4C-2024
- Published Paper: "A novel approach to mitigate micro gravity induced bone loss in astronauts" - IAC 2022.