Summary:

Rajasekhar Narala is a Design Verification Lead with over 10 years of experience in validating high-performance GPUs and accelerators. He has expertise in UVM-based testbenches, optimizing verification flows, and driving successful product launches. He has a proven track record in verifying complex GPU subsystems such as shaders, rendering pipelines, and compute units, consistently improving verification efficiency and product quality.

Name: Rajasekhar Narala

Email: rnarala@asu.edu

Phone: 520 906 1774

Location: Folsom CA

Country: USA

Position Category: Design: Logic design, Verification: Design verification, Architecture

Desired Job Role: Staff GPU Design Verification Engineer

University: Arizona State University, BITS, Pilani

Degree: Master of Science in Electrical Engineering, BE Electronics and Instrumentation

Graduation Year: 2015, 2013

Years Experience: 10

Notable Companies: Intel, AMD

Top Skills: UVM, System Verilog, Verilog HDL, C++, Perl, Python, TCL, Git, Perforce, JIRA, VCS, Verdi, Jasper Formal, OpenGL, DirectX, CUDA, ZEBU Platform

Job Intention: full-time

Visa Status: --

Able: no

Subject: Working at Ahead computing

Date Sent: 03-06-2025

Resume: Yes