arpan.raja@proton.me | 978-277-8505 | linkedin.com/in/arpanraja | US Citizen

Arpan Raja

Refrences available on request

I. SKILLS

System Verilog/Verilog | C/C++ | Tcl | Python | RTLA | Verdi | VCS | PowerArtist | AMBA | TileLink | RISC-V

II. EXPERIENCE

Samsung Semiconductor . . . . . **May 2024 – Apr 2025**
RTL Design Engineer Austin, TX

- Performed timing/power analysis on the coherent interconnect for the Samsung Galaxy Flagship
- Proposed and implemented architectural changes that reduced peak dynamic power consumption upwards of 10%
- Found and fixed critical clock tree timing violations in the design
- Integrated POR features to reduce the memory bottleneck for AI applications
- Removed unnecessary legacy features from the translation block between the CHI protocol and a proprietary ACE-based protocol
- Identified stimulus holes, using code coverage analysis, and communicated the missing test conditions to the DV team
- Setup sign-off flows for IP-XACT, Clock Domain Crossing, X-Propagation, and Automated Extracted Properties
- Worked on next gen architectures to keep up with increasing AI bandwidth requirements

University of Illinois, Urbana Champaign . . . . . **Aug 2023 – May 2024**
Research Assistant Champaign,IL

- Investigated upcoming semiconductors, such as Gallium Nitride and Silicon Carbide, for digital signal processing in power electronics applications

Nvidia . . . . . **May 2022 – Dec 2022**
Design Intern Remote

- Managed and optimized two partitions on next gen tegra processors
- Identified timing issues and communicated necessary solutions to the RTL design team.
- Created a company tool in tcl to quickly select certain timing paths and output relevant data in aggregate for simpler timing analysis

AMD . . . . . **Jan 2022 – May 2022**
Design Intern Remote

- Managed setup and hold time issues that arose with RTL/Floorplan updates for Zen6 cores
- Synthesized a memory based subtile, and instantiated it in the design to improve PPA

III. PROJECTS

Multicore Processor

- Created a 16-core multiprocessor system with a MESI coherence protocol and custom interconnect solution
- Designed and taped out a 5-stage pipeline CPU with an interconnect bus controller on TSMC 64nm
- Soldered all 16-cores to a custom pcb and connected them to a fpga, which served as the memory controller

Out of Order CPU

- Built a RISC-V CPU, with in order commit (ROB) and OoO execution (Tomasulo)
- Contained additional features such as an L2 Cache and a G-share branch predictor
- Introduced an on chip matrix multiplication accelerator to target operations involving fully homomorphic encryption.

IV. EDUCATION

University of Illinois, Urbana Champaign . . . . . **Fall 2019 – Spring 2023**
B.S. in Computer Engineering - 3.73