MADHAVI BOINAPALLY

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EDUCATION

San Diego State University, San Diego, CA Aug 2022 - Dec 2024
Master of Science in Electrical Engineering GPA: 3.6/4.0
Coursework: ASIC Design, VLSI System Design, VLSI Circuit Design, Analog IC Design, VLSI Testing

CVR College of Engineering, Hyderabad, India Aug 2018 - May 2022
Bachelor of Technology in Electronics and Communication Engineering GPA: 3.8/4.0
Coursework: Digital Design, Computer Architecture, ASIC and FPGA Design, Microprocessors and Controllers

SKILLS

Programming Languages	Python, TCL Scripting, SDC, SKILL, Verilog, SystemVerilog, C, C++
Concepts and Methodologies	Place and Route, CTS, CDC, Static Timing Analysis, Timing Closure, DRC, LVS, DFT, Low Power Design, UVM, RTL Design,
Software & Tools	Cadence Virtuoso, Innovus, Genus-Synthesis, Tempus, Linux, Spectre, Synopsys Design Compiler, Xilinx Vivado, ModelSim, Matlab
Certifications	Cadence certificates - SKILL Programming, RTL to GDSII

ACADEMIC PROJECTS

Physical Design of 4-tap FIR Filter **Verilog, SDC**

- Leveraged Synopsys Design Compiler to synthesize the RTL design in a 180 nm CMOS process, optimizing for timing, area, and power using SDC constraints. Applied clock uncertainties of 7%, 10% for accurate timing analysis.
- Automated floor planning, placement, clock tree synthesis, and routing in Cadence Innovus using TCL scripts.

Low Power Design of CORDIC II Architecture **Physical Design**

- Designed low power CORDIC II architecture, targeting both Spartan 3E Xilinx FPGA, and ASIC implementations using Verilog. The ASIC design demonstrated a 28.9% increase in power efficiency.
- Implemented the FPGA design using Xilinx Vivado. Synthesized the ASIC design using Cadence Genus-synthesis, executed the physical design flow using Cadence Innovus.

Optimized ASIC Design and Timing Analysis of MulAcc Circuit **Verilog, TCL**

- Developed parametric RTL design using Verilog. Employed Synopsys Design Compiler and automated synthesis for 19 routing scenarios (full-cycle paths, half-cycle paths, multi-cycle paths) using TCL scripting.
- Performed static timing analysis (STA) to address setup and hold time violations, and optimized critical paths.

Layout Design of 64-Bit (8×8) SRAM **Cadence Virtuoso**

- Implemented size-optimized schematic and layout of 64-bit SRAM with a propagation delay of 0.02 ns.
- Simulated the design in Cadence Virtuoso and performed DRC, LVS, and parasitic extraction.

Adder Layout Design **Cadence Virtuoso**

- Designed CMOS circuit-level schematic and layout optimizing power to 2.813 µW, and area to 50.21 µm2.
- Performed DRC, LVS, and parasitic extraction to assess the impact of layout parasitics on circuit performance.

Built-in-Self-Test (BIST) Design and Simulation **Design for Testability**

- Spearheaded the design and simulation of BIST structure using Built-in Logic Block Observer (BILBO) to test a 16-bit adder in Verilog. Efficiently implemented PRPG and MISR modes to enhance the test.

WORK EXPERIENCE

Research Assistant (Design Engineer), SDSU, San Diego **Jan 2024 - Dec 2024**

- Designed and verified a parallel, pipelined Gated Recurrent Unit for the Brain-Computer Interfacing; synthesized for Xilinx Virtex-7 FPGA, to achieve a 40% throughput increase and 50% hardware efficiency improvement.
- Conducted an error analysis in MATLAB using the mean-square method (noted error: 0.0001) and documented.

Design Verification Engineer, VLSIGURU, Remote **May 2023 - Dec 2023**

- Built SystemVerilog and UVM verification environments integrating generator, driver, monitor, register models for Ethernet MAC, AXI, AHB, SPI, and I2C protocols. Achieved 94% code coverage and 95% functional coverage.
- Implemented functional verification methodologies by developing custom Python and TCL scripts to automate the project. Leveraged Questasim to debug and improve project efficiency.