Ulises Gutierrez

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Education

North Carolina State University - Engineering Online

Master of Science, Computer Engineering, GPA: 4.1665 Graduation December 2025

- Relevant Coursework: ASIC & FPGA Design, Architecture of Parallel Computers , VLSI Systems Design, Microprocessor Architecture, Neural Networks, ASIC Verification, Advance Microarchitecture

Bachelor of Science, Computer Engineering, Summa Cum Laude August 2015 - December 2019

Course Projects

Transformer Model Self-Attention Equation

- Implemented a synthesizable (excluding memories) matrix multiply Verilog module to calculate the scaled dot-product attention equation as described in A. Vaswani et.al “Attention is all you need”
- Design used 3 SRAM modules (2 for matrix inputs and 1 for output), pipelined multiply-accumulate unit, 2 FSM’s for control, 4.9ns clock period, achieved best performance in my specific class section (defined by 1/ area*delay)

64 bit (8x8) Content Addressable Memory

- Collaborated in a group of three to design (schematic and layout) a 64 bit CAM using Synopsys Custom Compiler with the FreePDK 3nm design kit
- Used a combination of 9T NAND and NOR bitcells in the array to balance power and speed of design

CPU Simulators

- Actively working on academic projects to implement stages of a modern out-of-order superscalar processor in C++. Blocks include rename, dispatch, register read, and retire.
- Implemented a C++ cycle accurate simulator of a 5-stage Out-of-Order processor with support for speculative execution, load/store bypassing, MIPS ISA (Spring 2024)

Work Experience

Product Development Engineer – Analog Devices, Durham, NC August 2022 - December 2023

- Developed, on LabVIEW and Teststand, a suite of RF tests to verify embedded firmware and algorithms of an eight transmitter, eight receiver, two observation receiver RF IC designed for 3G/4G/5G TDD/FDD small cell, massive MIMO, and macro base stations.
- Collaborated with Applications, Project Management, Design, and Software teams to perform regression testing and bug fixing for upcoming software releases to ensure on time delivery to various customers
- Utilized C#, NUnit test framework, and Visual Studio Code to develop IQ compression/decompression tests for ORAN compliance using Keysight S5040 DU Emulator and an in-house FPGA platform to de-risk future products.

Test Development Engineer – Analog Devices – Greensboro, NC March 2020 – August 2022

- Developed of hardware/software to run High Temperature Operating Life (HTOL) qualification of RFIC transceivers
- Created python scripts to test firmware fixes for customer returns or implemented ATE test screens using LabVIEW/Teststand to screen out issues at final test.
- Schematic capture of burn-in board for 8Tx, 8Rx, 2Orx transceiver, 10 DUT’s/board, power delivery using three different rails, communication buses (SPI, I2C, RS232), temperature monitoring, and onboard MCU
- Developed embedded firmware and Labview application to control and monitor data points such as temperature, voltage, and current draw during High Temperature Operating Life (HTOL) stress tests of RF transceiver IC’s.

Skills

- Languages and Tools: SystemVerilog, C/C++, Python, Labview, Teststand, Git
- EDA Tools: Synopsys Custom Compiler, Synopsys Design Compiler, Questa Simulator, Allegro Schematic Capture
- Lab instruments: Oscilloscopes, Spectrum Analyzer, Signal Generators, DMM’s, Power supplies, VNA’s
- Academic Experience: RTL Design, Object Oriented Programming, CPU Architecture, Cache/Memory Coherence