Summary:

Highly motivated and experienced CPU physical design and STA engineer with 9+ years of experience involved in designing high speed CPU and server designs with expertise in Synthesis to GDS flow and timing convergence. Very well versed with logic equivalency verification (FEV) and debugging.

Name: Nikhil Pillai

Email: nikhilmohanpillai@gmail.com

Phone: +1(480)-335-2646

Location: Beaverton, OR

Country: USA

Position Category: Design: Physical Design

Desired Job Role: Staff Physical Design Engineer - PPA Optimization

University: Arizona State University, University of Mumbai

Degree: Masters in computer engineering, Bachelor of Engineering

Graduation Year: 2015, 2012

Years Experience: 9

Notable Companies: Intel Coporation

Top Skills: Scripting: Tcl, Perl, Shell, Python, Tools: Synopsys Fusion Compiler, Primetime, PTPX, Cadence Conformal LEC

Job Intention: full-time

Visa Status: --

Able: yes

Subject: Working at AheadComputing

Date Sent: 03-26-2025

Resume: Yes