Sai Surendra Reddy Yaraballi

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Education

Texas A&M University, College Station, TX — Jan 2023 - Dec 2024
Master of Science in Computer Engineering — *GPA: 3.5/4*
- **Coursework**: Advanced Hardware Design Functional Verification, Advanced Computer Architecture, Parallel Computing, Digital Integrated Circuit Design, Microprocessor System Design, Test and Diagnosis of Digital Systems (DFT)

Gandhi Institute of Technology and Management, Visakhapatnam, India — Jun 2016 - Jun 2020
Bachelor of Technology in Electronics and Communication Engineering — *GPA: 9.07/10*
- **Coursework**: Digital System Design, Digital Logic Design, Basic VLSI Design, Computer Organization and Design

Technical Skills

Programming Languages: Verilog, SystemVerilog, UVM, SystemVerilog Assertions, UPF, C, C++, Python, Tcl

Tools: Xilinx Vivado, Synopsys - VCS, Verdi, Design Compiler, PrimeTime, TestMAX ATPG, Design Vision, Cadence - Simvision, Xcelium, JasperGold, vManager, IMC, Virtuoso, Innovus

Protocols: DDR, AXI, AHB, APB, I2C, UART, SPI

Experience

Tata Consultancy Services, Hyderabad, India — Oct 2020 - Nov 2022
Assistant System Engineer
- Developed, tested, and deployed Java based intranet applications to manage, store and fetch product data for users. Developed shell scripting scripts to set the environment in linux server to run application.
- Collaborated with three other team members to revamp enterprise application 70% UI in terms of design, responsiveness, layout, and scalable with minimal API hits in React JS.
- Aided Business Analysis team by employing software reverse engineering techniques to capture and understand business requirements.

Centre for Development of Advanced Computing, Hyderabad, India — May 2019 - Jun 2019
RTL Design Intern
- Designed DDR SDRAM Memory controller by developing RTL code using Verilog HDL and verified and simulated the design by creating a testbench in Xilinx Vivado.
- Implemented and validated an FPGA-based temperature monitoring and control system using Verilog HDL.

Projects

Functional Design and Formal Verification of Multicore MESI based Cache Design System
- Created verification plan from design specification at the IP level and constructed UVM testbench to verify MESI Cache Coherency protocol on Cadence Xcelium.
- Developed assertions, cover groups, and 35 test methods to validate 19 features, analyzed Simvision waveforms to identify bugs, and achieved 94.09% functional coverage and 92.72% code coverage by triaging regressions.

Design and Functional Verification of AHB2APB Bridge using UVM
- Designed Verilog RTL design for AHB, APB and AHB2APB bridge protocol and developed the UVM testbench including driver, sequencer, monitor and scoreboard components and verified functionality of AHB2APB Bridges.
- Created a Verification plan and developed constraint random stimulus along with assertions, cover groups and traige regression and achieved a functional coverage of 100% and code coverage of 93.28%.

RTL Design of MIPS 5-stage Pipelined Processor
- Developed digital logic of basic building blocks of CPU such as Register File, ALU, Data Memory unit, ALU Control unit and verified functional correctness using Verilog test bench in Xilinx Vivado ISE.
- Implemented Forwarding and Hazard units to overcome pipeline hazards. Integrated these units with remaining data path logic. Verified functionality using Verilog test bench. Attained a maximum frequency of 125MHz.

Implementation of Perceptron Based Branch Predictor
- Implemented Perceptron based branch predictor using C++ in Champsim Simulator and compared the perfromance with Gshare, Tournament and Bimodal branch predictors.
- Achieved improvement of 7.61% in branch accuracy, 13.1% increase in IPC and 39.4% decrease in MPKI by running 10 integer and 10 FP benchmarks from SPEC CPU 2017 suite.

Formal Verification of Combinational Lock
- Developed assertions, assumptions, and cover points for the combinational lock design by analyzing the specification sheet, utilizing formal property verification techniques to ensure design correctness.
- Developed the script to perform mathematical analysis by using JasperGold tool, leveraging formal property verification to debug the design, identify, and resolve critical bugs.

Certifications

- System Verilog for Design and Verification v21.10 offered by Cadence Design Systems.
- System Verilog Accelerated Verification with UVM v1.2.5 offered by Cadence Design Systems.