M S Sai Kamesh
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Overall experience : 3 .5+ Year in VLSI Design Verification(IP and SoC) (2021 oct- present) and 6 months training.

Education:

B Tech [2017-21] : Electronics and Communication Engineering (Raghu institute of technology 8.2/10)
Intermediate [2015-17] : Narayana Jr college [945/1000]
SSC [2015] : Vijayam techno school[8.0/10]

Area of Expertise / Project summary :

Green Wave Radios : [May 2023 - present]

Worked on PCIe gen 4 :

1. Integrated PCIe RTL with VIP in SoC level and created wrapper for PCIe (core,pcs,pma).
2. Written test cases for PCIe(PCIe having interface with AXI master, slave and DBI) on PL,DL and TL.
3. Implemented Outbound transactions from Packet Processor To PCIe AXI interface (and VICE VERSA).
4. Experience in PCS/PHY/CLK debugging
5. Implemented Port driver For EP transactions
6. Configured VIP from PUREVIEW according to Specification of inhouse product.
7. Written sequences and tests according to SoC level requirements on PCIe.
    1. Inbound Outbound AXI transaction sequences
    2. BIT Bash sequences (with ral and without ral)
    3. PME ACK and nak seq implementation
    4. MSI sequences (CPU -> EP -> RC) and MSI debugging and MSI pending bit issues and MSI generation
    5. TLP sequences on CFG,MEM TLP's
    6. LTSSM debugging and DLCMSM debugging
    7. Found Issues on Inhouse PCS CLK blocks like core clock, aux clock and synchronization issues.
    8. Debugging Experience on gear box of PCS block

Worked on RxDFE & Efuse

1. Developed Complete SoC level env and test bench for RxDFE and Efuse.
2. Written sequences and tests and injected test vectors for RxDFE and verified each sub block.
3. Performed register access for both RxDFE and Efuse to verify register access at software level
4. Worked On Block level and Top level (Complete verification of RxDFE and Efuse)

Excel Vlsi technology : [2021 to may 2023 [clint intel]] [Worked on USB 3.2, PCH]

1. Experience in Intelfabric protocol IOSF (Depended on IOSF ISM) .
2. Experience in UVM methodology(Written test casesfor USB 3.2 , XHCI as Host), And Debugged few test cases
3. Debugg Experience on Constraintrandomverification at sublevel IP DBC, USB, XHCI.
    -> Debugged on Link Training Status State Machine (LTSSM), Link layer and Protocol layer.
    -> Debugged on USB-DBC Transactions. And XHCI-USB Transactions.
    -> Debugged on XHCI PORTSC register concepts.
    - Having debug Experienceo n USB (worked on Link Layer and LTSSM, Protocol Layer)
    - Includes the detailed verification of different categories of failure occurred in USB IPs such as test components.
4. Verified few testcases based on Assertion verification, that depend on Wake conditions(Self wake and Remote wake).
    -> Debug Experience on RAL debugging (FRONTDOOR ACCESS).
    -> Debugging on Control and Status Registers.

-> Verifying the Data transactions from CSME ip to other ip's in SoC and vice versa.
-> Debug Experience on Error Scenarios in interconnect(IOSF,AHB).
-> Debug Experience on Interconnect verification that uses AHB, IOSF protocols.
-> Worked on Low power modes of CSME.

Worked in specmen e project verifying AHB – IOSF Bridge (oct 2021-feb 2022) .
Good knowledge on UVM RAL Debugging.
Having good knowledge on AMBA bus protocols.
Debugging experience of AXI/APB protocol using SV.
Having Basic Knowledge on SX and S0iX powerstates

Tools: VCS, Cadence, VERDI, DVT (at basic level), git, Questasim
Programming Languages: Verilog, system Verilog, UVM, UNIX, PERL
Protocols: PCIe gen4, PIPE-5.1 , USB3.2, AXI, APB (CSME PCH Intel on chip soc)