Hi

I'm currently working for Altera, which may or may not be in the process of being sold off by Intel.

If we continue with ex-Intel exec management and their reduced engineering staffing levels I'm going to want to move on, however I'm looking to stay involved with RISC-V development.

As you'll appreciate Altera is an FPGA business, and I was initially drawn to the potential of building spatial-compute architectures using these devices. Though it seems I have spent my entire career swinging between HPC and industrial applications!

The Altera RISC-V soft cores have a simple 3 or 4- stage pipeline, single-issue and without speculative execution - so I cannot claim to have leading-edge knowledge! My role has been to add capabilities that are valuable in industrial applications, namely the FPU and now also the Core Level Interrupt Controller (it has been interesting to be involved in the Fast Interrupts TG).

In my past work as an IP engineer with Altera, I've been the technical lead for fabric integration of the Agilex 7 M series HBM controller and fabric NoC, worked on heterogenous FPGA+Xeon compute solutions for the financial service industry, DSP IP, and also the OpenCL compiler for FPGA (not my choice, a reorg moved me off DSP IP - but the point is that I have a pretty good - if now somewhat rusty - understanding of compiler internals, both front and middle end).

I am based in the UK so that might rule me out from theget-go, and as you can see my knowledge is broad rather than especially deep.

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