Roger Hayward

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Summary of Qualifications

- **Signal Integrity / Power Integrity / Electro-Migration Reliability Verification Engineer**. Transmission line analysis (frequency-domain), package power delivery modeling, package-to-bump EM/IR analysis including die-stacking ("3D").
- **Modeling & Characterization** of on-wafer & thin film structures, including measurement of GaAs / GaN technologies, passives, transmission lines, high performance sockets and RF probes.
- **CAD Automation Expert**: Fully Automating verification flows after methodology has been properly established.
- Adjunct instructor, Portland State University: Microwave RF Circuits, RFIC Design.

Major Accomplishments

- **Cell-based Design Reliability Verification** tool for emerging CPU designs (1999-2001). Wrote internal (C++) program to perform EM checks on early synthesis layout 1 decade before commercial tools were available. Tool was retired after 20 years of regular use.
- **Novel approach to Noise Parameter Extraction**: Utilized a Keysight VNA with vector-corrected noise receiver and source-pull system to measure noise figure on GaAs and GaN devices to 50 GHz. Keysight adopted the technique into future product offerings.
- **3D EM verification of stacked-die**. Utilized commercial "3D RV" tools on flagship CPU designs to properly model power distribution of integrated voltage regulators, silicon interposer and package substrate to guarantee quality prior to first tape-out.

Professional Experience

Intel Corporation, Hillsboro, OR

Physical Design Integration Engineer, DDG, Multi-die Power Delivery (EM/IR) Dec 2013- Nov 2018, Nov 2020-Present

- Multi-Die Power Delivery, Client CPU products. Lead engineer developing multi-die EMIR techniques for lead designs. Developed automated package model (SPICE) extraction using Sigrity PowerDC; Automated flows to improve turnaround time and design quality.
- Reliability Verification automation for block-level and chip-level verification. Power Grid checks for Electro Migration & IR Drop. Developed methodologies for > 1 Billion resistor network checks, including 3D stacked die and package emulation.

FormFactor, Beaverton, OR

Senior Staff Engineer, R&D Probe Architecture Nov 2018-Nov 2020

- Responsible for Power and Signal integrity analysis on emerging space transformer designs for high volume wafer-test applications. Created automated flow to analyze new designs through Sigrity PowerSI / PowerDC & ADS for power impedance, IR drop, and signal integrity. Developed new architectures to scale product line to meet future applications.

TriQuint Semiconductor, Hillsboro, OR

Senior Engineer, Semiconductor Device Modeling Group Oct 2009 – Dec 2013

- Measurement expert, Modeling Laboratory. Responsible for developing new measurement processes related to device modeling and material characterization. Developed systems to archive measurements for internal distribution. Created numerous flows for automated data analysis, plotting & reporting.
- Hands-on experience with advanced on-wafer RF test systems, including Load Pull, IMD, Noise Figure, nonlinear power sweeps (NVNA); Scattering parameters, spectrum analysis, phase noise, pulsed-IV and flicker noise measurements.
- Developed a new technique for obtaining noise parameters directly with a Keysight VNA and source tuner. Presented a paper at the 80th ARFTG conference, Nov. 2012. The technique was integrated into the VNA as a product option.

Portland State University, Portland OR

Adjunct Instructor, ECE Department — Winter Term 2014, Spring Term 2016

- Instructor, Senior / Graduate level Microwave RF Circuits courses. Presented techniques on transmission lines, wave theory, Smith Chart, impedance matching. Created lab curriculum to reinforce topics. Received adjunct ECE instructor of the year, 2014.

Cascade Microtech, Beaverton, OR

Senior Engineer, Pyramid Probe Engineering Group — May 2005-Oct 2009

- Circuit design of transformers, impedance matching networks & other applications involving Pyramid Probes. Extensive use of Ansoft HFSS & Keysight ADS for package characterization. Automated steps to streamline layout verification into HFSS.
- Developed breakthrough high volume production probe for emerging 77 GHz RF applications (5G). Verified the design through laboratory measurements to 110 GHz. Received a patent involving this work.
- Applications Support: Published application notes on Pyramid probe technology, including transmission line circuit modeling, impedance matching, in-situ baluns & calibration techniques. Presented papers annually at the (IEEE) Semiconductor Test Workshop.

Intel Corporation, Hillsboro, OR

Senior Staff Engineer, Desktop Microprocessor Products Group — Dec 1993 -Jan 2004

- Responsible for implementing and improving reliability verification (RV) tools for 180nm – 65nm microprocessor design power delivery layout. Developed a next-generation power grid estimator and validation tool in C++, (20,000 lines). This tool was renamed "Airstream" in 2006 and was used internally for 15+ years. The Grid Estimator allows for rapid prototyping of power systems for emerging process technologies. The grid estimation project earned a best-paper award at an internal conference.
- Created dynamic IR-drop methodologies to identify weak links in layout. This closed the loop between timing tools and power delivery layout. Created automated flows to improve coverage, accuracy, and time-to-market for multiple flagship CPU designs.

Education

Portland State University, Portland OR — 2005

Post-Graduate Courses in Microwave Engineering.

Oregon State University, Corvallis OR — 1992, 1986

Master / Bachelor of Science in Electrical and Computer Engineering

Skills

C/C++, Perl, Python, TCL. Written programs to interact with complete measurement systems.

Analog Circuit Measurement & Simulation Tools: Ansys HFSS, Sigrity PowerSI, Keysight ADS, Redhawk/SC/GPS, Cascade WinCal, Analog LT-Spice. Comfortable with RF test and measurement equipment, including Vector Network Analyzers. Experienced with Load Pull systems to 50 GHz, Noise Parameter extraction, Gain Compression, IMD, PAE, Pulsed-IV measurement systems.

Designed, prototyped, and built a 500 MHz weak-signal RF power meter with LCD display and high-resolution features. Received the ARRL 2006 Technical Excellence award for a published article on this design.

References available upon request.