SHREYA MAHETALIYA

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EDUCATION

University of Washington, Seattle September 2023 – June 2025
MS in Electrical and Computer Engineering GPA: 3.92
Relevant courses: Computer Architecture, Complex VLSI System Design, HPCA, Advanced Embedded System Design

K. J. Somaiya College of Engineering, Mumbai, India August 2017 - June 2021
Graduated with a Bachelor of Technology in Electronics with *Distinction* GPA: 3.82
Received merit prize for ranking 1st in 4th Semester Applied Mathematics among 130 students in the department

TECHNICAL SKILLS

- Programming languages: C, C++, Java, Python, Verilog/SystemVerilog, HTML, CSS, SQL
- RTL Design, Coverage, Microprocessors and Microcontrollers
- Tools and Software: Cadence (Genus, Innovus, Conformal LEC, Tempus), ModelSim, Quartus, MATLAB, LTspice, AutoCAD, Arduino IDE, SAP, Linux, Proteus, Eagle

PROFESSIONAL EXPERIENCE

JumpStartCSR, Seattle, USA| *Electrical Engineer Intern* June 2024-September 2024

- Tested and validated a proof of concept for a BLE gateway to transmit sensory data from wearable devices to the cloud by integrating BLE with LTE-M connectivity and adding GNSS functionality
- Contributed to developing a prototype Personal Gateway that receives multiple data streams from wearable devices via Bluetooth and transmits them to the cloud using 5G
- Collaborated with a multidisciplinary team to ensure seamless integration and functionality of the gateway system

Accenture, Mumbai, India| *Software Engineer Analyst* June 2021- July 2023

- Acted as an SAP Functional Consultant while gathering requirements from the client (Microsoft), interacted with the business users on the requirement, and worked closely with the development team on the implementation; tested the scenarios of the different requirements in SAP software on every sprint basis
- Involved in designing a system model in the SAP software for Microsoft under Accenture to support E-Invoicing Digital Transformation as made mandatory by the Indian Government

PROJECTS

Hardware accelerator for QR decomposition March 2024 – June 2024

- Designed and implemented a hardware accelerator using the Modified Gram-Schmidt algorithm to enhance numerical stability and accuracy in orthogonal matrix computations
- Wrote RTL for the entire architecture and executed the RTL to GDSII flow, including RTL synthesis with timing constraints using Cadence Genus and conducted place and route in Cadence Innovus, ensuring compliance with design rules using MAGIC for DRC, and performing sign-off STA with Tempus
- Identified and documented limitations and future optimization opportunities, focusing on algorithmic refinements, hardware architecture enhancements, and power efficiency improvements

Verification mini project March 2024

- Verified a synthesizable SystemVerilog module from Basejump STL, ensuring it included two or more covergroups and six or more control signals
- Developed a testbench in Python using the cocotb library, achieving 100% functional coverage

Domain-specific accelerator design: Conway's Game of Life January 2024 - March 2024

- Implemented an RTL accelerator with a streaming interface to accelerate a specific algorithm
- Executed RTL to GDSII flow, including RTL synthesis with timing constraints using Cadence Genus, and ran formal verification in Cadence Conformal LEC
- Conducted place and route for this accelerator in Cadence Innovus, ensuring compliance with design rules using MAGIC for DRC and Calibre LVS for LVS, and performing sign-off STA with Tempus
- Optimized critical path by performing RTL optimization and clock tuning, resulting in a 4.83% improvement in performance, an 8.8% reduction in power consumption, and a 17.36% decrease in area

Pipelined ARM Microprocessor September 2023 - December 2023

- Developed a 64-bit ARM Single-Cycle CPU by creating various critical components, including register file, ALU, Datapath, and Control signals
- Building on the single-cycle CPU foundation, developed a simple 5 stage pipelined ARM microprocessor for a 12 instruction ISA, focusing on enhancing performance and efficiency within the architecture
- Implemented stages for instruction fetch, decode, execute, memory access, and write-back to ensure improved throughput and synchronization within the processor
- Utilized Verilog for hardware description and modeling of the CPU architecture, with simulation and verification carried out using ModelSim