Shravan Ramamoorthy

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EDUCATION

University of Illinois at Urbana-Champaign — Champaign, USA
Master's, Electrical & Computer Engineering — Jan. 2024 – Present (Expected May 2025)

SRM Institute of Science and Technology — Chennai, India
Bachelor's, Electronics and Communication Engineering — Jun. 2017 – Jun. 2021

Related Coursework
Computer Organization & Design, Advanced Computer Architecture, Digital Systems, VLSI Design, Digital Logic Design with VHDL

TECHNICAL SKILLS

Programming Languages: SystemVerilog ; Python ; C/C++.
Methodologies: UVM ; Constrained-Random, Assertions-Based and Metric-Driven Verification ; Object Oriented Programming
Tools: Synopsys VCS ; Verdi ; gem5 Simulator
Domains: Cache Coherence ; Pipelining ; Branch Prediction ; RTL Debugging ; Processing in Memory (PIM).

PROJECT HIGHLIGHTS

PIM-Based Matrix Multiplication Accelerator

- Worked with a team to implement scalable Processing-in-memory (PIM) based matrix multiplier in SystemVerilog using dynamic unit selection and parallel chunking strategies and verified robustly with the UVM flow.
- Developed UVM testbench components-sequencers, monitors, and scoreboards to verify functionality across configurations.
- Simulated RTL in VCS and benchmark against CPU implementations in gem5 to analyze performance trends.

MESI Cache Coherence Protocol

- Designed and verified a snooping-based MESI cache coherence protocol for a 4-core system with crossbar interconnect and centralized arbiter.
- Developed assertion-driven and constrained-random testbenches, achieving ~85% functional coverage across key transitions.
- Debugged 10+ transient mismatches using VCS and Verdi, ensuring reliable state behavior and memory consistency.

Bimodal and TAGE Branch Predictors

- Designed and verified 32-entry bimodal and TAGE branch predictors with geometric history lengths, achieving high accuracy.
- Enhanced alias resolution by 25% through tag/hash tuning and verified correctness through directed and randomized testing.
- Verified an 8-entry Branch Target Buffer (BTB) under LRU and collision conditions for realistic branch scenarios.

Pipelined 4-Way Set-Associative Cache

- Designed and verified a 4-way set-associative cache with pseudo-LRU replacement, through randomized & assertion-based testing.
- Integrated OpenRAM models to ensure timing correctness and validated behavior under concurrent read/write access.
- Achieved 90%+ tag and dirty-bit coverage, resolving 15+ protocol mismatches across operational test cases.

5-Stage Pipelined RISCV Processor

- Designed and verified a 5-stage pipelined RISC-V processor with hazard detection, data forwarding, and flushing mechanisms.
- Created constrained-random tests for 40+ scenarios; automated regressions reduced verification time by 35%.
- Connected RVFI and Spike golden models to identify and resolve compliance issues, ensuring ISA correctness.

Gem5 Simulation Projects – ISA Comparison, Cache Design Space, Ideal Prefetcher Modeling.

- Wrote and modified Python simulation scripts to configure system parameters, run experiments, and collect performance stats.

WORK EXPERIENCE

Software Development Engineer — Bangalore, India
Nunify — Jul 2021 – Jul 2023

- Built and maintained modular, spec-compliant application components with reusable logic, ensuring consistency and reliability across complex feature sets.
- Developed 20+ robust features using systematic debugging and test-driven workflows, significantly reducing regressions and improving long-term stability.
- Automated key internal flows like quote generation and validation using lightweight scripting, improving efficiency and minimizing manual touchpoints.