*Formal Verification Engineer – Intel Corporation*

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# Rocco Salvia

My primary goal is to make computer programs reliable, safe and efficient.
I started my professional career in the domain of software verification, with the development of static analysis techniques to detect security issues in Android applications. During my PhD, I developed hands-on experience with automated theorem provers and symbolic execution especially in the domain of numerical analysis. I studied how to improve the scalability and the performance of several verification engines in the context of real-word problems. Currently, I develop formal proofs to guarantee the correctness of digital circuits.

## Professional Appointments

*[1/2022]*

### Formal Verification Engineer at Intel Corporation, Santa Clara (USA)

Managers: *G. Gavrielov*

Datapath verification using the state-of-the-art for formal I write proofs to guarantee the correctness of digital circuits. I study what are the best practices to tackle the complexity of the verification process. I can debug complex RTL designs, and I can understand where in the design the engines are struggling and why. Moreover, I can deeply understand the specification of a design and suggest modifications towards formal friendly specs. Finally, I can orchestrate and lead the work between architects, designers and formal engineers. I lead the trainings and the ramp-up of new members in my group, I supervise other PhDs and engineers and I guide them in the process of executing, learning, and delivering results.

*[5/2020 - 9/2020]*

## Research Intern at Facebook (now Meta), Seattle (USA)

Manager: *S. Qadeer*

I study the fragility of SMT solvers towards futile mutations in the verification environment (aka butterfly-effect). In collaboration with Microsoft RiSE, I extended the logging architecture of z3 to log the activity of the solver.
Prototype at: https://github.com/Z3Prover/z3/pull/4619

*[4/2019 - 8/2019]*

## Research Assistant at Imperial College, London (UK)

Manager: *G. A. Constantinides*

I study how to use automated theorem provers to run numerical analysis of floating-point programs. I developed a prototype to estimate the likelihood of the rounding error lying within a given interval.
Prototype at: https://github.com/soarlab/paf

*[1/2019 - 4/2019]*

## Research Intern at MPI-SWS, Kaiserslautern (Germany)

Managers: *E. Darulova, R. Majumdar*

Design of memory efficient mixed-precision Model Predictive Controllers (MPC) for robust control of Linear Time Invariant (LTI) micro controllers. I study how to combine SMT solvers and static analysis to guarantee the implementation of a microcontroller is robust to the perturbation caused by the use of finite precision arithmetic.

*[6/2018 - 12/2018]*

## Research Intern at NASA Langley Research Center, Hampton (USA)

Managers: *L. Titolo, C. Muñoz*

I implemented a prototype of SMT solver able to reason about the mix of real and floating-point formulas.
I tested my prototype on real-world safety critical applications to detect when the ideal execution of a program (with pen-and-paper) diverges from the finite implementation in a computer.
Prototype at: https://github.com/nasa/FPRoCK

*[5/2016 - 8/2017]*

## Software Developer at Julia S.R.L, Verona (Italy)

Managers*: P. Ferrara, F. Spoto*

I developed static-analysis techniques to detect leaks of sensitive data in Android applications. I also worked on security issues in automotive systems together with the analysis of Android auto apps.

# Education

[9/2017 - 9/2021]

### PhD in Computer Science at the University of Utah, Salt Lake City (USA)

*Advisor: Z. Rakamarić*

*Thesis*: "Formal Analysis of Floating-Point Programs in Uncertain Environments"

[9/2014 - 11/2016]

### Master's degree in Cyber Security at the University of Venice, (Italy)

*Advisor: A. Cortesi*

*Thesis*: 'Intent Flow Analysis in Android Applications'

[9/2011 - 10/2014]

### Bachelor's Degree in Computer Science at the University of Venice, (Italy)

*Advisor: A. Cortesi*

*Thesis*: '360° Multisource feedback evaluation of the Veneto regional council staff'

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# Publications

1. G. Constantinides, F. Dahlqvist, Z. Rakamaric, R. Salvia: 'Automated Roundoff Error Analysis of Probabilistic Floating-Point Computations' ACM Trans. Probab. Mach. Learn (TOPML), 2024.
2. R. Salvia, A. Gupta, J. O'Leary: *'Measuring ECC - Quality of Implementation using symbolic co-simulation in Python', Jasper User Group (JUG) 2023.*
3. G. Constantinides, F. Dahlqvist, Z. Rakamaric, R. Salvia: *'Rigorous Roundoff Error Analysis of Probabilistic Floating-Point Computations',* International Conference on Computer-Aided Verification (CAV), 2021*.*
4. F. Dahlqvist, R. Salvia, G. Constantinides: *'A Probabilistic Approach to the Accuracy and Stability of Numerical Algorithms'*, Asilomar Conference on Signals, Systems, and Computers (ASILOMAR), 2019.
5. M. Salamati, R. Salvia, E. Darulova, S. Soudjani, R. Majumdar: *'Memory-Efficient Mixed-Precision Implementations for Robust Explicit Model Predictive Control'*, International Conference on Embedded Software (EMSOFT), 2019.
6. R. Salvia, L. Titolo, M. Feliu, M. Moscato, C. Munoz, Z. Rakamaric*: 'A Mixed Real and Floating-Point Solver*', NASA Formal Methods Symposium (NFM), 2019.
7. R. Salvia, Z. Rakamaric: *'Exploring Floating-Point Trade-Offs in ML*', Workshop on Approximate Computing Across the Stack (WAX), 2018.
8. R. Salvia, P. Ferrara, F. Spoto, A. Cortesi: *'SDLI: Static Detection of Leaks across Intents'*, International Conference On Trust, Security And Privacy In Computing And Communications (TRUSTCOM), 2018.