Summary:

Sanket Patil is a recent graduate from Portland State University with a Master's degree in Electrical and Computer Engineering. He has hands-on industry experience from his internship at AMD as a CPU Post-Silicon Validation Intern. He has a strong academic foundation in Computer Architecture, System Verilog, Assertion-Based Verification, Formal Verification, and advanced methodologies like UVM, RTL Design and ASIC workflows, STA, and coding languages like SV, C/C++, Python.

Name: Sanket Patil

Email: sanketpatilpdx@gmail.com

Phone: (971) 427-8865

Location: Portland, OR

Country: USA

Position Category: Verification: Design verification

Desired Job Role: Design Verification Engineer

University: Portland State University, K J Somaiya College of Engineering

Degree: Master of Science- Electrical and Computer Engineering, Bachelor of Technology- Electronics and Telecommunication Engineering

Graduation Year: 2024

Years Experience: 1

Notable Companies: AMD

Top Skills: Verilog HDL, System Verilog, C/C++, UVM, Python, Linux, Assembly Language, RTL Design, Cache, Pipeline, Assertions, Constraints, Coverage, DFT, RISC-V, Formal Verification, Object Oriented Programming (OOPs), UVM, DDR, STA, Synthesis, ASIC, SOC, Microarchitecture, Debugging, Problem solving

Job Intention: full-time

Visa Status: --

Able: yes

Subject: Seeking Full - Time Opportunities in Design Verification

Date Sent: 04-01-2025

Resume: Yes