Cesar Tomás Gómez Cruz

Computer Engineering – UNAM
Specialization on Statistical Methods Applied to Data Science – CIMAT
Specialization on Embedded Systems – ITESO
MSc Electrical Engineering focused on Automatic Control – CINVESTAV
Master in Electronics Design – ITESO
PhD. in Sciences in Engineering with focus on IA – ITESO

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Senior Electronic Designer
Verilog **/** SystemVerilog **/** VHDL
VCS **/** DVE **/** Verdi **/** Questa **/** ModelSim
UVM **/** SystemVerilog Assertions

Embedded Systems Developer
C **/** ARM Assembly **/** PIC Assembly **/** TMS320xx Assembly
Robotics **/** Automotive **/** Communications
TI-RTOS **/** FreeRTOS **/** Zephyr

Senior Software Developer
C#/C++/C **/** Java **/** Python **/** Perl **/** Kotlin **/** Swift **/** HTML+CSS
SQL Studio **/** SQL Lite **/** MySQL **/** Postgress
Linux **/** Windows **/** MacOS **/** Android **/** iOS

Data Scientist
Python **/** R Language **/** C#/C++ **/** Matlab **/** SQL
Tensorflow **/** PyTorch **/** Keras
SPSS **/** JMP **/** Orange **/** Splunk

Summary

I am an electrical engineer in the classic sense of denomination, with strong expertise in software development (+15 years) for desktop, embedded and web systems, data analysis (+10 years), digital electronics design and validation (+5 years) and automatic control (+15 years).

As a digital electronics designer, I have knowledge and expertise using Verilog, SystemVerilog and VHDL for digital systems, in combination with tools from Synopsys and Mentor Graphics to simulate functional behavior (VCS, DVE, Verdi, Questa and ModelSim) and with UVM and SystemVerilog Assertions to create testbenches. For analog, mixed signal and high frequency systems I have knowledge and expertise working with Virtuoso, PSpice, LTSpice, Qucs, ADS and HFSS.

As software developer, I have proficiency using C#, C/C++, Java, Python, Perl, Kotlin and Swift as primary tools over several operating systems: Linux, Windows, MacOS, Android, iOS, TI-RTOS, FreeRTOS and Zephyr (last three for embedded systems). It's worth to mention that I have worked mainly, developing desktop applications (connected to databases), systems simulators, web sites (also connected to databases), firmware (for signal processing, control algorithms and communications) and mobile applications (academic projects).

As information analyst I am competent using Python (and its main libraries for machine learning and data science: scikit learn, pandas, scipy, numpy, matplotlib, Tensorflow, PyTorch and Keras), R language, Matlab, SPSS, Splunk and databases to transform raw data into valuable knowledge to take decisions.

Professional Goal

I want to be part of a highly qualified digital electronics design and software development team in an innovative company focused on providing high value products and services, to contribute to such enterprise with my skills, knowledge and expertise in electronic design, software development, and information analysis, and in the process found new challenges and opportunities to enhance my perspective of professional growth.

Born place and date	Mexico City. February 12th, 1975.
Professional Experience (latest 10 years)	**Senior CPU Design and Validation Engineer for Intel – Atom** (from September 2024 until today). • Validator of floating-point sets of instructions (x86 assembly and uCode for AVX10 and AVX512). • Test developer on x86 assembly + Intel's proprietary tools. • Developer of x86 microcode simulator for pre-si validation (coded in C++). **Senior CPU Design and Validation Engineer for Intel – x86s** (from January 2023 until July 2024). • Owner of Hard IPs pre-silicon validation embedded into x86s core (PLL, thermal sensor and clocks). • Owner of memory transactions simulator for pre-si validation (coded in SV and C++). • Developer of x86 microcode simulator for pre-si validation (coded in C++). • Developer of model's build automation flows (GitHub Actions, Perl, Python and Unity containers). • Developer of data mining tools to get information from large log files to find RTL and microcode bugs. **Adjunct Teacher for ITESO – Jesuit Guadalajara's University** (from August of 2023 until today). Subjects I teach : structured programming, design of data structures, operating systems, and cybersecurity and computer networks. **Senior IP Logic Design Engineer for Intel – Memory products** (from January of 2018 to December of 2022). • Senior developer of memory controller's simulator (coded in C++) for performance analysis. • Co-Designer of security features for memory controller. • Owner of GLS model of the entire memory controller (core + IO), an important tool for pre-silicon validation. • Owner of XProp utility, a useful VCS' RTL level tool for pre-silicon validation. **Adjunct Teacher for Monterrey's Institute of Technology** (from August of 2019 to December of 2020). Subjects I taught: digital systems, advanced digital systems, laboratory of advanced digital systems and computer architecture. **Senior Electrical Validation Engineer for Intel** (from January of 2016 to December of 2018). • Leader of technical validation meeting for low speed and high-speed interfaces in products of client and server segments.

Professional Experience (continuation)	• Leader of team that documented all milestones (deliverables and activities) of whole post-silicon electrical validation process. • Owner of UFS (Universal Flash Storage) and CNVi (Connectivity Integration) electrical validation for products of client segment. • Instructor and champion of statistical methods for data analysis. • Developer of communication tools to collect data from platforms and oscilloscopes and store it into a database. • Developer of scripting tools to analyze all the data collected from electrical validation test. **Senior Software Developer and Leader Engineer of Technical Support, Maintenance and Training for Clinical Analysis Equipment for Dadial Medica** (from March of 2014 to December of 2015). • Leader for Software Development, Information Services and Technical Support for clinical analysis equipment from Abbot, Coulter Beckman, Roche and Dirui. • Developer on Java (since late 2016) for Android app to deliver medical test results to patients. • Developer on Xcode for iOS app to deliver medical test results to patients.
Academic degrees and professional training	**PhD. in Sciences in Engineering with focus on IA – ITESO Jesuit University of Guadalajara.** From August of 2024 to June of 2028. **Specialization in Statistical Methods Applied to Data Science – Center for Research in Mathematics (CIMAT)** From August 2022 to July 2023 (graduated by academic excellence). **Specialization in Embedded Systems – ITESO Jesuit University of Guadalajara** From August 2022 to July 2023 (credits completed and degree work in progress: implementation of machine learning techniques in firmware to manage battery charge of low-orbit satellites). **Master's in Electronics Design – ITESO Jesuit University of Guadalajara** From 2015 to 2017. **Master of Science in Electrical Engineering with specialization in Automatic Control – Center for Research and Advanced Studies of National Polytechnic Institute (CINVESTAV-IPN)** From 2003 to 2005. **Bachelor's Degree in Computer Engineering – School of Engineering– Mexico's National University (Facultad de Ingeniería-UNAM)** From 1994 to 1999.

	Certificate on Cybersecurity – ITESO Jesuit University of Guadalajara From March 2022 to September 2022 – 120 hrs. **Certificate on PMI Method Project Management – ITESO Jesuit University of Guadalajara** From October 2021 to March 2022 - 120 hrs. **Certificate on Java's Programming – ITESO Jesuit University of Guadalajara** From 2020 to 2021 - 120 hrs. **Certificate on Programming TI DSPs and TI-RTOS – ONIK Electronic Systems** 2016 - 120 hrs. **Certificate on Programming Android's Mobile Devices – University of Guadalajara** From 2015 to 2016 - 60 hrs. **Certificate on Telecommunication's Networks – School of Engineering – Mexico's National University** From 2002 to 2003 – 240 hrs.
Languages	**English.** TOEFL ITP with a total score of 607 points. November 2019. **German (intermediate level).** Goethe Institut, Guadalajara. 2004 – 2006. **Spanish.** Native language.
Personal and professional references	**PhD. Ismael Martínez López** Full Time Researcher and former Chairman of Electrical and Electronic Engineering School of Engineering – Mexico´s National University ismartz@unam.mx **PhD. Antonio Ramírez Treviño** Full Time Researcher and former Academic Dean of Center for Research and Advanced Studies of National Polytechnic Institute art@gdl.cinvestav.mx **MI. Esdras Juárez Hernández** Senior SOC Design Engineer Intel Labs – Intel Corporation (GDC) esdras.juarez.hernandez@intel.com **PhD. José Francisco Cervantes Álvarez** Full Time Researcher and former Chairman of PhD. in Engineering Sciences ITESO Jesuit University of Guadalajara fcervantes@iteso.mx