Pranava Krishnamurthy Bhat

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Education

Masters of Science, Electrical Engineering, *Texas A&M University* 08/2024 – present | College Station, USA
Advanced Digital System Design, Computer Architecture and Introduction to Advanced Hardware Verification **CGPA: 3.7/4.0**

Bachelors of Engineering, *Visveswaraya Technological University* 08/2017 – 08/2021 | Bangalore, India
Digital Electronics, Microprocessors, Verilog, Analog electronics and Circuits, CMOS and VLSI design, Programming in C and data structures **CGPA: 8.18/10**

Skills

HDL and Design — Verilog and SystemVerilog, UVM, RTL Design and Verification.

Programming — C, C++, Python, Shell Scripting and Matlab

Tools and Technologies — Cadence Xcelium, Cadence Virtuso, Cadence Spectre, Cadence IMC, Intel Quartus, Seimens ModelSim, and Xilinx Vivado,

Certifications — System Verilog for Design and Verification, Cadence

Professional Experience

Software Engineer, *Mphasis India Ltd* 08/2021 – 02/2024 | Bangalore, India
- Worked as a consultant for FedEx as a full stack developer. Developed new Features and tools for FedEx's internal import and export scanning solution used in FedEx hubs worldwide.
- Devoloped an automated global exchange rate parsing system using python, which helped in reducing shipment sorting misses by 15 percent.

FPGA Intern, *Senpronics PVT Ltd* 03/2021 – 07/2021 | Bangalore, India
- Worked with a team of interns building a seismic data acquition system using the Altera Cyclone 2 FPGA system on the ADC-SoC board and worked on the integration of the ADC-SoC board to a Raspberry Pi for seismic data processing and transmission.

Projects

Performance Analysis of GPU Scheduling Algorithms using accelsim 01/2025 – present
- Built the experimental Light Weight Out of Order Scheduling technique designed for GPUs on the AccelSim GPU simulation framework and performed trace-driven-simulations to measure the percentage of stall cycles.

Implementation of the Static Re-reference Interval Prediction Cache Replacement Policy 10/2024 – 10/2024
- Implemented the SRRIP cache replacement policy in ZSim, a fast and accurate simulator for modelling x86 cores, using C++.
- Proceeded to measure the performance of SRRIP against other replacement policies such as LRU and LFU.
- Achieved overall improvement in IPC of 0.98 in the stream cluster benchmark, in the SPEC2006 benchmark suite.

Design of a 16 bit RISC-V processor with a 5 stage pipeline with dynamic scheduling 11/2024 – 02/2025
- Designed a 16 bit RISC-V processor with a 5 stage pipeline supporting Memory Load/Store and ALU instructions, achieving an overall speed up factor of 3.12 over an unpipelined design.
- Implemented out of order scheduling with speculation further improving speed up and reducing the possibilities of stalls.

Design Verification of a HyperTransport Advanced X-bar using UVM 09/2024 – 11/2024
- Built a complete UVM test bench complete with a virtual sequencer and sequences for the regression testing and verification of a HyperTransport Advanced X-bar, which is primarily used in multiprocessor interconnections, and tested the coverage as per the design specification.
- Achieved overall coverage of 97 percent with respect to the design specifications.

32 bit Baugh and Wooley multiplier for signed multiplication. 08/2024 – 08/2024
- Built a gate level design of a 32 bit Baugh and Wooley multiplier for fast multiplication using verilog.
- Design achieved signed multiplication of two 32-bit numbers within 5 clock cycles.

Publications

Missile Tracking using IMM and GNN
• Published a research paper, titled Missile Tracking using IMM and GNN, with IEEE in the 5th International Conference on Electronics, Communication and Aerospace Technology (ICECA). (DOI - 10.1109/ICECA52323.2021.9676032).