# Eduardo Jiménez López

Digital Design Engineer

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## Objective

8+ years of experience working on design and verification for the most innovative hardware architectures ranging from ASICs to IPUs and with different applications including graphics processing, networking, and high-performance computing.
Proven ability for RTL design, verification, and integration of large systems using state of the art methodologies, tools and techniques; collaborating cross-functionally with architecture, software, and firmware teams to identify and resolve potential issues.

## Skills

- Verilog/SystemVerilog
- Computer architecture
- Performance analysis
- Object-oriented programming
- RTL development
- C/C++
- Python
- Linux

## Experience

### Senior Design Verification Engineer
### Micron Semiconductor. January 2025 – Present

- In charge of developing and maintaining UVM based testbench for the digital and analog mixed signal verification of DRAM5 memory models aimed for the Compute market segment.
- Responsible for implementing a coverage driven methodology and functional coverage model to drive the digital verification strategy of DRAM6 memory models.

### Logic Design Engineer
### Intel Corporation. July 2022 – June 2023

- Owner of a logic block that translated data packets from a proprietary protocol into AXI4 packets and vice versa. Responsible for providing fixes and identify enhancements to improve performance of the digital block.
- Successfully integrated Media IP into an SoC platform providing guidance in floor area planning, logic gates counting, and support for critical issues that put chip tapeout at risk.

### Design Verification Engineer
### Intel Corporation. March 2017 – July 2022 / July 2023 – November 2024

- Planned and executed comprehensive unit level verification of AXI4 protocol and Address Translation mechanism in a complex digital design for high-performance interface implemented for next-generation of Xeon server chips.
- Successfully delivered complete unit level verification for Associative Cache IP. Development and review of test plan and UVM parameterized testing environment with all verification components needed, e.g. Scoreboard, BFMs, Sequence Libraries, Tests, Monitors, Coverage, etc.

## Education

### M.S. Computer Science
Tecnológico de Monterrey – ITESM
Guadalajara, Jal, MX. 2023

### B.S Electronics and Communications Eng.
Universidad de Guadalajara – UdeG
Guadalajara, Jal, MX. 2017