Summary:

Mark Zakharov is an experienced CPU Microarchitecture & Logic Design Engineer with a Master's degree in Computer Science & Engineering from the University of California, Santa Cruz. He has 4 years of experience in RISC-V ASIC development and research, including 2 years at Esperanto Technologies, a RISC-V startup. His skills include Verilog, Python, Bash, Chisel, C, C++, RISC-V ASM, DSLX, Linux, Git, Yosys, Icarus Verilog, Verilator, and RISC-V Sim and Compiler Toolchains.

Name: Mark Zakharov

Email: markzakharov1102@gmail.com

Phone: (925)-818-3586

Location: Santa Cruz, CA

Country: USA

Position Category: Design: Logic design

Desired Job Role: Senior CPU Microarchitecture & Logic Design Engineer

University: University of California, Santa Cruz

Degree: Master of Science, Computer Science & Engineering, Bachelor of Science, Computer Engineering

Graduation Year: 2024

Years Experience: 4

Notable Companies: Esperanto Technologies

Top Skills: Verilog, Python, Bash, Chisel, C, C++, RISC-V ASM, DSLX, Linux, Git, Yosys, Icarus Verilog, Verilator, RISC-V Sim and Compiler Toolchains

Job Intention: full-time

Visa Status: --

Able: no

Subject: Interest in Logic Design - Execution Unit Position

Date Sent: 02-26-2025

Resume: Yes