Nilesh S. Karnik
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Profile:

Sr. ASIC Design Engineer with several years of experience and proven technical leadership at INTEL Corporation covering various roles and responsibilities including Physical Design - Planning, Implementation, SOC Design and Integration, Tools-Flows-Methodology development & support, Pre-Si STA/SI Convergence, Quality/Reliability and Signoff, IP Logic Design (RTL) & Formal Verification, Soft-IP Qualification, PPA Estimation etc.

Objective:

Seeking Senior/Staff Engineer Full-time (Onsite/Hybrid/Remote) Role in the CPU Physical Design in Design Methodology Development, IP Qualification (PPA), Construction, Implementation, Integration, Verification, Signoff and CAD/EDA domains on IP/SOC/TFM Pre-Si Design Team at AheadComputing Inc.

Professional Experience (Starting from Most Recent):

INTEL CORPORATION (01/2001-07/2024)

IP Logic Design Engineer **07/2022-07/2024**
DCAI, Intel Corp, Santa Clara, CA

Accomplishments + Highlights

- Logic development, RTL Coding, Implementation, Integration, Formal Verification, Syn/Timing closure of DFD Features “Survivability, Response Controller, Block Arbitor Functions, Debug Error Mapping and Error Logging, Observation/Visualization Bus (VISA) and DVP Actions/Triggers” etc. for Host-IO Processor (HIOP) ® IP block and its hierarchical partitions.
- Developed scripts to generate critical observation/debug probes list based sigfiles for IP insertion, Performed detailed analysis & RTL fixes that resulted in 23% cell count reduction and associated timing improvements on implemented DFD features.
- RF/CAM HIP integration in IP and sub-partitions. Developed fast RF Integration flow to implement late changes/ecos. Performed Quality Checks on RF Interface using IP-XACT/Metadata. Implemented RF timing/design improvements and ECOs e.g.0-latency CAM x-injection issue, RTL/Timing flops etc.
- Identified Scan/DFT (at-speed/stuck-at) issues & coverage gaps vs. targets on RTL netlist, Performed SGDFT analysis and implemented changes to improve Scan-Coverage for ATPG signoff.
- Delivered Power/CGE analysis and implementation for power savings. Performed Idle/TDP power (workload) tests in PowerArtist/OnePower, FSDB quality checks, MTL fixes and RTL vs. SYN CGE improvements (PowerArtist, DC) in RTL using incremental Clock Gating, DOP duplication, Large/MBIT Sequential swaps, Identify and fix Clock Dangles, Always-On Clock RCB/LCB tieoffs.

- Developed Submodule block-agnostic R2G Top-Down Flow (Fusion Compiler, RTL-Architect) to run fast synthesis/logic placement and generate PPA results for feature growth feedback in collaboration with in-house TFM team and SNPS-AE. Added multiple improvements to in-house R2G flow for customized timing/QoR reports and Netbatch settings tuning with special Memory Class/Core reservations to expedite R2G runs for Logic/RTL owners.

Technical Lead for SIP Qualification & Design Svcs. **10/2019-06/2022**

DCAI, Intel Corp, Santa Clara, CA

Accomplishments + Highlights

- PPA Estimation and Soft-IP (SIP) Qualification Methodology/Execution/Signoff owner for 4 “High Speed IO" and Bridge IP blocks (HIOP, CXL, IOMMU, B2CXL) on INTEL Xeon HPC products.
- Performed PPA studies for new uArch features/IPC/Logic Growth. Created PPA targets in partnership with Arch/Senior Logic owners, Developed and implemented Design recipes for Area, Congestion, Utilization (wire load models), Power projections, and Critical Path Timing estimation and Design constraints for initial Synthesis, UPF and Logic Placement guidance and QoR Improvements.
- Built/verified/delivered SIP reference-designs & floorplans for IP hardening.
- Contributed to Memory Solutions (RF/CAM) Spec generation and HIP integration etc. Performed in-depth design quality and IP health checks and reviews. Documented SIP qualification findings through Design Integration guide, IP datasheets and engaged with product/customer teams after IP drops/cadence.
- Horizontal Domain Owner for Design Constraints management and Fishtail RTL Verification for IP Group (20+ Soft-IPs).
- Horizontal Domain owner for Clock MCSS/Definitions, generated and maintained clock collaterals files (MCMM constraints/exceptions/uncertainty/Guardband) for 8+ IP blocks through IP drops.
- SD-QRE liaison, drove MTBF/FIT data analysis, Performed Caliber/ERC Checks (Meta-Flops Max Freq violations) at MCMM, conducted Pre QRE handoff Design reviews and implemented solutions including VT-Swap (Cell Family vs. PPA tradeoff) for affected Blocks and worked with SOC and QRE partners for final signoff.
- Co-owner for IP Hardening (Design Svcs) on CHA/CBOX (Highspeed, IDI/Ring Bus) Block on Server SOC product on Intel 7nm. Responsible for Design Implementation SYN/APR (RTL2GDSII), STA and DFx/DFT-Scan/DFD logic implementation, Design verification, Partition Quality Reviews/Closure Checklist development and Tape in.

Complexity: High-Speed IO and CXL-IO Protocols, Hierarchical designs, ~3M+ cell instances, High-Speed, 2GHz, Multi Voltage, Multi-Clock Domains, Low-Power, 200+ RF/CAM HIP EBBs instances, Intel 10nm+++/7nm process.

Sr. SOC Design Engineer **08/2018-09/2019**
DCAI, Intel Corp, Santa Clara, CA

Accomplishments + Highlights

- Timing and DF* implementation convergence owner for "High-Speed IO Subsystem/chiplet.
- Responsible for Physical/timing/VA/UPF/Clock/IO Constraints Development, Tuning, Deployment in Design implementation.
- Performed Hierarchical integration, SYN/APR, CTS/CTMESH, STA Convergence. Drove Design Quality Reviews/Audits.
- Co-owned methodology and additional automation development with in-house EDA/TFM teams for aforementioned IO subsystem.

Complexity: ~5M cell instances, High Speed 2.5GHz, Multi-Power Plane, RF/CAM EBBs, CTS/CMESH, DF*, PPA Estimation, Design Planning/Construction/Convergence, Late RTL/Design ECOs and Sign-off/VTI on Intel PDK 10nm+++ process.

Engineering Manager **06/2014-07/2018**
CCG, Intel Corp, Folsom, CA

Accomplishments + Highlights

- FLM, directly managed team of 6 Engineers (4 EEs, 2 Interns) for 4 years, responsible for planning team's deliverables/assignments and Career growth Initiatives/Opportunities.

Sr. SOC Timing Convergence Engineer **06/2014-07/2018**
CCG, Intel Corp, Folsom, CA

Accomplishments + Highlights

- Contributed to SOC/Subsystem Timing Tech Readiness, PV Guardband/BinSplit Definition, MCMM analysis, UPF-Low-Power Intent Constraints evaluation for timing; Repeater Planning, Feedthrough delay estimation and TFM improvements on Client CPU/SOC products.
- Built/Analyzed FC Timing/Hyperscale models, Reviewed/Solved timing violations & drove timing feasibility for Arch/Critical/XPV paths & provided RTL/SD feedback; Generated and Implemented Timing ECOs, Performed PTPX /Low-Power analysis.
- Defined and Drove Design Quality/Calibre/ERC checks (Transition/MaxCap) for sign off.

Sr. Component Design Engineer - Physical Design **10/2010-05/2014**
CCG, Intel Corp, Folsom, CA

Accomplishments + Highlights

- Responsible for enabling multi-core modular Physical and Timing Hierarchical Integration on SOC products. Contour owner for weekly design collateral Rolldown/Rollup (FC/Partition) cadence to enable construction milestones on Synthesis/APR blocks.
- Owner of Full chip Backend Netlist Generation/verification.
- Drove Backend clocks definition; timing-specs planning for interfaces like IOSF, Side Band, PMA & bottom-up timing integration (SPEC/ETM - LIB); DFD/DFT (VISA/ DVP/ TAP / HTI / Northpeak / MBIST) interface planning, Integration & convergence.

Design Automation Engineer - Physical Design **01/2002-09/2010**
CCG, Intel Corp, Folsom, CA

Accomplishments + Highlights

- Developed, maintained, supported and managed in-house automated PNR CAD tools, design flows+systems.
- Delivered integrated solutions combining industry leading physical Design tools + Intel automated CAD solutions (TFM) for Client CPU with focus on highly advanced and complex chip layout planning-routing-assembly-integration-verification.

Focus on: RTL2SD, Floorplan Assembly, Integration, Place and Route, RLS, Timing/Repeater Insertion, DFM, Layout Verification tools/flows and related methodologies at Block/Partition/Sub-system/SOC-Level etc.

Graduate Intern/Co-Op – System Design & Emulation Engineer **01/2001-12/2001**
Flash Products Memory Group, Intel Corp, Folsom, CA

Accomplishments + Highlights

- As part of Flash Architecture and Systems Maintenance (FASM) team, was responsible for System Design and Emulation work, developing BFM-HDL Models and writing Testbenches (sverilog) and testing for StrataFlash (NOR) Flash Memory codenamed “Trumbull” ® product in INTEL ETOX flash memory family of products.
- Also contributed to building and testing Hardware Emulators (FPGA and DRAM based) and System Boards for memory system design, compiling, configuring and debugging purposes.

Skills and Knowledge - Design Tools-Flows-Methodology-EDA

- **Protocol/Standards:** PCIE, IOSF, GPSB, USB, Host-IO, CXL-IO, JTAG, DFD-VISA (Familiarity)
- **Logic Design/Implementation**: VCS, Verdi, Fishtail, RTL-Architect, GIT-Hub, Gatekeeper.
- **Formal Verification/Debug Tools**: FEV-Conformal, SGDFT, SG-LINT/VC-LINT, SG-CDC/VC-CDC, VCLP (SNPS) etc.
- **Functional Verification**: Trex/Simregress, familiar with UVM method and test plan generation.
- **IP-SOC Handoff & Integration**– CoreTools (SNPS), SoCBuilder, DeFacto, IPXACT, IPX.
- **FC Design Flows and Methodologies** –Design Rollups/Rolldowns and SOC/ Partition handoff, FC Timing spec/bottom-up/hyperscale/ETM verification timing model builds (MCMM, XPV, DMSA), BE Clocks – Definition & Clock Constraints Generation.
- **Partition Design Flows** – RTL2GDSII, SDP
- **Physical Design Implementation/Quality Tools** – Physical Design Planner (PDP –Cadence), DC, Fusion Complier, ICC/ICC2, Fishtail (Synopsys), Calibre (Siemens), Galaxy, Parade (INTEL)
- **Extraction, PV, STA** – Carmel, APV and Tango (INTEL), Star-RC/Primetime/PTPX/PTLR (SNPS)
- **Languages** – SystemVerilog, PERL, TCL/TK8.5, SHELL/SED/AWK, Make and Familiar working with Python.
- **Indicators/tickets** – Splunk, LIRA, JIRA, HSD-ES
- **Platforms/OS** – UNIX, Linux and Windows Platforms.
- **Statistical Analysis & Database** - SQL, VB+, Excel Macros, VLOOKUP, JMP etc.
- **Misc** - HTML, MS Project, MS-VISIO, OneNote, Photoshop.

Education, Research and Papers/Publications (Most Recent to Past)

- MSEE (VLSI) – California State University, Sacramento CA (2001)
- BSEE (Electronics) – Mumbai (Bombay) University, India (1999)
- Diploma in Industrial Electronics (associate degree) –Mumbai (Bombay) University, India (1996)

- "*Auto Floorplan: RTL drop to floorplan in one day"* paper/poster – Victoria Kolesov, Nilesh Karnik et.al. (INTEL), published and presented at Design Automation Conference, 3-5 June 2013, Austin TX
- "*Ivybridge® Chop Methodology*" paper – Nilesh Karnik, Seema Shafajoo, et.al INTEL, published and presented @ DTTC, INTEL internal conference, August 2012, Portland OR
- "*Design, simulation and experimental study of near-field beam forming techniques using conformal waveguide arrays*, N.S. Karnik R. Tulpule et.al., IET Microwaves, Antennas & Propagation, February 2010, 4(2), 162–174." Published. (Won Best paper award at 2012 IET Microwaves, Antennas & Propagation Premium Achievement Awards Conference, London, U.K.)
- "*Smart Cut – Dual to Single: Penryn® Single Core Layout Methodology*" - Kalapi Royneogi, Nilesh Karnik et.al. (INTEL), published at DTTC, INTEL internal conference, July-August 2008, Portland OR.
- "*Conformal K-band 5 element wave guide array for near field applications*" paper – Nilesh Karnik, Dr. B.P. Kumar and Dr. G.R. Branner, published and presented @ IEEE-APSI International Symposium, July 2001, Boston, MA.

Strengths

- Independent technical contributor, strong abilities to self-ramp on new technologies, methodologies and immediate contributions, Excellent Automation skills, scripting debug and provide problems analysis, solutions & improvements for Design productivity.
- Ability to work across x-sites teams on demanding schedules across different geographical locations and time-zones (Austin, Bangalore, Chandler, Fort-Collins, Hudson, Haifa-Israel, Penang, Portland, Santa-Clara etc.)
- Excellent communication skills & working valued networking/partnerships with colleagues across Industry.
- INTEL-University certified instructor for INTEL DTS/PESG FC in-house layout tools (Parade, Galaxy), provided classroom and virtual training to 50+ layout engineers in multiple x-site design teams.
- Outstanding coaching/mentoring skills – provided technical leadership and mentorship to several Jr. Engineers, Interns/Coops, responsible for hiring/coordination at INTEL.
- Ability to lead a small taskforce and/team (have previously directly managed team of 6 EEs at INTEL).
- Managing at Intel (MAI) and LEAD (INTEL-University) courses certified.
- Active contributions on various technical forums, working groups and virtual teams (SoC PV Methodology & Solutions, Physical Design Integration Methodology, SIP Qualification-PPA etc.) within INTEL and outside Industry.

References available upon request.