Summary:

Accomplished silicon design professional with over 12 years of experience managing SoC IPs for Intel Server product line. Successfully delivered multiple ASIC tape-outs by driving execution across cross-functional teams, managing risk, and ensuring milestone alignment. Adept at program planning, stakeholder coordination, and technical execution oversight in complex ASIC development programs.

Name: Mini Aggarwal

Email: agr.mini@gmail.com

Phone: 646-942-0535

Location: 10810 167th Ave NE, Redmond, WA 98052

Country: USA

Position Category: Design: Physical Design

Desired Job Role: Physical Design Lead

University: Illinois Institute of Technology (IIT), Chicago, IL, Bangalore Institute of Technology, India

Degree: M.S, Electrical Engineering, Bachelor of Engineering, Electronics and Communications

Graduation Year: 2007, 2004

Years Experience: 12

Notable Companies: Intel

Top Skills: Technical Expertise - Physical Design, Floorplanning, STA, Timing Closure, Low-Power Design, Program Management Project Planning, Risk Mitigation, Agile/Waterfall Execution, Silicon Development Lifecycle RTL to GDSII, Tape-Out, DFT, Stakeholder Communication Executive Reporting, Milestone Tracking, Resource Planning, Cross-Functional Leadership Coordination across design, verification, layout teams, Vendor & Partner Engagement Foundry (TSMC, Intel), EDA (Synopsys, Cadence), IP Integration

Job Intention: full-time

Visa Status: --

Able: no

Subject: Resume for Physical design roles

Date Sent: 04-22-2025

Resume: Yes