Summary:

Pre-Si verification engineer with 15 years of experience. Proficient in leading engineers on all stages of the validation, as well as providing coaching for professional growth. Capable of switching contexts and can work on multiple areas of the project, as well as collaborating across teams to achieve milestones.

Name: Enrique Nezahualpilli Perez Moreno

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Phone: +523337241626

Location: Zapopan, Jalisco, Mexico

Country: Mexico

Position Category: Verification: Design verification

Desired Job Role: CPU Design Engineering Manager

University: Instituto Tecnologico y de Estudios Superiores de Occidente, Universidad de Guadalajara

Degree: Specialty program in Integrated Circuit Design, Bachelor of Electronics and Communication Engineering

Graduation Year: 2010, 2008

Years Experience: 15

Notable Companies: Intel Tecnologia de Mexico S.A. de C.V.

Top Skills: Pre-Si verification, UVM, x86 verification, IP integration, Security IP verification, GLS verification, SMBUS verification, DFx logic verification

Job Intention: full-time

Visa Status: --

Able: yes

Subject: Working at AheadComputing

Date Sent: 02-23-2025

Resume: Yes