Blake Buschur

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16100 SW Century Dr. APT 188, Sherwood, Oregon 97140

EDUCATION

Master of Engineering in Computer Engineering, *University of Cincinnati* August 2018
Bachelor of Science in Electrical Engineering, *University of Cincinnati* May 2016

PROFESSIONAL ENGINEERING EXPERIENCE

Intel | Formal Verification Engineer | Hillsboro, Oregon March 2022 - Present

- Created and executed formal verification test plans by collaborating with architects and RTL design engineers for 5+ sub-components of the Intel Xeon CPU
- Used JasperGold to verify the functional correctness of various RTL designs including: deadlock, starvation, forward progress, data integrity, routing, ordering, arbitration, and clock gating
- Created reusable and scalable proofs allowing for quick verification and bug detection of next-gen components
- Reviewed test plans and SystemVerilog code, oversaw execution, and provided technical leadership for 5 sub-components of a cache coherency system
- Maintained top-tier quality by debugging and fixing 1000s of unreachable coverpoints, integrating formal properties into simulation environments, and achieving 99%+ Proof Core coverage
- Developed efficient test strategies utilizing abstraction techniques (parameter reduction, black-boxing, free variables, credit abstractions) to resolve unproven assertions, reduce runtime, and improve bug detection
- Collaborated with security teams to identify areas suitable for security properties; implemented and verified those properties using JasperGold Formal Property Verification (FPV) and Security Path Verification (SPV)
- Adapted under resource constraints (team attrition, tight deadlines) by reprioritizing tasks, cross-training team members, and completing deliverables without compromising quality

Edaptive Computing Inc | Senior Hardware Verification Engineer | Dayton, Ohio June 2018 - March 2022

- Worked as the formal verification tech lead; researched new formal verification techniques, created technical goals and roadmaps for new tools, and designed verification test plans for new hardware designs
- Led 3-day technical formal verification trainings to outside customers using the OneSpin formal verification tool
- Managed, mentored, and trained 5 junior formal hardware verification engineers
- Acted as the Primary Investigator for SBIR Phase I contract; researched technical areas, created the product solution and technical whitepaper/proposal, facilitated meetings with customer, and collaborated with subcontractors
- Implemented an improved verification test plan utilizing 6 formal verification tools by reviewing the design specifications of various RTL designs (communication interfaces, interconnects)
- Formally verified a RISC-V SoC for tape-out by using automated checks and debugging the design
- Certified various hardware designs using SystemVerilog and PSL assertions to analyze and debug
- Acted as product owner of a customer-facing GUI hardware verification app
- Reduced the verification setup time by 95% through automating the process using TCL scripts
- Facilitated a team of 11 as the scrum master using the Agile Development Process
- Helped in the recruitment process by reviewing resumes and giving technical interviews to 20+ job candidates

Weld Plus Inc. | Electrical Engineer | Cincinnati, Ohio November 2016 - November 2017

- Increased weld throughput by 150% by integrating cutting-edge laser technology with out-of-date equipment

Meiban Group Pte Ltd | Electrical Engineering Co-op | Singapore, Singapore June 2015 - August 2015

- Gained a valuable cultural experience working with individuals and groups from Singapore

Skills

Formal Verification, JasperGold, OneSpin, CPU Verification, Cache Coherency, SystemVerilog, Revision Control Systems (Git), TCL, RTL, SystemVerilog Assertions (SVA), Agile Software Development, Scrum