MINI AGGARWAL

agr.mini@gmail.com

10810 167th Ave NE
Redmond, WA 98052

Mobile: 646-942-0535

SUMMARY

Accomplished silicon design professional with over 12 years of experience managing SoC IPs for Intel™ Server product line. Successfully delivered multiple ASIC tape-outs by driving execution across cross-functional teams, managing risk, and ensuring milestone alignment. Adept at program planning, stakeholder coordination, and technical execution oversight in complex ASIC development programs. Known for delivering high-quality, innovative solutions and driving designs from concept to completion for multiple generations of products. Passionate about silicon program management, bridging the gap between engineering and business objectives to ensure silicon success.

SKILL SET

- **Technical Expertise** - Physical Design, Floorplanning, STA, Timing Closure, Low-Power Design
- **Program Management** – Project Planning, Risk Mitigation, Agile/Waterfall Execution
- **Silicon Development Lifecycle** – RTL to GDSII, Tape-Out, DFT
- **Stakeholder Communication** – Executive Reporting, Milestone Tracking, Resource Planning
- **Cross-Functional Leadership** – Coordination across design, verification, layout teams
- **Vendor & Partner Engagement** – Foundry (TSMC, Intel), EDA (Synopsys, Cadence), IP Integration
- Self-driven with strong analytical and problem-solving skills, effective in fast-paced, team-oriented environments.

WORK EXPERIENCE

Silicon Design Lead, Xeon Engineering Group, Intel™ — Aug 2016- Present

Sr. Physical SoC -Subsystem Design Lead

- Currently leading design and integration of a complex >2.5million gate multi-voltage core tile subsystem on Intel's leading-edge technology node for next generation Server SoC product.
- Led a team of five, ensuring milestone alignment and risk mitigation through daily stand-ups and iterative execution cycles.
- Managed sprint planning, defining priorities, and managing critical paths to ensure predictable outcomes.
- Collaborated closely with Soft IP and Hard IP teams to align on specs and maintain highly time sensitive schedule.
- Technical expert and mentor guiding junior engineers through complex design challenges

Physical Design Lead Intel™ Xeon 6 (E-core) Server

- Led physical integration and convergence of DDI Subsystem for Intel™ Xeon 6 (E-core) Server product on Intel 3 process node.
- Collaborated with physical layout team during the early stages of the design phase to identify and mitigate critical floorplan-related issues affecting multiple designs across sub-systems
- Spearheaded a workgroup to drive last-mile convergence work, identifying unique design issues and defining optimized strategies for timely and efficient design closure.
- Communicated status to senior management by monitoring milestones and highlighting progress, risks and providing mitigation plans.
- Orchestrated a cross-functional team of engineers and tool developers for preparing design recipes to consume late breaking logical bugs with minimum disruption to project schedule and design quality.

MINI AGGARWAL

agr.mini@gmail.com

10810 167th Ave NE
Redmond, WA 98052

Mobile: 646-942-0535

- **Product Development Engineer, Software Solutions Group, Intel™ WA Aug 2015- July 2016**

    - Defined technical requirements for software development platforms (SDP) as the technical lead for client desktop and high-performance mobile segment.
    - Interfaced with cross-functional and cross-site teams including client business unit and suppliers to influence the next generation SDPs.
    - Translated stakeholder requirements into tangible hardware solutions to meet the needs of internal engineering teams and external independent SW vendors, OS vendors to develop and optimize operating systems, applications and tools that differentiate IA in the marketplace.

- **CPU Physical Design Lead, Xeon PHI Server, Intel™ OR Feb 2008- July 2015**

    - Led physical design convergence of Vector Processing IP with over 1 mil gates running at more than 3Ghz for Intel Xeon PHI Server line.
    - Used cutting edge methodology for sub-IP integration to reduce the overall physical design convergence effort by over 30%.
    - Achieved >9% performance boost on silicon for aggressively driving power reduction during project metal stepping.
    - Met best case schedule with cross-disciplinary teams of architects and logic designers to deliver a production quality design meeting design specification on a best-case schedule.
    - Resolved partition congestion issues thorough floorplan analysis, utilizing understanding of architectural data flow in collaboration with logic design team.

EDUCATION

Illinois Institute of Technology (IIT), Chicago, IL	Dec 2007
M.S, Electrical Engineering	G.P.A: 3.7/4.0
Bangalore Institute of Technology, India	May 2004
Bachelor of Engineering, Electronics and Communications	G.P.A: 3.7/4.0