Tapas Sastry

Results-driven electrical engineer with 7+ years of experience in RTL design, integration, and optimizing execution through automation.

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WORK EXPERIENCE

Intel Corporation
SoC Design Engineer

12/2018 - Present *Hillsboro, OR*

- Front-end RTL design lead for chip subsystems, delivering all milestones from architectural spec to tape-in.
- Logic design + constraints for designs with custom high-speed and lossless async protocols developed in-house.
- Dictating methodology and coding guidelines to ensure smooth and predictable execution for RTL work including design, handoff, timing closure and GLS.
- Creating an efficient test and release environment to ensure bugs are caught before handoff to verif/SD teams. Improved execution efficiency by 80% for rapid tape-in cycles.
- Driving enablement and debug on tools/flows/methodology for project execution. Set standards and audited QC for RTL, UPF, SDC using Lint, CDC/RDC, LP, Synthesis and LEC tools.
- Successfully taped in several projects, including Xeon products and iterations of an ultra-low power chip with cutting edge power saving techniques.
- Mentor and organizer for intern program, providing job training for interns and recent college grads through effective documentation.

Intel Corporation
Technical Intern

06/2017 - 12/2018 *Hillsboro, OR*

Long-term internship, June-Sept 2017, April-Dec 2018

- Developed SoC RTL for an AI processor, SubSystem RTL for 11th Gen Intel Core processor.
- Responsible for FE RTL assembly and tools/flows - Lint, CDC, LEC, Synthesis checks.
- Automated quality checks using Perl/Shell/TCL scripts.

Portland State University
Lab Instructor - ECE Labs

01/2017 - 04/2018 *Portland, OR*

- Guided EE students with their term project: design and construction of a custom Op-Amp (ECE 322).
- Instructed students on BJT/MOS based design, Spice modeling/simulations and circuit builds (ECE 322, ECE 222 and ECE 101).
- Mentored junior EE/CE major students to fine tune their technical skills and with general schoolwork.

TECHNICAL SKILLS

RTL Design + Integration | Scripting - Perl / Python / TCL / UNIX | Verilog / SystemVerilog | Tools / Flows / Methodology | Efficient Execution | Synopsys / Cadence Tool Suite | FE to BE Handoff | Gate-level Simulation

EDUCATION

B.S. Electrical Engineering
Portland State University

09/2015 - 12/2018

- Outstanding Undergraduate Student Award 2016-17
- President's List - Spring 2016 Term
- Dean's List - Fall 2016, Winter 2017, Spring 2017