# Adithi S Upadhya

Atlanta, Georgia 30308
470-530-7680 adithi.u7@gmail.com linkedin.com/in/adithi-su github.com/adithi-su

## Education

**Georgia Institute of Technology** **April 2025**
*MS in Electrical and Computer Engineering, GPA: 3.75* *Atlanta, Georgia*

**National Institute of Technology Karnataka** **May 2023**
*B.Tech in Electronics and Communication Engineering* *Mangalore, India*

## Relevant Coursework

Advanced Computer Architecture, Computer Organization & Architecture, Hardware/Software Co-design for ML, Digital System Design, Microprocessors, VLSI Design/CAD, Low-Power VLSI Design, Parallel Programming for FPGAs, Physical Design Automation

## Experience

**Samsung Austin R&D Center** **May 2024 – Dec 2024**
*GPU RTL Design Intern* *Austin, Texas*

- Implemented System Verilog Assertions for critical interface timing, enhancing signal synchronization and detecting power-related bugs in GPU architecture.
- Optimized power efficiency through strategic clock gating and PTPX analysis.
- Engineered RTL feature in texture subsystem for masked data write-back to Shader and aided in the development of directed tests to enhance verification coverage, expanding stimulus generation for comprehensive design validation.
- Created Python scripts to run Lint and Formality.

**Intel** **August 2022 – Jan 2023**
*RTL Design Intern* *Bangalore, India*

- Used FW-build-IDE of the CPU, to compile and build binaries for C code, and ran them on Verilog simulations. C-code for performance evaluation of CPU's load/store was written, built and simulated on Verilog platform.
- Performed simulations using a basic AXI initiator agent to assess the fundamental functionality of the SRAM controller IP.

## Projects

**End-to-End Framework and Simulator for Systolic Array** | *Verilog*

- Developed custom RTL for GEMM operations based on a Systolic Array architecture, processing input from a PyTorch model.
- Implemented a parameterized dense systolic array (output stationary dataflow) featuring a PE Grid, Controller, SRAM Banks, and Instruction Reader.

**Superscalar Pipeline with Branch Prediction** | *C++*

- Implemented data dependency tracking, data forwarding and related stalls for a N-wide Superscalar.
- Integrated the pipeline design with perfect and GShare Branch Prediction.

**CMP Memory System Design** | *C++*

- Designed and implemented a multi-level cache system with separate L1 instruction and data caches (32KB), and a unified L2 cache (1MB) and DRAM (16 banks, row buffer).
- Utilized 64-byte cache lines for efficient data transfer and spatial locality exploitation and LRU replacement policy to optimize temporal locality.

**VLSI Design using Openlane** | *Verilog*

- Executed RTL to GDSII flow for 16-bit counter with Openlane using Skywater130nm PDK. Performed design exploration and used regression to find the best set of parameters (Gate count: 50, Are: 391.63$\mu m^2$, Delay: 865.79ps).

## Technical Skills

**Languages**: Verilog, System Verilog, Python, ARM v7, MIPS and RISC-V ISA
**Developer Tools**: Cadence Virtuoso, Cadence Innovus, Synopsys Verdi, Vivado, Synopsys PrimeTime PX, Matlab, ModelSim, LT Spice, NG Spice, MAGIC VLSI, Keil Vision, OpenLane, Arduino, Git, Linux

## Achievements

- Recipient of the **2021 APAC Generation Google Scholarship: for women in Computer Science**, formerly known as Women Techmakers Scholarship.