Venkata Ramana Molabanti

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OBJECTIVE: Seeking **Full time** in Digital Design Verification/Emulation starting **February 2025**

EDUCATION

M.S., Electrical and Computer Engineering **GPA: 3.6/4.0**
Portland State University, Portland, OR **Dec'24**
Coursework: Intro to System Verilog, Microprocessor System Design, Computer Architecture, Pre-silicon Validation, Assertion Based Verification, Computational Tools, Emulation and Functional Specification Verification

B.Tech., Electronics and Communication Engineering **GPA: 8.0/10**
Vignan's University, INDIA **Aug'21**

TECHNICAL SKILLS

Programming Languages : System Verilog, Verilog, Python
EDA Tools : QuestaSim, VSCode, SynopsysVCS
Verification Methodology : Universal Verification Methodology **(**UVM), Assertion Based Verification (ABV)
Emulation Platform : Veloce, Z2
Protocols : I2C
Skills : Cache Coherence, Virtual Memory, Pipelining, Branch Predictions, DDR, RAM, SRAM, MIPS, Coverage, OOPS, Interfaces, Verification Plan, TBX, DPI-C, SCEMI PIPES, XRTL, Inferencing Algorithms

WORK EXPERIENCE

Advanced Micro Devices (AMD, USA, Austin) **Aug'24 – Dec'24**
Platform Emulation Intern

- Performed the NPU validation at SoC level using emulation to ensure the functionality in Pre-silicon stages
- Executed various test cases which include inferencing, security, and power tests by integrating models and firmware components on Cadence Z2 and Veloce emulators to validate NPU performance
- Managed post-execution activities, debugging the issues through log analysis and waveform inspection
- Developed XML-based scripts for automating the system-level tests and reducing manual effort

ACADEMIC PROJECTS

Design and Verification of Asynchronous FIFO [UVM-QuestaSim] **Mar'24**

- Implemented Asynchronous FIFO to operate at the desired frequency for both read and write operations
- Design is verified by both class based testbench and UVM based testbench
- Multiple test cases had been written to check the design's functionality and achieved 82.6% of code coverage

Design and Verification of a memory subsystem using I2C [SystemVerilog-QuestaSim] **May'23**

- Simple I2C protocol is designed and integrated with a functional unit and a memory controller
- Utilized a class-based testbench featuring randomization, coverage analysis, assertions, and interfaces

Data Path Controller based Memory model [ABV-VC Formal] **Dec'23**

- Sequence Equivalence Checking and Formal Property Verification is used to validate different modules in design
- Assertions and Assumptions created for the memory model to validate the behavior of the design

Designing Three Level Adaptive Branch Predictor [C++-VSCode] **Dec'23**

- Developing a three-stage adaptive global history branch predictor for a superscalar processor
- Created and used multiple traces as benchmarks which include gcc, jpeg etc.
- Compared this technique with multiple branch predictors like bimodal and gshare and achieved 84% of similar prediction rate

Simulation of 5-stage pipeline MIPS Lite Architecture [Python] **Mar'23**

- Simulated behavior of MIPS architecture without pipeline and with pipeline (forwarding and without forwarding)
- Forwarding reduces stalls by approximately 89.17% and improves execution time by about 28.94% compared to without forwarding

PUBLICATION

- A technical research paper on YOLOV3 based Real Time Drone Detection for Counter Drone System and published under "IEEE" publications 10.1109/TEMSMET56707.2023.10149935