Summary:

Accomplished Physical Design Engineer with a masters degree and over 9 years of experience in pioneering technology projects. Expertise in ASIC design, clock tree implementation, and verification methodologies. Proficient in STA, including developing timing constraints and executing top/blocks level timing ECOs for closure. Skilled in the Synopsys suite and experienced with technology nodes ranging from 180nm to 3nm across various foundries.

Name: Nicte-Ha Reyes

Email: anictereyes@gmail.com

Phone: +52-3316232839

Location: Mexico

Country: Mexico

Position Category: Design: Physical Design

Desired Job Role: Staff Physical Design Engineer CPU PPA Optimization

University: INAOE, Puebla-Mexico, ITM Morelia Mexico

Degree: M.S Integrated Circuit design, Electronic Engineer

Graduation Year: --

Years Experience: 9

Notable Companies: Synopsys Inc., Intel Labs., Intel Company, Freescale Semiconductor

Top Skills: ASIC design, clock tree implementation, verification methodologies, STA, Synopsys suite, Cadence suite, TCL SHELL scripting

Job Intention: full-time

Visa Status: --

Able: no

Subject: Working at AheadComputing

Date Sent: 03-25-2025

Resume: Yes