Supreet Gulavani

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Skills

Protocols & Architectures: UART, I2C, SPI, PCIe, ARM, PIC, x86, RISC-V, Xilinx FPGAs, Lattice FPGA
Software: C, C++, Python, SystemVerilog, UVM, RTL, Bash, GDB, Makefile, Git, RTOS, Linux, Driver development, SV Assertions
Hardware: Oscilloscope, Logic Analyzer, Board Bring-up, Soldering, Hardware Debuggers, Schematic reading

Work Experience

HP (Contract Worker) **May 2024 - Feb 2025**
Firmware Engineer Spring, TX

- Performed hardware bring-up by writing Verilog RTL on Lattice's CertusPro-NX FPGA to test different IPs
- Collaborated on creating a project plan for a m.2 form factor PCIe Gen3-based debug tool
- Developed a DMA engine in Verilog to perform read/write transactions over AHBL and AXI via PCIe Gen3 X4
- Created documentation for the software team to develop applications over the DMA engine
- Successfully integrated the ADC IP module, enabling real-time on-die junction temperature display
- Assisted in verifying schematics for tape-out

Intel Corporation **Oct 2022 - Jun 2023**
Firmware (BIOS) Developer Intern Hillsboro, OR

- Ported over 20 test cases onto upcoming CPU platforms enhancing the CI/CD environment for more automated testing
- Resolved Slim Bootloader build script bugs for improved efficiency and reliability
- Created open-source documentation to ensure accuracy and consistency, minimizing discrepancies
- Developed structured documentation for internal processes, promoting clarity and organization within the team
- Performed code cleanup and refactoring for Intel's open-source Slim Bootloader resulting in improved readability
- Authored a whitepaper on Slim Bootloader showcasing the capabilities and advantages to the team and clients
- Generated maintenance release packages with Yocto, Windows, and UEFI payloads

NXP Semiconductors **June 2022 - Sep 2022**
DFT Intern Austin, TX

- Developed a custom tool to automate test analysis from ATPG reports, improving test coverage and saving time
- Acquired knowledge of advanced DFT methodologies, including SCAN, ATPG, and MBIST
- Contributed to subsystem-level IJTAG regressions to improve test coverage

Projects

Verification of Rojoblaze **May 2022 - June 2022**
ECE593 Project

- Created a verification plan with black box and grey box testing methodologies for an 8-bit microcontroller with a 4-stage pipeline
- Developed a testbench environment with a BFM, generator, driver, monitor, and scoreboard covering the concepts of OOP
- Wrote a Makefile to feed random test cases, and gather functional and code coverage reports of 65% and 68% respectively

RISC-V ISA Simulator **Feb 2022 - Mar 2022**
ECE586 Project

- Designed a simulator in C++ to parse a memory image file to decode and execute instructions
- Implemented RV32 Base Integer instruction set, multiply extensions, ecall and ebreak system calls
- Incorporated single-step and multiple breakpoint functionality for precise debugging using RV- GNU

DDR4 DRAM Memory Controller **Nov 2021 - Dec 2021**
ECE585 Project

- Developed a simulator in C++ to parse input requests, utilizing queues and command processing logic to ensure accurate output and efficient system performance
- Implemented in-order, first ready first access, and out-of-order scheduling policies, adhering to the timing parameters
- Created exhaustive test scenarios to verify DRAM timings and the robustness of the simulator

Education

Portland State University **Sep 2021 - Jun 2023**
Master of Science, Electrical and Computer Engineering Portland, OR

Savitribai Phule Pune University **Aug 2016 - May 2020**
Bachelor of Engineering, Electronics and Telecommunication Pune, India