# Cheng-Hao Hsiao (Harry Hsiao)

+1 984 379 1874 | harry.chenghaohsiao@gmail.com | https://chenghaohsiao-harry.github.io

Computer Engineering student seeking an internship to apply expertise in architecture, design, and verification

## EDUCATION

**North Carolina State University**, Raleigh, NC, USA — Aug 2024 - May 2026
*First-year Computer Engineering master's student* — *Overall GPA: 4.0/4.0*

**National Taipei University**, New Taipei, Taiwan — Sept 2022 - Jan 2024
*Bachelor of Science in Electrical Engineering* — *Overall GPA: 3.5/4.0*

## SKILLS

- Languages: Verilog, SystemVerilog, C++
- Tools: ModelSim, QuestaSim, Vivado, Xilinx ISE, Klayout, Design Compiler/Vision, Innovus, mflowgen

## PROJECTS

**Verification of I2C Multiple Bus Controller with Wishbone Interface(ongoing)** — April 2025(expected)

- Creating a test plan and verifying DUT with functional coverage, code coverage, and assertions
- Developed UVM-like layered testbench including generator, driver, monitor, scoreboard, and coverage
- Designed an I2C slave Bus Function Model(BFM) to support all test cases in the test plan

**Value Predictor for Performance Optimization in RISC-V Superscalar Processor** — April 2025

- Addressed data dependency bottlenecks by designing a Stride Value Predictor under a 32KB storage budget
- Developed a pipeline structure with prediction injection, misprediction detection, and a recovery mechanism
- Improved Instruction Per Cycle(IPC) by 6.8% through the implementation of a blacklist mechanism

**Out-of-Order Superscalar Processor with Physical Register Architecture** — Feb 2025

- Designed a full-scale RISC-V superscalar processor with rename, dispatch, execute, and writeback stages
- Managed physical register file with active list, free list, rename map table, and architectural map table
- Solved branch misprediction recovery and selective squash issue by using a checkpoint and GBM
- Verified design through simulation with industry-standardized SPEC CPU 2006 & 2017 benchmark suites

**Dynamic Instruction Scheduling** — Dec 2024

- Developed an out-of-order(OOO) superscalar processor simulator with a nine-stage pipeline architecture
- Built configurable Rename Map Table(RMT), Issue Queue(IQ), Reorder Buffer(ROB), and function units
- Analyzed Instruction Per Cycle(IPC) with 10,000 instruction tests, varying IQ, ROB, and bundle sizes

**Cache Coherence Protocol Simulator for Multi-Processor System** — Nov 2024

- Applied MESI/MOESI protocols for data consistency in a 4-processor snoop-based multiprocessor system
- Analyzed the performance by tracking memory transactions, cache-to-cache transfer, miss rate, and latency

**Configurable Matrix Multiplication for Transformer Attention Equation** — Nov 2024

- Designed a deeply pipelined architecture for multiplying five matrices, including one transposed matrix
- Optimized performance by fetching data in transposed order, eliminating overhead of explicit transposition
- Achieved 217 computations in 1,213 cycles with a 5.5 ns clock and 10,771 μm² area, ranked 23/180 in class
- Executed synthesis, place-and-route(PNR), DRC, and LVS, culminating in GDSII generation for tape-out

**Branch Predictor Simulator** — Nov 2024

- Developed a hybrid branch predictor that combines Gshare and Bimodal branch predictor
- Built a Branch History Table and prediction table to document the actual branch outcome and Smith counter
- Analyzed prediction accuracy by adjusting table size and history length, successfully passing a 2M data test

**Configurable Cache and Memory Hierarchy Simulator** — Oct 2024

- Developed a flexible cache simulator supporting size, associativity, block size, and cache level adjustments
- Implemented Write-back Write-allocate(WBWA) and Least-Recently-Used(LRU) replacement policy
- Analyzed cache Average Access Time (AAT) performance by executing 10,000 virtual addresses per test