M.Sc. Eliseo Torres Casales

Zapopan, Jal. Mexico
Cell: +52 3310553261
ecasales@gmail.com

Summary: VLSI AMS engineer with experience in Design, Verification and Silicon Validation of Serdes, DDRphy and high speed blocks. Hands on expertise in Analog and Physical design flows from concept to GDSII.

Hands-on experience in all aspects of the AMS IP and circuit design. From architecture, design, layout implementation, technical supervision, schedule and execution management, Change Control Board analysis and implementation, Physical Verifications, GDSII Tape-out among others. Responsibilities include Silicon Compliance and post-product customer support.

Mentored and managed design teams locally (Mexico) and remotely (India). Full experience working with cross-functional teams worldwide in several countries and locations. Emphasis on quality assurance and delivery on time to exceed customer expectations.

Professional Experience:

Physical Design Engineer (Intel) **2024 – Current Date**

Physical design of UCIe interfaces in Intel advanced technologies. Full APR flow execution and verifications. Adhered quickly to the Intel flows and methodologies to support the projects under execution.

Technology readiness study for architecture implementation from Synthesis to GDS. Evaluation and implementation of floorplan, timing, physical verifications like LVS/DRC, reliability, etc.

Physical Design Architect (Wipro Technologies) **2017- 2024**

Working on design services for different customers around different locations. Demonstrated quick ramp-up on their design architectures and adhered and understood the design flows and in-house tools that each customer require.

Relevant Projects:

Design Lead of multiprotocol SerDes IP development and Silicon Validation for NXP for several families of microcontrollers from 1.25G to 25G.

- Mentored and managed a team of 10 analog design, physical design and Digital verification designers in Guadalajara. Followed up execution performance, design architecture pass-downs, tool flow related issues, design implementation

guidelines and conducted design reviews for physical integration, AMS simulations, Analog design and digital verifications.

- Managed execution of DFT and Digital verifications. Reviewing test compliance, coverage, test writing according to specs and functionality.
- Timing characterization lead of analog cells using Silicon Smart to create liberty files of macros used in top level integration. Testbench and environment creation from scratch. Expertise in the various .lib formats NLDM, CCS, LVF.

DDR5phy and LPDDR5phy 6.4Gbps Design and Verifications - Intel.

- Mentored and managed a team of 16 designers located in India. Followed up career development, milestones accomplishments, execution performance. As well as design architecture pass-downs, tool flow related issues, design implementation guidelines and conducted design reviews.
- Technical lead of the analog building blocks like level shifters, output buffers, power gates, LDOs and delay, resistance and slew compensation in Intel advanced node technologies.

Non-volatile memory layout designer - Impinj.

- Designed layout of the NVM portion for RF tag devices starting from floorplan to final layout release for Tape out using both manual and automatic routing flows. Performed the required physical verifications (LVS, DRC, MRC, reliability) in GF and TSMC technologies. Participated in testchip projects using non-standard PDK devices taking into account device physics and manufacturability.

Physical Design Engineer (Intel) 2015 -2017

RTL to GDS design running the full APR flow from Synthesis, Timing constraints creation, Floorplanning, Power Planning, Placement, Clock Tree Synthesis, Routing, Timing Analysis and fixes, Physical Verifications and GDS release to Foundry. Expertise in Intel and TSMC process technologies from 0.35um to 14nm.

Freescale Semiconductor (Acquired by NXP)

VLSI Design Engineer 2004-2015.

- Technical lead for multiprotocol SerDes building blocks from 1.25G to 25Gbps in Rx path and clock distribution network: CTLE, LDO, Bias circuits, Clock drivers including retimers and clock division. High Speed clock network layout.
- Reliability and Physical verifications of the final GDS file to SoC follow up integration into the System on Chip block. Package team interaction, bump placement, script writing and power planning among other physical design and verification activities were developed.

Education:

Master of Science with specialty in Electronics Integrated Circuits Design, Instituto Nacional de Astrofisica, Optica y Electronica. 2005. Puebla, Mexico.
Electronics and Communications Engineer, Instituto Politecnico Nacional, 2002. Mexico City.

Additional Trainings:

Project Management Fundamentals Training. 2006 and 2013, internal training in Freescale.
Physical Synthesis Training, 2015, Cadence Design Systems.
Power and IR drop analysis sign-off training, 2010, Cadence Design Systems.
LEAN Fundamentals.
Static timing analysis fundamentals.
Synopsys Trainings: ICC2 SoC Design Planning and block implementation, Primetime Power and signal Integrity.

Publications and Papers:

EDA tool for checking signal power domain crossings.
*Melanie Etherton, Michael Khazhinsky, Edgar Oropeza, Eliseo Torres, Suzanne Biganzoli, Steffen Lorenz, Louis Thian***,** 2010 International Electrostatic Discharge Workshop. Poster Session.

Languages:

Spanish, Fluent English.

Software, Tools

Windows, Office Suite. Ms Project

C/C++, QT, TCL, PERL, Linux Shell scripting for tools programming and setup.
Extensive use of Linux environment.

Cad Tools

Cadence Virtuoso Analog Design Environment, Maestro, Innovus, Voltus, IC Compiler.
Synopsys Custom Compiler, Fusion Compiler.
Siemens Calibre.
Ansys Redhawk and Totem IR drop Analysis.
Synopsys Physical Design tools: Design Compiler, IC Compiler, ICC2, Primetime suite Fusion Compiler.
Version Control Management tools.
Spice Simulators, Command/text or GUI based.