VARUN SUBRAMANIAM

Raleigh, North Carolina | +1-9196370210 | vsubram8@ncsu.edu | https://www.linkedin.com/in/varun-subramaniam

Education

North Carolina State University, Raleigh, NC — *Aug 2023 – May 2025 (Expected)*
Master of Science, Computer Engineering — ***CGPA – 3.67/4***
Academic Coursework: Microprocessor Architecture, Advanced Micro-architecture, Architecture of Parallel Computers, ASIC and FPGA Design with Verilog, Advanced Verification with SystemVerilog, Advanced Functional Verification with UVM, Electronic System Level Design and Physical Design

SASTRA University, Chennai, India — *Aug 2017 – Apr 2021*
Bachelor of Technology, Electronics and Communication Engineering — ***CGPA – 3.62/4***
Academic Coursework: Digital Electronics, Computer Organization and Microprocessors, VLSI Design and Testing

Technical Skills

- **Programming & Scripting:** C/C++, Python, Verilog, SystemVerilog, Tcl
- **Verification Methodologies:** UVM (Universal Verification Methodology), Assertion-based Verification (SVA), Constraint-Driven Verification, Functional & Code Coverage
- **RTL Design:** FSMs, Datapath/Control Path Logic, Static Timing Analysis, Power-Aware RTL, Multi-Clock Domain
- **Protocol Knowledge:** I2C, AMBA (AXI, AHB, APB), PCIe
- **Tools:** Synopsys VCS, Intel Quartus Prime, QuestaSim, Git, MATLAB
- **Areas of Interest:** CPU Microarchitecture, Simulation, Timing and Performance Bottleneck Debugging

Academic Projects

Cache Design and Memory Hierarchy Simulator [C++] — *Sep 2023*
- Implemented an **N-Level cache simulator**, analyzing performance, area efficiency, and energy consumption using SPEC benchmarks and microbenchmarks. Developed a flexible cache simulator with **customizable stream buffer prefetching,** at each cache level. Applied **LRU replacement and Write-Back, Write-Allocate (WBWA)** methods to optimize cache setups.
- Examined three standard cache configurations **(Direct Mapped, Set Associative, Fully Associative)** and conducted graphical analysis to estimate Average Access Time while varying cache parameters.

Branch Prediction Simulator [C++] — *Oct 2023*
- Simulated a **branch predictor for instruction fetch stage of pipelined microarchitecture** focused on predicting branch outcomes and implemented various models in simulation **(bimodal, g-share and hybrid)** and evaluated their performance in predicting branch outcomes. Leveraged **object-oriented programming (OOP)** to enhance modularity and maintainability.
- Assessed the effectiveness of branch predictor simulator on misprediction rates by varying design parameters like prediction table size and GBHR size.

RISC-V Out-Of-Order Superscalar Pipeline Simulator [C++] — *Nov 2023*
- Developed and simulated a configurable **out-of-order superscalar CPU pipeline** enabling concurrent fetching and issuing of **'N'** instructions per cycle with **dynamic scheduling to maximize instruction-level parallelism (ILP)**.
- Implemented **register renaming, reorder buffer (ROB),** and **issue queue (IQ),** and **verified execution correctness** to effectively eliminate pipeline hazards **(WAR, WAW)**. Analyzed performance by comparing IPC values across varying superscalar widths, issue queue sizes, and reorder buffer configurations.

RTL Design and Synthesis of Quantum Computing Emulator [Verilog] — *Oct 2023*
- Designed a quantum computing emulator for **FP(floating point) matrix multiplication** across 1 to 4 qubits with distinct control/data paths using **FSMs**.
- Integrated IEEE-standard DesignWare MAC and Adder units to meet setup/hold constraints and achieved 0.02 slack across 2150 clock cycles with minimal area.

Work Experience

Cognizant, India — *Aug 2021 – Jul 2023*
Programmer Analyst *- Master Data Management*
- Orchestrated end-to-end ETL processes, MDM and data cleansing using SQL and Java, improving data accuracy and consistency.
- **Collaborated with cross-functional engineering teams** to troubleshoot and resolve defects, optimizing debugging workflows across large datasets.

Intrusion Detection Lab, SASTRA University, India — *July 2019 – Dec 2020*
Research Assistant
- Built and validated an Intel FPGA based RGB image encryption system, utilizing pseudorandom numbers generated from non-linear chaotic attractors for diffusion, with LFSR for pixel confusion operations. Optimized entropy (7.9961), correlation (-0.0019) and PSNR value (99.6375), to validate image encryption strength.

Licenses and Certification

SystemVerilog for Design and Verification | *Cadence Design Systems* — *July 2024*