Phong D Bach

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Physical Design Engineer

Results-driven Physical Design Engineer with over 20 years of experience in ASIC/SOC IC design, specializing in RTL to GDS physical design implementation. Proficient in utilizing cutting-edge EDA tools for logic synthesis, floor planning, place & route (PnR), and static timing analysis (STA), functional and timing ECOs, formal verification (FEV), DRC/LVS layout verification across multiple technology nodes from 90nm to 3nm and Intel 18A process. Leading fullchip and IP integration for numerous test chips in Intel's R&D prototype group, and known for delivering high-quality designs, achieving full-chip timing closure.

Key Skills

ASIC/SOC Design Flows | RTL to GDS Physical Design | Logic Synthesis | Floor Planning | Place and Route (PnR) | Static Timing Analysis (STA) | Synopsys Fusion Compiler | Design Complier | Primetime | Synopsys ICC/ICC2 | ICC-DP | Conformal FEV (LEC) Functional/Timing ECOs | ICV DRC/LVS Physical Verification | Siliconsmart | Calibredrv | icwbev | TCL | Perl Scripting Full-Chip and IP Integration | 14nm to 3nm and intel 18A Process Nodes | Leadership and Collaboration

Professional Experience

Intel Corporation, Hillsboro, Oregon **January 2016 - Sept 2024**
Sr. Physical Design Engineering
Performed RTL to GLS physical design implementation for various chip design for Intel's R&D prototype group, delivering clean databases and achieving tape-outs across multiple process nodes from 14nm to 3nm and intel 18A. Collaborated with cross-functional teams to integrate fullchip and IP, achieve full-chip timing closure and final DRC/LVS verification signoff.

- Executed complete RTL2GDS flow, including logic synthesis, floor planning, place and route (PnR), clock tree synthesis (CTS), and timing static analysis (STA), functional and timing ECOs, Conormal FEV (LEC) and DRC/LVS verification across Intel 14nm, 22nm, 10nm, 7nm, 5nm, 3nm and intel 18A process nodes.
- Led top-level and IP integration for numerous test chips, achieving tape-outs across multiple process nodes including Intel 3nm and 18A technologies and performing timing closure and DRC/LVS physical verification sign-off.
- Completed design convergence for advanced projects, including Micro Digital Sensor IP (Intel 18A) and HBM3IO IP 5nm to 3nm migration and IVR chiplet testchip based on 22nm process.

Intel Corporation, Chandler, AZ **January 2004 - December 2015**
Component Design Engineering
Executed the RTL2GDS design flow at partition/block level for multiple integrated chipsets and SoC projects. Provided synthesis and design support to ensure high-quality APR block-level execution and successful tape-outs across Intel's 90nm to 14nm processes.

- Led logic synthesis tasks and improved tool flow methodologies, ensuring high-quality results for APR execution. Incorporated DFT scripts into synthesis flow to do scan insertion and performed scan re-ordering in placement stage.
- Coordinated with front-end design teams to ensure RTL synthesis and APR quality compliance.
- Built and delivered full-chip netlists, optimizing for floorplaning, static timing analysis (STA), GLS executions.

Intel Corporation, Chandler, AZ **October 2000 - December 2003**
CAD Engineering
Contributed to the development and automation of ASIC/SOC design flows, focusing on tool validation, issue resolution, and flow enhancement. Provided DA support to the wireless/handheld division.

- Developed and validated design flows using Synopsys EDA tools, identifying and mitigating potential project risks.
- Collaborated with EDA vendors to enhance tool capabilities and resolve tool limitations in the design flow.

Intel Corporation, Chandler, AZ **June 1999 - March 2000**
Intern
Supported ASIC/SOC design flow validation, identifying tool limitations and developing solutions to enhance design methodology.

- Developed netlist test cases to evaluate PnR flow for new technology nodes, improving design efficiency.

Education

Bachelors of Science, B.S. Electrical Engineering
University of Washington, Seattle, WA

Citizenship: U.S. Citizen