Summary:

Enthusiastic and motivated engineer seeking an entry-level role in Formal Verification to develop expertise in applying formal methods for design verification. Passionate about logic, automation, and verification techniques, with a keen interest in learning model checking, theorem proving, and abstraction to ensure system correctness.

Name: Shweta Sarap

Email: shwetasarap12010@gmail.com

Phone: 669-263-4779

Location: Pune, IN

Country: India

Position Category: Verification: Formal verification

Desired Job Role: Formal Verification Engineer

University: Arizona State University, University of Pune, IN

Degree: Master of Science in Software Engineering, Master of Technology in Computer Engineering, Bachelor of Engineering in Computer Engineering

Graduation Year: 2021, 2018

Years Experience: 6

Notable Companies: TIAA, Atos Syntel

Top Skills: Formal Verification, System Verilog Assertions, System Verilog, C/C++, Python Scripting, Java

Job Intention: full-time

Visa Status: --

Able: no

Subject: Working at AheadComputing

Date Sent: 02-21-2025

Resume: Yes