SAUGAT SHARMA

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EDUCATION

Doctorate in Electrical and Computer Engineering, *University of Nevada, Las Vegas* May 2025

Course: Advanced Computer Architecture (Grade: A), Interconnected Networks for Parallel Processing (Grade: A), Modern Processor Architecture (Grade: A), Advanced Machine Learning (Grade: A)

Bachelors of Science in Electronics and Communication Engineering, *Tribhuvan University, Nepal* Nov 2017

EXPERIENCE

FPGA Design, *I/ONX Neuromorphic* | Las Vegas (Remote) May 2024 - Present

- RTL design and implementation of a custom convolution layer and DNN activation function in Vitis HLS for Versal FPGAs with SFP-based Ethernet.
- Developed AXI-stream processing for DMA input/output, memory-mapped to CIPS, and deployed via PetaLinux.
- Developed Python and Shell scripts for driver interaction, log analysis, and device tree modifications.

Graduate Teaching Assistant,*University of Nevada, Las Vegas*

Computer Logic Design, Digital System Architecture and Design, and Embedded System laboratory Jan 2019 - Apr 2024

- Taught design of datapath and control units for RISC/ARM-based microprocessors using Verilog and EDA tools.
- Guided students in writing testbenches and performing functional verification with VCS and ModelSim.
- Microcontroller(Atmega328P) programming (Assembly/C) covering Timers, Interrupts, PWM, ADC, I2C, SPI.
- Instructed on designing sequential & combinational circuits, FSMs, & arithmetic circuits using Verilog and Quartus.
- Guided students in performing timing analysis, simulation, and testing of synchronous digital systems.

PROJECTS

RTL Design and Verification of a 5-Stage Pipelined Processor for MIPS Architecture

- Designed and implemented a 5-stage pipelined MIPS processor in SystemVerilog on ZedBoard FPGA.
- Developed forwarding and hazard detection units to minimize stalls and improve instruction throughput.
- Verified functionality using UVM with constrained-random testbenches and coverage metrics.

RTL Implementation of Tomasulo's Algorithm for Out-of-Order Execution.

- Implemented Tomasulo's algorithm in SV, including instruction queue, reservation stations, reorder buffer.
- Developed hazard detection, forwarding, and register renaming for efficient instruction scheduling.

UVM Based Verification of AXI Memory and UART.

- AXI Memory: Developed UVM-based tb to verify AXI4 memory interface with random stimulus, protocol compliance, error scenarios, and coverage-driven checks for read/write, burst, and address/data operations.
- UART Interface: Designed UVM testbenches to verify UART TX/RX transmission, including baud rate handling, error detection, and protocol compliance with constrained-random stimulus and coverage analysis.

Cache Memory Simulator

- Designed and implemented an m-way set-associative cache simulator using python with sizes up to 128KB.
- Integrated LRU replacement policy to optimize cache performance and eviction strategy and track cache hits/misses.

System Verilog based MOESI simulator

- Modeled and analyzed MOESI cache states ensuring correct data consistency and memory coherency.
- Implemented various scenarios and performance metrics to evaluate the behavior of cache interactions, including cache hits, misses, and state transitions.

TECHNOLOGY & SKILLS

Programming	Python, C/C++, C#, embedded C, Matlab, Git, LaTeX, Assembly, Verilog, SV, VHDL, UVM
AI, Embedded Systems	TensorFlow, PyTorch, OpenCV, Scikit-Learn, Linux, AVR, ARM, x86, Raspberry Pi,Arduino
EDA Tools	VCS, DC, PowerArtist, Modelsim, Quartus, Vivado, Xilinx ISE
Certifications	Introduction of OpenCL on FPGAs (2023) | SV/UVM for Verification Fundamentals (2023)