BALAJI VELIKANDANATHAN

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Looking for a challenging and visible leadership role in implementation, design automation and methodology of cutting-edge process node Cores & SoCs

Summary

Seasoned VLSI professional with expertise in synthesis, P&R, signoff flows and methodology. Have held various technical and managerial roles in Intel (USA, Malaysia), Qualcomm (India) and Synopsys (USA). Have experience in CAD tool development, PD implementation, Flow and methodology development, DFx - DV execution and RTL to GDS implementation. Worked on implementation of multiple CPU, Chipset and Mobile SOCs across process nodes from TSMC, SEC and INTC foundries.

Developed scalable implementation flows for latest process nodes. Drove multiple PPA benchmarks on assorted designs like ARM cores, RISC-V cores, GPUs, PCIE, NPU and DDR subsystems on N5, 16FF and N3E process nodes. Worked with IP micro-architects on optimal design partitioning and AUC reduction.

Worked on successful Mobile/ML/Compute/IOT/Automotive SOCs that power millions of products. At India R&D, led an organization of more than 100+ engineers across Physical Design, Hard Macro IP development, Physical Verification, Design Convergence and Sign-off, catering to more than 6+ SOC Tape-outs (using 7nm, 10LPE, 5nm) annually in multiple market segments.

Contributed to the success of CPU and Chipsets in implementation and DFX domains. Worked on DFx verification, Power reduction, RTL coding of microprocessor features, Implementing key control blocks in ID, IFU, EXEC and MEM clusters. Involved working with architects to do power/performance trade off studies, retiming of logic, improving clock gating efficiency and CDC checks. As a CAD tool developer, I worked on physical design engines like placer, sizing and legalizer and built a full RTL2GDS flow competing with Magma and Physical compiler.

HIGHLIGHTS

- Strong technical, mentoring and leadership skills.
- Years of expertise in CPU (X86/ARM/RISC-V) and IP design, vertical implementation (RTL2Layout) and DFX verification
- Skilled in R2G physical implementation while building and retaining high performance teams with a focus on collaboration, agility, quality and results.
- Groomed/mentored several senior individual contributors to senior leadership roles.
- Multi-domain skill/work exposure and experience with strong belief in role rotation and continuous skill development

EXPERIENCE

SYNOPSYS

Sr. Solutions Architect ***Apr 2023 – Dec-2024***

- Worked on strategic engagement with multiple customer designs across foundry for Fusion Compiler (FE & BE)
- Working on customizing and deploying latest FC reference flow for customers
- Working with IP micro architects (ARM, NOC, DDR, PCIE) on PPA challenges.

Solutions Architect Apr-2019-March-2023

- Worked on improving timing/power/area metrics for complex DSP and ARM Core designs.
- Involved in benchmarking activities to show case best in class PPA for N7 and N3E designs.
- Worked on Fusion Compiler QOR improvement, Correlation between implementation and signoff engines and

run time improvement.

QUALCOMM ***Aug-2014 – Mar 2019***

Director of Engineering

- Lead a team of 125 designers. Team is responsible for physical design implementation (RTL-GDS) for Multimedia subsystems, Wireless LAN and Peripherals.
- Worked closely with IP micro architects to identify wholistic solutions for PPA challenges.
- Have worked on 10LPE (SEC), 7FF(TSMC), 7LPP, 8LPP, 11LPP, 12FF (TSMC) nodes MDM, MSM and Compute SOCs.
- Built a utility (QUA) that analyzes base and metal utilization concurrently that is used across QCOM SOCs.
- Owned multiple aspects of convergence & automation across P&R, Synthesis, STA, PDN, FV/CLP, PV for multiple SS of varying complexity.
- Collaborated with P&R EDA vendors to improve run time, QOR and correlation with signoff tools.

Principal Engineer/Mgr. (Process and Technology Vehicle Team lead)

- *As vertical team lead owned microarchitecture, RTL-GDS implementation activities.*
- *Taped out multiple test chips (complex chips with multiple IPs, power domains, 100mm^2 die size for Yield learning). They helped flag multiple process, IP issues for SoC products.*
- *Drove many PD pioneering studies like utilization push, Metal stack studies, Fmax push for ARM cores and Area metrics for QCOM SoCs.*
- *We now handle multiple test chips in parallel for IP validation and Yield learning! We work closely with the SoC PD&PV teams to share our learning's and BKMs.*

INTEL

- ***RLS Cluster Manager*** ***Apr-2014 – July-2014***
  - *Owned RLS flow development and pioneering and IP hardening of CPU HMs in 10nm process.*
  - *This involved working with micro architects to do some early 10nm Pioneering studies, converging on to SoC flows for Intel CPUs.*

- **Chipset DFx Cluster Manager** **March 2011 – March 2014**
  - Managed micro-architecture, Design & validation of DFT, DFD, DFx for chipset. Grew the team from 15 to 35 members. Built an ODC in BDC.
  - Drove the move to OVM and 10x power reduction for DFx features during functional mode working closely with the architecture, PDE and physical design teams for Lynxpoint Chipset. We also hit a DPPM of 32 vs. goal of 70 for first MCP product in Intel!

- **Cluster RLS Execution Lead** **June 2006 – Feb 2011**
  - Managed RLS Execution, (RTL to Layout, team of 15 DEs) mentoring junior RLS DEs, worked with stake holders and managed milestones to meet deliverables on NHM, WSM, HSW CPUs
  - *Worked with CPU cluster architects to retime logic, improve clock gating, partition designs to meet PPA targets and evaluate new architectural features like Fused Multiply Add*
  - Owned and drove front end and Execution cluster RLS block convergence, section timing convergence and silicon speed path fixes for a cross-site microprocessor design team in Oregon and Penang
  - Involved in methodology development, planning and execution of RLS blocks of varying complexities.
  - Drove the TR for MS unit in HSW, Coded MS Mode based branch feature (HSW), IQ perfmon and IQ macro fusion logic (NHM), Owned VPU cycle1-cycle3 re-pipelining for iLRB3, ALU and Shuffler in LRB3-FPC.
  - In the process of design convergence and by organizing chalk talks got familiar with the Front End and Exec Architecture and UCODE interaction.

- **Staff CAD Engineer** **April 2003 - May 2006**

Optimization flow development

- Key member of the placement optimization team developing optimization flow for microprocessor design teams

- The flow was deployed in Penryn CPU core.

- Ran a cross-site optimization WG with BNL, PNR, NHM RLS DA teams to deploy our flows.
- Developed and deployed buffering engine integrated the same with sizing and placement engines.
- Worked on QOR improvement and run time improvement of the optimization flow.
- Worked on QOR and run time improvement of cone re-synthesis flow.

- **Senior Engineer – ASIC Design** **March 2001 – March 2003**

Taped Out two million gate designs successfully.

- Was one of the key members of the team in taping out the two million gate fully functional first silicon LAN/WAN chips. Owned power analysis and SI analysis of all the blocks and full chip integration.
- Responsible for the full chip floor planning, power planning, power analysis and SI analysis with the IOs, blocks and boundary scan placements, top-level power routing.
- Functioned as DA for IME India and implemented several scripts in Tcl and Perl Languages for the automation of the ASIC flow.
- Helped in hiring, mentoring and managing schedules and tasks for junior DEs.

Evaluating innovative EDA tools

- Have been the early adopters of new SI and Power analysis tools (Celestry and Celtic) and work extensively with the vendors in providing futuristic inputs to improve QOR bettering the existing tools. **B**enchmarking these new tools against the industry standards to evaluate the price/performance of different tools.

Engineering IP analysis

- Managed the engineering analysis of soft and hard IPs**,** Worked closely with vendors like Rambus, Leda, Parthus, and TriCN while performing IP analysis for the designs at IME as part of the die size and effort estimation and planning**.**

- **Senior Engineer CAD,** Intel Corporation **Feb '99 – Feb '01**

- **Design and development of detail placer and legalizer.**

- Developed standard cell detail placer and legalizer. Involved 5K lines of C++ code. The placer had three different modes namely, wire length driven, congestion driven and timing driven.
- Also worked on Gordian based global placer. Worked on integrating a new timing engine into the placer.

- **CAD Engineer,** Intel Corporation **Nov '96 - Jan '99**

Design and development of CAD framework.

- Collaborated with a team of three members to design and develop a CAD framework that would bring a common look and fell for all Intel CAD tools. Ported the same to WINNT operating system.

- Collaborated with a team of four members to provide and support additional features and flows to existing Layout editor.

- **Summer Intern**, Intel Corporation **Jun '96 - Sep '96**
  Member of the object-oriented design team that designed and implemented a C++ based GUI for Intel CAD tools.

Country of citizenship **USA**

EDUCATION

- M.S., in Computer Science, Syracuse University, NY.
- B.E., in Electronics and Communication Engineering,
  Guindy Engineering College, Anna University, India.

DESIGN SKILLS

- ***EDA Tools***:
  Back end: Fusion Compiler, ICC2, EDI, Red Hawk, DSO.ai
  Front-end: Design Compiler, RTLA, Prime Time, Verdi-Debussy
- ***Languages Proficient In***: C, C++, Tcl, System Verilog, Perl

REFERENCES

- Available on request