Summary:

Pavan Kiran Reddy Kotla is a skilled formal verification engineer with experience at AMD and Arteris IP. He has a Master's degree in Computer Engineering from the University of Houston and a Bachelor's degree in Electronics and Communication Engineering from Osmania University. His top skills include System Verilog, Verilog, SVA, UVM, C, JavaScript, Python, TCL, VC Formal, Jasper, VCS, Verdi, Mentor Questa, ModelSim, Quartus Prime, MATLAB.

Name: Pavan Kiran Reddy Kotla

Email: kotla.pavankiran@gmail.com

Phone: (713) 517-2475

Location: San Francisco Bay Area, CA

Country: USA

Position Category: Verification: Formal verification

Desired Job Role: CPU Formal Verification Engineer

University: University of Houston, Osmania University

Degree: M.S in Computer Engineering, B.Engg in Electronics and Communication Engineering

Graduation Year: 2023, 2020

Years Experience: 2

Notable Companies: AMD, Arteris IP

Top Skills: System Verilog, Verilog, SVA, UVM, C, JavaScript, Python(scripting language), TCL, VC Formal, Jasper, VCS, Verdi, Mentor Questa, ModelSim, Quartus Prime, MATLAB

Job Intention: full-time

Visa Status: --

Able: no

Subject: Interested in Formal Verification Engineer position at Ahead Computing

Date Sent: 03-11-2025

Resume: Yes