Mark Zakharov

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Education

University of California, Santa Cruz — Santa Cruz, CA
Master of Science, Computer Science & Engineering, Thesis Route — *Graduated June, 2024*

University of California, Santa Cruz — Santa Cruz, CA
Bachelor of Science, Computer Engineering — *Graduated June, 2021*

Experience

RTL Design and Verification — Jun 2021-Oct 2022, Summer 2023, Aug 2024-Current
Esperanto Technologies — *Mountain View, CA*

- **RISC-V Vector/Floating-Point Unit Design** - Optimized RTL for low-power and low-area with consideration for process technology of Minion in-order core. Debugged issues in FMA and FCSR/VCSR units.
- **Cosimulation Support for Verification** - Augmented in-order core pipeline stages for payload timing to link C++ API with DPI based transactors to track D-cache, synchronization primitives, and interrupt traffic. Implemented event-driven callbacks in Architectural model to match DUT.
- **Dromajo RISC-V ISA Reference Model** - Added support for RVV vector unit and Maxion out-of-order core. Used to debug core issues in verification and silicon bring-up.

Graduate Student Researcher — Mar 2023-Jun 2024
University of California, Santa Cruz — *Santa Cruz, CA*

- **HDL-Agent Multi-Language Agent** - Led research group investigating uses of LLMs as RTL designers, guiding implementation flow through compiler feedback and custom-tailored context of unknown HDLs. Agent supports Verilog, Chisel, PyRTL, and DSLX development and uses Yosys for synthesis.
- **HDEval Language Neutral Dataset** - Developed HDL dataset for evaluating LLMs as RTL designers for any language. **Accepted paper into ISLAD workshop**. Fine-tuning paper **Invited as WIP Poster** to present dataset being used to train LLM to patch RTL based on waveform feedback.
- **Accelerator Tapeout with Caravel 130nm** - 2nd place winner of Efabless' GenAI contest through submission of RISC-V compliant 32-bit Cryptographic Accelerator, achieved by contextually few-shot teaching LLM an unfamiliar language, DSLX. Prize was free tape-out.

Teaching Assistant - Computer Architecture, Embedded System Design — Fall 2022, Spring 2024
University of California, Santa Cruz — *Santa Cruz, CA*

- Managed undergrad tutors as assistants to students and led hands-on lab sections for Linux/Microcontroller development. Hosted weekly office hours with self-prepared supplemental materials. Responsive and respectful with Slack messages, while being patient with struggling students.

Research

LiveHD RTL Compiler — Feb 2021-Feb 2023
MASC Research Group — *University of California, Santa Cruz*

* Helped debug Multi-lang RTL compiler for logical equivalence between languages, ensuring accurate Verilog generation from AST model. Implemented generic, synthesizable template for RAM generation.
* Developed random code generator to create equivalent circuits in various HDLs to validate compiler translation flow. Used Yosys as SAT solver to perform logical equivalence checks.

DESESC Architectural Simulator — Dec 2022-Feb 2023
MASC Research Group — *University of California, Santa Cruz*

* Integrated Dromajo as backend driver, replacing QEMU, improving runtime as well as eliminating dependencies.
* Enchanced users' debugging capabilities by enabling functional use of GDB stub with simulator-run binaries.

Technical Skills

Languages: Verilog, Python, Bash, Chisel, C, C++, RISC-V ASM, DSLX

Technologies & Tools: Linux, Git, Yosys, Icarus Verilog, Verilator, RISC-V Sim and Compiler Toolchains

Relevant Coursework: Advanced Microprocessor Design, ASIC Systems Design, Adv Topics in NLP, Intro High Perf Computing

Interests: Highly parallel architectures, LLMs for RTL design and verification, out-of-order processors, ASIC design