Dear Hiring Team,

Hope you are doing well.

My name is Sai Surendra Reddy Yaraballi, and completed my Master's in Computer Engineering at Texas A&M University. Currently, I am looking for full-time roles to start immediately. I saw that you are hiring for SeniorFormal Verification Engineer role at Ahead Computing and I express my interest in the opportunity.

I have 2 months of Internship experience as anRTL Design intern where I worked on DDR SDRAM Memory controller RTL design and FPGA based Temperature monitoring control system. Coming to academic background I completed Introduction to Hardware Design Verification, Advanced Hardware Design Functional Verification and Advanced Computer Architecture courses. During my coursework, I worked on Verification projects utilizing Cadence Xcelium, JasperGold, vManager, IMC tools for the below mentioned projects:

1. Functional Design and Formal Verification of Multicore MESI based Cache Design System.
2. Design Verification of High Throughput Advanced X-bar (HTAX).
3. Design and Functional Design Verification of AHB2APB Bridge.
4. Formal Verification of Combinational Lock
5. RTL Design of MIPS 5-stage Pipelined Processor

By completing the above mentioned projects, I gained skills such as Verilog, System Verilog, Universal Verification Methodology (UVM), System Verilog Assertions (SVA), Covergroups and assumptions. I am also proficient in C, C++, Python, Tcl and have knowledge in AMBA AXI, APB, AHB and DDR protocols.

I strongly believe I can contribute my skill set and knowledge by working on key projects and will help me in excelling my career growth and looking forward to connecting with you to discuss about the opportunity.

I am attaching my resume to look over.

Thanks & Regards,

Sai Surendra Reddy Yaraballi