Summary:

Experienced Physical Design Engineer with a master's degree and 9 years of experience in ASIC design, clock tree optimization, and verification methodologies. Proficient in Synopsys suite and skilled in technology nodes ranging from 180nm to 3nm.

Name: Nicte Reyes

Email: anictereyes@gmail.com

Phone: +52-3316232839

Location: Mexico

Country: Mexico

Position Category: Design: Physical Design

Desired Job Role: Staff Physical Design Engineer - CPU PPA Optimization

University: INAOE, ITM Morelia Mexico

Degree: M.S Integrated Circuit design

Graduation Year: Estimate

Years Experience: 9

Notable Companies: Synopsys Inc. Mexico, Intel Labs. Mexico, Intel Company. Mexico, Freescale Semiconductor. Mexico

Top Skills: ASIC design, STA, RTL-to-GDS flow, Clock tree optimization, Synopsys suite

Job Intention: Full-time

Visa Status: --

Able: Yes

Subject: Working at AheadComputing

Date Sent: 03-25-2025

Resume: Yes