Srikanth Muthuvel Ganthimathi

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EDUCATION

Binghamton University, State University of New York, Thomas J. Watson College of Engineering and Applied Science
Master of Science in Electrical and Computer Engineering, Specialization in VLSI *Expected May 2026*
Cumulative GPA: 3.60/4.00
Relevant Coursework: *CMOS VLSI Circuits & Architecture, System on a chip (SoC), RFIC (Integrated circuits), Digital Systems Design II, Computer Design/Architecture, and Hardware-Based Security.*

SASTRA Deemed to be University, Thanjavur, India
Bachelor of Technology in Electronics and Communication Engineering *Aug.2020 - June 2024*
Cumulative GPA: 3.05/4.00
Relevant Coursework: *Device Physics, Digital Systems Design, Digital VLSI Design, IoT Devices, Embedded Systems, Nano Electronic Devices, Microwave Engineering, Linear Integrated Circuits.*

TECHNICAL SKILLS

Hardware Description Languages: Verilog, SystemVerilog

EDA Tools: Cadence Virtuoso, Synopsys Sentaurus TCAD, Xilinx Vivado, Questa, Electric Open EDA, MATLAB, LTSpice

Programming Languages: Embedded C, C++, Python

Hardware Platforms: PYNQ Z2, ATmega328 Microcontroller

Other Tools: Visual Studio Code, Vitis HLS, Simulink, AutoCAD

PROFESSIONAL EXPERIENCE

Graduate Research Assistant | *SUNY, Binghamton* *Aug. 2024 - Present*

- Designed and optimized a **6T SRAM cell** and a **2×2 1T1C DRAM array** in **LTSpice**, improving memory efficiency and stability.
- Developed and tested **peripheral circuits**, including **bitlines**, **multiplexers (MUX)**, **demultiplexers (DEMUX)**, **4:1 decoders**, **sense amplifiers**, and **wordline drivers,** ensuring seamless read/write operations.
- Implemented **TSMC 180nm technology**, optimizing **power, performance, and area (PPA)** for high-speed memory applications.

PROJECT EXPERIENCE

Optimized 16-bit Accumulator for Real-time Data Processing | *Cadence Virtuoso* (Aug. 2024 – Dec. 2024)

- Designed a **16-bit accumulator** using **D flip-flops** and a **multi-bit adder**, achieving a **50% efficiency boost** in continuous summation.
- Implemented **a 1-bit circuit** with 2 XOR, 1 OR, 2 AND, 1 NAND, and 5 inverters, passing **Design Rule Check (DRC)**, **Layout Versus Schematic (LVS)**, and **Electrical Rule Check (ERC)** for ASIC compliance.

TFET-Based Biosensor for High-Sensitivity Biomolecule Detection | *Synopsys Sentaurus TCAD* (Jan. 2024 – May 2024)

- Developed a **QESV-DM-TFET biosensor** with dielectric modulation, enhancing biomolecule detection sensitivity.
- Achieved a **1e9 on/off current ratio**, **improving threshold voltage** sensitivity and **reducing subthreshold swing** for efficient detection.

High-Speed 32-bit Floating Point Unit (FPU) Design | *SystemVerilog, IEEE 754* *(Aug. 2024 – Dec. 2024)*

- Designed an **IEEE 754-compliant FPU** for addition, subtraction, multiplication, and division, optimizing numerical precision.
- Achieved **100% accuracy** in binary input handling and **95% error detection** in simulation testing.

Optimized Cache Memory for High-Performance Computing | *Verilog, Xilinx Vivado* *(Aug. 2024 – Dec. 2024)*

- Developed a **direct-mapped cache** with **16 cache lines**, **32-bit addressing**, and **4-word block size**, reducing cache latency.
- Implemented optimized tag-matching algorithms, **boosting data processing speed by 30%** in simulation tests.