Jose David Bolaños Rodriguez

Senior Systems Engineer & FPGA Design Specialist

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Summary

Dedicated and knowledgeable Sr. Systems Engineer with over a decade of experience in Hardware design, FPGA design, and embedded systems. With a solid background in Python, I've effectively used my skills for automation and streamlining design processes for 10 years. My career includes impactful roles at Intel Corporation and Plexus Corp, where I focused on hardware design, system architecture, and collaborative team efforts. I am proficient in C/C++ programming, PCB layout, and signal integrity simulation, and I am committed to continuous learning and growth in embedded system technologies and technical project leadership.

Core Competencies

- Systems Engineering
- FPGA Design & SoC Architecture
- Python for Automation & Process Improvement
- Embedded Systems Development
- Hardware Design & PCB Layout
- Signal Integrity & Power Sequencing
- Collaborative Leadership & Project Management
- IoT Connectivity & Sensor Integration
- Mechatronics

Work experience

Embedded Systems Engineer October 2023 - Present

Intel Corporation

Specialized in Agilex 7 devices, focusing on developing and supporting embedded systems with C/C++ programming, leveraging Acceleration Functional Unit (AFU), and debugging protocol management.

FPGA Design Applications Engineer, Acceleration Systems March 2022 - October 2023

Intel Corporation

Reviewed product requirements, developed customer journey, performed product evaluations, developed technical assets, and responded to customer technical queries.

Sr. Hardware Engineer - Digital August 2018 - May 2021 - June 2021 - March 2022

Plexus Corp

Developed engineering/product concepts fulfilling stakeholder needs, performed design work, supported proposal development, and possessed skills in schematic capture, PCB layout, signal integrity

Basic information

Nationality
Mexican

Website
linkedin.com/in/jdavidbr

simulation, HDL coding, and lab equipment operation.

Sr. Functional Validation Engineer May 2021 - June 2021
Intel Corporation
Developed system validation environment and test suites, applied post-Si validation tools, and interfaced with various teams for improving post-Si test content.

Hardware design engineer March 2018 - August 2018
A2e technologies
Focus on designing new projects for other companies, defining full project scope, technology stack, major component placements, and FPGA Design HW/FW.

Hardware Design Engineer & FPGA RTL June 2014 - February 2018
Intel Corporation

- Hardware Design of Complex Reference Boards for Xeon Server Platforms (Single, Dual, and Quad socket systems).
- Responsibilities included requirements gathering, platform architecture studies, silicon devices pin assignments, schematics generation, power delivery and distribution, board connectivity design, power sequencing, RTL code design and validation, FPGA features implementation, and high interaction with various internal teams.

Python Developer Internship July 2013 - June 2014
Intel Corporation

- Developed an schematic Reviewer tool for hardware designers to check errors like shorts, aesthetic wrong connections for cleaner schematic output.
- Created an Auto-Placement tool for board design allowing user and stakeholders to set parameters and get possible configurations.

Education

Bachelor of Engineering. Electronics and Communication July 2009 - June 2013
University of Colima

SKILLS & ENDORSEMENTS

Systems Engineering, FPGA Design, SoC Architecture, Embedded Systems, C/C++ , Programming, Hardware Design, PCB Layout, Signal Integrity Simulation, Schematic Capture, Power Sequencing, Cross-functional Collaboration, IoT Connectivity, Mechatronics, Sensor Integration, Post-Silicon Validation.

Interests

Advanced Embedded System Technologies, Technical Project Leadership, Cutting-Edge SoC Developments, Innovation in Electronics and IoT, System Architecture Design, Cross-Functional Team Management, Industry Trends in FPGA and Hardware Design.