Alejandro Iglesias

Verification Engineer

Achievement-oriented verification engineer with passion for self-learning and improvement. Hunter of difficult problems to develop solving skills. Known for attention to detail, and the ability to collaborate in fast-paced environments. Committed to leveraging technology to drive results and enhance performance.

Guadalajara, Jalisco
+52 811 743 4327
jaim_ccm@hotmail.com
linkedin.com/in/jesusaiglesias/

EXPERIENCE

Intel Corporation

Pre-Si Verification Engineer January 2024 - Present

Focus on core cache and execution unit of flagship efficient core.

Main responsibilities:

- Developed test plans based on architectural specifications and requirements.
- Created and modified UVM testbenches to test DUTs using constrained stimuli and SystemVerilog Assertions (SVAs).
- Planned, developed, and collected coverage based on functional specifications at the IP level.
- Debugged issues related to design and environment using verification tools like Verdi.

Achievements:

- Took ownership of several features regarding 2nd level cache and floating point execution, making sure all steps of the verification plan were fully achieved.
- Created a debug setup script to minimize interactions before a debug session using a specified path, reducing debug times by preparing the terminal with the correct environment setup and automatically opening the simulation waveform file.

Post-Si Validation Engineer January 2022 - January 2024

Focus on IO-to-die bridge (PCIe protocol to coherent protocol), the coherency mesh network, and various die utilities (locks and interrupts) on flagship server SoC

Main responsibilities:

- Developed test plans in the initial stages of projects.
- Created tools, tests, and checkers for individual IPs to enhance corner-case validation.
- Debugged issues related to the functionality of IPs.

Achievements:

- Developed a script to compare versions of our tools and firmware images between the systems we used to validate, and pin-point version mismatches between them. A technical paper was submitted to an Intel internal conference.
- Developed a script to obtain the coverage of our tests in volume validation. This increased the efficiency of our tests by reporting which instructions were overlapping or missing from the random stimuli of our test generators.

Hardware Design Intern June 2020 - January 2022

Achievements:

- Created an embedded system that measures the impedance of motherboard pathways, allowing coworkers to save time compared to manual measurements. The development process included testing individual ICs, designing the PCB, and developing the firmware. A paper detailing this work was submitted and accepted at an Intel internal conference.
- Developed an application that enables JTAG programming for FPGAs via USB, eliminating the need for a Blaster.
- Developed a console-based application that utilizes an Excel spreadsheet to adapt Verilog designs based on user needs, facilitating the creation of Quartus projects for individuals with basic Verilog knowledge.

SKILLS

UVM
SystemVerilog
Python
C
C++

EDUCATION

University of Alberta

Electrical and Computer Engineering Exchange Student

January 2020

Edmonton, Alberta

Autonomous University of Guadalajara

Electrical and Biomedical Engineering

December 2021

Guadalajara, Mexico

Achievements:

-Created a full course on logical design with the approval of the dean of engineering.

-Won innovation and entrepreneur contest with application to detect neonatal asphyxiation in hospitals.