SHARAFAT HUSSAIN

Lahore, Pakistan

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ABOUT ME

Sharafat Hussain is a **Design Verification Engineer** with over **2+ years** of experience, specializing in the verification of data-centric, out-of-order RISC-V cores. He is skilled in RISC-V ISA, directed testing using C and assembly languages, and in implementing UVM testbenches for comprehensive functional verification. Additionally, he has expertise in writing architectural test plans, verifying functionality through UVM testbenches, and ensuring coverage closure to validate the design thoroughly.

WORK EXPERIENCE

Design Verification Engineer

10xEngineers *November 2022- December 2024*
Lahore, Pakistan

Working for a prominent **US-based client** with a task of verifying a next generation cutting-edge Out-Of-Order **RISC-V data-centric core**

- **Branch Predictor Unit(BPU)**
  - Performed functional verification of the BPU unit in the core using a UVM-based testbench, which involved writing checkers and executing BPU test plan to validate accurate branch prediction functionality
  - Debugged and resolved 50+ DV and RTL issues, ensuring the BPU functioned correctly and met all specified requirements
  - Worked on functional coverage for the BPU across various scenarios, writing coverpoints and applying missing stimulus to achieve coverage closure
- **Vector Execution Unit(VXU)**
  - Developed and executed an architectural test plan for the RISC-V vector extension by writing architectural tests in C and assembly, then porting them to RTL and reporting RTL failures
  - Integrated RISC-V Crypto Architectural Test suits into the verification environment, validating the architectural behavior of vector crypto instructions
  - Debugged and reported test failures during RTL execution, highlighting key issues for resolution
- **Global Pipeline Controller(GPC)**
  - Implemented functional coverage for the GPC and performed coverage closure to identify and address gaps, validating all pipeline stages
  - Gained in-depth understanding of Out-of-Order processor micro-architecture
- **Regression debugging of architectural tests:**
  - Triage a wide range of RISC-V architecture-specific regression tests, covering both unprivileged and privileged specs, to identify RTL and DV bugs
- **Macro-Op Cache Tag(MOCTag):**
  - Enhanced the UVM testbench for the MOCTag unit by updating checkers and improving the cache model to ensure robust verification.
  - Developed a comprehensive environment for injecting parity errors in parity-protected RAMs, ensuring proper error detection and accurate RAS reporting.

* Monitored and optimized functional coverage for the MOCTag unit, driving improvements in verification efficiency and completeness.

Associate Engineer
10xEngineers Pvt. Ltd *July 2022- December 2022*
Lahore, Pakistan

- **Comprehensive training program**
  * Covered areas of RTL Design, Computer Architecture and Design Verification
  * Developed a verification environment in UVM for verifying an AHB Lite Slave module IP
  * Worked on creating and driving sequence items to AHB Slave IP (DUT) and monitored the stimuli for comparing it to a reference model in scoreboard
  * Created UVM-based verification environment from scratch to verify the Ibex Core by comparing the trace files generated from RISC-V toolchain and RTL

EDUCATION

University of Engineering and Technology, Lahore *Oct. 2018- Nov. 20*
Bachelor of Engineering
Electrical and Computer Engineering

PROJECTS

Verified the two generations of RISC-V based server class cores

SKILLS

SystemVerilog	Universal Verification Methodology (UVM)	Verilog
Questa Sim Tool	Visualizer	C
RISC-V Assembly	SystemVerilog Assertions(SVA)	Git
Python		