NAJIMUN AHMED

ahmednajimun@gmail.com
+91-7002722876,9387140407

Job Profile

An electronics engineer who is always in the thrive to learn new things and enhance personal as well as professional goals.

Work Experience

Arm Embedded Technologies Pvt Ltd Bangalore
Verification Engineer *Oct 2022 – Sept 2024*

- System Development and validation of ARM V9 class CPUs -
  -Involved in the complete integration, bring up and verification of the V9 platform on both emulation and simulation, right from development of System level test plan and test scenarios through out the development cycle of the CPU IP.
- System level validation of ARM enterprise class interconnect which involves planning, implementation and execution of stress test cases scenarios to find RTL bugs.
- System Development & Validation -
  Understanding of System Architecture & memory map.
  Integration of ARM IPs into our SOC.
  Integration testing.
  Exposure to simulation & emulation verification environments.
- Responsible for stress verification of Arm CPUs at system level on platforms like Emulators and FPGA, using RIS (Random Instruction Sequence) tools based methodologies.
- Worked on verifying Arm processors like Cortex-A725, Cortex-A520 and Cortex-A925 and Arm big.LITTLE platform.

Logic Fruit Technologies Bangalore
Verification Engineer *June 2022* – Sep 2022

- Working on PCIe Gen6 VIP Development
- Performance monitoring of PCIe Gen5 Phy Regressions.

Smartsoc Solutions Pvt Ltd Bangalore
Verification Engineer *May* 2021 – May '22

- Developed constrained random verification environment for
  • AXI,APB Protocol VIP Verification.
- Working on AMD VCN Project.
- Developed an environment with single master agent and single slave agent which can be configured later.
- Verified the AXI VIP's functionality with different types of transfers and bursts. Generated functional coverage for verification on sign-off.

Professional Course

Advanced VLSI Design and Verification from Maven Silicon

- Advanced Digital, Verilog, System Verilog, Systemverilog Assertions STA and UVM

Google Project Management

Arm Functional Safety SW Development

- Systematic approach to product safety design and verification activities based on ISO26262 and V model-based approach.

Technical Skills

Languages: Verilog, VHDL, System Verilog, C
Scripting Languages: Perl,Python Scripting
Methodology: UVM
Tools: Visualizer,VCS, Questasim, QuartusPrime, Xilinix,Zebu,Veloce

Education

2024-26: M.Tech in AI from Indian Institute of Technology, Jodhpur
2018: B.E. in Electronics & TeleCommunication from Dibrugarh University with 71.48%
2013: HS from AHSEC, Assam with 85.80%
2011: HSLC from SEBA, Assam with 81.50%

Personal Details

DOB: 05th January 1995
Languages Known: English,Hindi & Assamese
Address: Malikuchi, Near Gandhi Park,Nalbari,Assam-781334

14-12-2024 Najimun Ahmed