Rahul Thomas Abraham
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EDUCATION

Northeastern University, Boston, MA — Sep 2021 – May 2023
Candidate for Masters in Electrical and Computer Engineering (GPA: 3.8/4)
Related Courses: CMOS Analogue Integrated Circuit Design, CMOS Digital VLSI Design, Advanced Power Electronics, Micro and Nano Fabrication, Low Power IC Design, Computer Architecture, SSD, Hardware Security

Vellore Institute of Technology, Chennai, India — Aug 2016 - May 2020
Bachelors in Electrical and Electronics Engineering (CGPA: 8.45/10)
Related Courses: Microprocessors and Microcontrollers, Advanced Control Systems, Electric Vehicles, Digital Integrated Circuits, Semiconductor Devices, Digital Signal Processing, High Voltage Engineering

TECHNICAL KNOWLEDGE

Programming Languages: TCL, Python, Java, C, C++, Verilog
Environment and Tools: Redhawk**,** MATLAB, Spice Software, Cadence Virtuoso, Simulink
Digital Electronics: Device physics, Verification, Timing Analysis, Hardware Failures, Physical Design

Work Experience

Intel Corporation, Oregon, United States — June 2023 - Present
Physical Design Integration Engineer

- Designing test chips that feed yield learning for advanced technological nodes
- Involved in full chip integration of various IPs using Fusion Compiler
- Working with block owners by analyzing results from physical verification flows and giving feedback to fix violations
- Collaborating with front-end engineers to drive LEC closure
- Improved TFM by manipulating the underlying code which reduced the debug time by 20%
- Utilized RTLFP tool for the first time to create pin rings for AMS and IO blocks which reduced the overall execution time by 20%
- Worked on Intel's Backside power delivery technology
- Designed top metal pattern to increase design rule coverage by 10%
- Performed static IR drop analysis to improve the power-grip robustness by 30%
- Designed and implemented custom TCL code for cell creation, placement, routing, design rule fixes and improving robustness which could be used across different designs
- Developed methodology to generate multiple derived databases from a single run thereby reducing the overall build-time for designs by 40%
- Involved in multiple path-finding projects for more efficient execution
- Automated several repetitive tasks using shell scrips improving efficiency by 20%

Intel Corporation, California, United States — May 2022 – Dec 2022
Post-Silicon System Validation Intern

- Involved in power and performance post-silicon testing.
- Create, define and develop system validation environment and test suites.
- Currently working on developing a synthetic workload to replace a widely used test procedure.

ACADEMIC PROJECTS

Silicon-level Implementation of Modified Booth Multiplier
Silicon-level implementation of Trans-impedance Amplifier