Summary:

Nilesh Karnik is a Sr. ASIC Design Engineer with 23+ years of experience, demonstrating proven technical leadership at INTEL CORP. His roles and responsibilities have covered a wide range of areas including Physical Design, IP Logic Design, and Formal Verification among others. He is seeking a Senior/Staff Engineer Full-time Role in the CPU Physical Design at AheadComputing Inc.

Name: Nilesh Karnik

Email: n_karnik76@hotmail.com

Phone: +1 (916) 402 1350

Location: Folsom, CA

Country: USA

Position Category: Design: Physical Design

Desired Job Role: Staff Physical Design Engineer CPU PPA Optimization

University: California State University, Sacramento CA, Mumbai (Bombay) University, India

Degree: MSEE (VLSI), BSEE (Electronics), Diploma in Industrial Electronics

Graduation Year: 2001, 1999, 1996

Years Experience: 23

Notable Companies: INTEL CORPORATION

Top Skills: Physical Design - Planning, Implementation, SOC Design and Integration, Tools-Flows-Methodology development & support, Pre-Si STA/SI Convergence, Quality/Reliability and Signoff, IP Logic Design (RTL) & Formal Verification, Soft-IP Qualification, PPA Estimation

Job Intention: full-time

Visa Status: --

Able: no

Subject: Application for Staff Physical Design Engineer CPU PPA Optimization position at AheadComputing Inc.

Date Sent: 04-15-2025

Resume: Yes