ASHISH JHA
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PROFESSIONAL SUMMARY

Executive Engineering Leader with over 27 years of engineering experience, demonstrating a unique blend of technical expertise, strategic business acumen, and people management skills. Proven execution-driven leader with a remarkable track record of collaborating with cross-functional teams and spearheading global initiatives to achieve business goals and technical excellence. Delivered multi-billion-dollar high-volume consumer products over two decades.

Extensive expertise in the x86/64 SoC product lifecycle, encompassing architectural innovations, product development, and successful NPI launches. Specializes in partner and customer engagement & enabling, competitive strategy & analysis, mergers & acquisition, product innovation & quality, hardware-software co-design, performance and power validation, benchmarking, characterization and performance optimization. Areas of expertise include High-Performance Computing (HPC), AI/ML, Enterprise, and PC/Workstation markets.

PROFESSIONAL EXPERIENCE

AMD (Advanced Micro Devices) Incorporate, Morrisville, North Carolina — May 2018 – Present
AMD Fellow (Executive), HPC, Enterprise & AI/ML Performance Architect, Datacenter Engineering Group

Intel Corporation, Hillsboro, Oregon — Mar 2001 – May 2018
Senior Staff Engineering Manager, HPC & Enterprise Performance Architect, Platform Engineering Group

InfoGain Corporation, Los Gatos, California — Jan 2000 – Feb 2001
Team Lead & Developer

SkyTech Solutions, Calcutta, India & Chicago, US — Sep 1998 – Jan 2000
Team Lead, Business Analyst, Architect & Programmer

TCG Software Services, Calcutta, India — Jul 1997 – Aug 1998
Software Engineer

AREA OF EXPERTISE

Product Leadership and Ecosystem Partner & Customer Engagement & Enabling:

- Delivered relentless execution prioritizing ecosystem engagements, empowering datacenter and cloud customers and partners with custom SKUs for their infrastructure. Oversaw ~15 accounts, including national and federal labs, academia, the open-source community, and partners (MDC/CSP/OEM/ODM/OSV/ISV). Established trust and demonstrated clear leadership in product quality including features, performance, and Total Cost of Ownership (TCO), achieving an impressive market share increase from 0% to 35% across five AMD EPYC SoC CPU generations.
- Directed over two decades of end-to-end SoC development with comprehensive pre- and post-silicon performance and power validation, benchmarking, and analysis encompassing CPU, memory, and network across various innovative architectures including AMD EPYC, Intel Xeon, Intel Atom, Intel Itanium, and Intel Knights targeting Datacenter, Cloud, Enterprise and PC/Workstation market segments.
- Orchestrated the cross-functional research & development of Intel's SIMD ISAs (SSE4.1, AVX1/2/512) initiatives, collaborating with ~20 US DOE Federal customers & OEM/ODM partners. Aligned requirements with product intercepts for over two decades of Intel Xeon CPUs, securing a dominant 98% market share in the datacenter sector.

Customer-Driven Strategy and Execution:

- Aligned with companywide Time-to-Market (TTM) initiatives, spearheaded joint benchmarking efforts with Mega Datacenter Cloud & Enterprise customers & partners to deliver quality NPI products and support launch of their infrastructure. Led cross-functional enabling of FAE Sales & Marketing teams, formulated go-to-market (GTM) strategies, using proof points and performance collaterals/briefs with early ISV/OEM/OSV certifications & enabling ensuring day-0 AMD EPYC product readiness.

- Served as the "Voice of Customers," leading deep engagements to build trust, gather requirements, and address issues, driving internal improvements through JIRA. Directed co-design efforts with ~15 US DOE Federal & Academia customers on Supercomputing development, influencing HW & SW enhancements and design wins.

Strategic Initiatives:

- Spearheaded AI initiatives across AMD business units, rigorously benchmarking AI workloads including Intel and ARM. Positioned EPYC CPUs as a cost-effective alternative for inference, driving alignment on common messaging. Ensured EPYC's status as the preferred host CPU for CPU-GPU platforms, securing funding for the development of an EPYC-based software stack that delivers superior performance and Total Cost of Ownership (TCO) to customers.
- Identified strategic threats from competitor x86 tools affecting AMD EPYC CPU performance and secured multi-year, multi-million-dollar funding for self-reliance. Influenced the acquisition of an HPC library company and built strong engagements with 10 HPC ISVs, driving AMD's first Compiler & Library software toolchain success, securing multi-million-dollar wins across Enterprise, Cloud and Workstation/PC market segments.
- Championed a multi-year initiative at Intel to address the divergence of products across Xeons, low-power Intel Atom, and Intel Knights accelerator Instruction Set Architecture (ISA) resolving x86 incompatibility. Led innovation initiatives (AVX512) that instilled confidence and delighted customers, culminating in multi-billion-dollar HPC wins.

Market and Competitive Analysis:

- Presented executive updates with competitive intelligence on benchmarking analysis of x86, ARM, IBM Power CPUs, and NVidia GP-GPUs. Leveraged foundational industry-standard benchmarks, open-source & commercial HPC & AI applications to shape product strategy, sales/RFP pricing, and counter competitive attacks with effective rebuttals.
- Uncovered strategic performance gaps and opportunities to enhance HPC performance and AI inference with EPYC through in-depth competitive analysis of AVX512 and AMX accelerators on competitive Intel hardware. This analysis influenced current and future generations of EPYC architecture, ensuring AI/ML performance and TCO leadership.
- Directed customer co-design efforts with US DOE Customers with competitive hardware & software benchmarking, delivering the industry's best core software stack of Intel compilers, libraries, and performance analysis tools with targeted application performance optimizations, which facilitated widespread Intel Xeon CPU adoption.

Organizational & Executive Leadership:

- Established and directed global teams across Russia, China, and India, fostering collaboration, flexibility, and adaptability. Oversaw vendor relationships, contracts, and agreements, aligning strategic goals for business growth.
- Executed KPI-driven initiatives through collaboration across business units, aligning short- and long-term goals. Delivered high-impact projects on time & within budget by leveraging resource planning and forecasting. Partnered extensively with FAEs, Sales & Marketing as ONE TEAM to drive product growth and boost sales performance.
- Empowered teams through coaching, mentoring, and performance management. Created comprehensive training programs to scale knowledge and skills, driving individual career advancement and business growth.

Thought Leadership and Digital Transformation:

- Pioneered a performance warehouse dashboard with automated benchmarking of over 300 HPC, AI/ML, and Enterprise applications. Formulated quick-turnaround methodologies for A/B testing, identifying early hardware and software issues, and achieving product readiness & quality by B0 silicon. Boosted visibility across business units, creating bias for action, and accelerating business growth with a consistent cadence of product launches every year.
- Championed Intel's Shift-Left strategy, employing Agile methodologies to develop innovative pre-silicon model for IP validation as early as RTL 0.5. Accelerated silicon power-on and reduced time to market by ~6 months.
- Championed innovation and industry visibility with 26 patents and ~14 publications. Authored chapters in two HPC books published by Intel and served as product evangelist, chair and technical speaker at major conferences.

EDUCATION

- Master of Science (M.S.), Computer Science, Portland State University, Portland, Oregon
- Bachelor of Engineering (B.E.), Electronics and Communications Engineering, Birla Institute of Technology, India

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SKILLS

- Team Leadership & Management, Coaching, Mentoring, Talent Development, Global Cross-Functional Collaboration
- Strategy & Analysis, Planning & Execution, Merger & Acquisition (M&A), Business Development, Financial Acumen
- Research & Development (R&D), Thought Leadership, Customer & Partner Engagement & Success, Budgeting
- Market and Competitive Intelligence & Analysis, Innovation, Change Management & Digital Transformation
- Semiconductors, Product Quality, Product and Program Management, Agile Methodologies
- Datacenter, Cloud Computing, High-Performance Computing (HPC), AI/ML, Enterprise, Server and PC/Workstation
- Virtualization, Security, Confidential Computing, Reliability Availability & Serviceability (RAS)
- Industry Standard Benchmarks, Validation, Performance Characterization, Analysis & Optimization, A/B Testing
- Hardware-Software Co-Design, Simulation/Emulation, Pre & Post-Silicon Validation, Performance & Power Analysis
- SoC CPUs (x86: Intel, AMD, ARM: NVidia Grace Superchip, Ampere Altra Max, AWS Graviton), GPUs (Nvidia, AMD)
- Parallel Programming (C/C++, Fortran, Python, CUDA, Perl, Java, Assembly, MPI, OpenMP), Ray, Daft
- AI/ML (PyTorch, TensorFlow, scikit-learn, OneDNN, ONNX, LLAMA.CPP, Ampere Model Library AIO)
- Advanced Performance Analysis Tools (Intel VTune, AMD μProf, Nvidia Nsight, Prometheus, Grafana)
- Continuous Improvement: Lean, Kaizen, Agile, DevOps (Git, JIRA, Scrum, CI/CD, Kubernetes, Docker)

PATENTS / AFFILIATIONS / PUBLICATIONS

- 26+ Patents in area of SoC CPU Instruction Set Architecture (ISA)
- Represented in SPEC's JAVA committee, Super Computing (ISC & SC) Conferences
- Chaired large internal conferences for 1000+ engineers, owned tracks and delivered presentations such as Design Test & Technology Conference (DTTC), MVSLE, Intel Managed Runtime & Software, and program Chair of International Super Computing (ISC) 2015 Intel Bird of Feather Session & Workshop
- IEEE 2023 Cluster & American Institute of Aeronautics and Astronautics (AIAA) Conference Papers, 2023-2024
- Co-authored tutorial on "Vectorization Strategies for Intel's 2nd generation Intel Xeon® Phi™ architecture codenamed Knights Landing" with NERSC & Argonne Labs presented at Super Computing 2016
- Authored "Programming with AVX-512 Intrinsics" in Intel's Xeon Phi Processor High Performance Programming Knights Landing Edition book, 2016
- Co-authored "Porting the MIMD Lattice Computation (MILC) Code to the Intel Xeon Phi Knights Landing Processor", IXPUG, International Super Computing 2016
- Co-authored "Numerical Weather Prediction Optimization" with NOAA Engineers in Intel's High Performance Parallelism Pearls: Multicore and Many-core Programming Approaches book, Volume 2, 2015
- Program Chair of International Super Computing (ISC) 2015 Intel Bird of Feather Session & Workshop
- Co-authored "Porting and Tuning WRF Physics Packages on Intel Xeon and Xeon Phi and NVIDIA GPU", ECMWF (European Centre for Medium-Range Weather Forecasts), 2014
- Presented "Atom Microarchitecture & Perf. Optimization BKM's", Software Engineering Summit (SES), Microsoft, European National Labs (CERN) 2011, "Optimizing Java Apps for Intel Architecture", SES 2004, "Performance Characteristics of Java Performance Optimization of ECperf on Intel® Itanium 2", Managed Runtime Summit, 2002
- Improvements in the Intel Core2™ Penryn Processor Family Architecture and Microarchitecture, ITJ 2008
- Co-authored "A Comparison of SPECjAppServer2002 and SPECjAppServer2004" CAECW-05, 2005
- Co-authored "Characterization of Java Appl. Server Workloads", IEEE 4th Annual WWC MICRO-34, 2000