Neil Dobler

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Project Execution Leader | Program Manager | Engineering Manager

Technical leader and technical program manager with extensive experience for an industry leader in creating world-changing technology and its flagship CPU products. Expertise in leading and developing teams, program management of full CPU IP RTL execution and validation, and delivering the full life-cycle; from architecture through deployment, delivering top-tier results on Intel's E-Core CPU IP and silicon test interfaces. An exceptional communicator with a proven track record of regularly updating upper management on program progress, adept at integrating multiple design teams into a cohesive and well-functioning group, and effective with resolving conflicts between technical experts.

Areas of Expertise

Program Management | Project Management | Team Leadership | Stakeholder Management
CPU IP & SoC Silicon Development | Design for Test (DFT) | JTAG | System Verilog | Logic Design
Mentoring | Coaching | MS Excel | PowerPoint | MS Project

Professional Experience

Intel Corporation June 2014 - September 2024

RTL Project Manager and Cluster Manager, Intel E-Core (1/2019 – 9/2024)

- Facilitated a collaborative working group, involving key design and validation leaders, to establish project RTL implementation and validation timelines for all CPU IP deliverables. Successfully navigated evolving project requirements, meticulously monitored deliverables, directed the rebalancing of work and resources, and effectively communicated progress to multiple levels of senior management, ensuring on-schedule delivery and seamless project execution. Fostered collaboration with multiple SOC customers, ensuring delivery of IP drops that consistently met or exceeded quality guidelines.
- Technical manager of Memory Execution Cluster (MEC) RTL design team and led execution management for entire MEC cluster, encompassing architecture, RTL design, and validation. Directed feature scoping, implementation, and production closure across multiple E-Core product generations. Enhanced team execution, with significant restructuring of cluster execution processes, achieving a *3-fold* reduction in post-tapeout bug rates, between IP generations.

Cluster Manager/DFT Lead, Intel - Next Gen Core (7/2016 – 12/2018)

- Managed design team, through pathfinding, for a generational update to Memory Execution Unit (MEU) cluster. Developed a detailed implementation plan, collaborated with architecture team on high-level specifications, oversaw scope management, and presented plan for approval.
- Devised a cost analysis of mux-d vs. LSSD scan cell area/power/perf study, working with multiple scan owners, around Intel. Led IP DFx team through pathfinding of functional debug features including ProbeMode and debug trace.

Engineering Manager and DFx Lead (6/2014 – 6/2016)

- Oversaw DFx team responsible for delivering test fabrics to multiple SOC designs.
- Directed a small team developing and delivering DFT (array and scan test) for Intel Atom CPU and north complex as a HIP. Collaborated with external customer to understand SOC environment and educated them on requirements of Intel-delivered HIP.

Additional Experience

Senior Designer, Intel SOC highspeed test fabric

- Led a team to spearhead first deployment of high-speed test fabric subsequently used on all Intel SOCs. Worked through issues in architecture, timing, and structural design.
- Interfaced with architects and designers from across Intel to develop specification for scalable high-speed test fabric.
- Served as virtual Team Lead for the team implementing DFT, on two Intel SOCs.

Architect and Lead Design, TAP and DFx special circuits

- Architected TAP (JTAG IEEE1149.1), Multicore Interface (MCI – high speed parallel tester fabric), and on chip debug control logic, on Haswell and Broadwell CPUs.
- Virtual team lead over architecture, design and validation, for all DFx areas, excluding scan and memory test.
- Directed work to implement auto adjusted JTAG registers based on custom hierarchical XML documentation, enabling accurate post-silicon tool definitions and faster power-on effort.

Lead designer, TAP and MCI Tester Fabric

- TAP and MCI micro-architecture and RTL execution owner for Nehalem, Lynnfield, and Westmere generation of Intel CPUs.
- Micro-architect and RTL owner for Intel's first multiple TAP client die. Implemented TAP chains for all debug features and supported use in post silicon efforts.
- MCI circuit owner of hand drawn cell-based design.
- Drove tester debug lab use of die test interfaces for scan and array testing.

Circuit Design and Cluster Timing Owner

- Drove memory cluster physical design for late Prescott revisions, implemented ECOs, and converged timing to tighter targets.
- Small signal array owner for post A step Prescott steppings. Performed spice simulations for design convergence in all PVT corners.
- Addressed and resolved partition timing issues, for Highspeed Execution cluster, for initial Prescott stepping.
- Vertical design owner for global and bimodal arrays and timing owner in Front End Cluster of Northwood steppings.

Education

Bachelor of Science (B.S.), Electrical Engineering

University of Idaho, Moscow, ID