JYOTIRMOY GHOSH

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SUMMARY:

Hands-on technical leader with a wide range of experience in chip design, specializing in the field of physical design of machine learning ASICs, server processors for high performance computing, and low-power mobile chips for wireless applications using advanced technology nodes.

- Synthesis, Floor Plan, Place and Route, Full Chip Integration, Static Timing Analysis
- RTL Power Estimation, Low Power Methodology, Power Convergence for large chips
- Nanosheet (Gate All Around FET), Backside power delivery, Multi-Die Chip Packaging
- Evaluation of IPs, Design Technology co-optimization for cutting-edge technologies
- Successfully taped out chips at 18A, 3nm and higher process nodes with Intel and TSMC
- Collaboration with cross-functional global design teams, foundries, IP and EDA vendors

EDA TOOLS PROFICIENCY:

- **Synopsys:** Fusion Compiler, RTL Architect, PrimeTime, PrimePower
- **Ansys:** PowerArtist, RedHawk
- **Cadence:** Innovus, SoC Encounter, RTL Compiler, Voltus

PROFESSIONAL EXPERIENCE:

Intel Corporation **2014 - Present**
Senior SoC Design Lead

- Technical lead for physical implementation of high-performance Xeon processor SoCs for data centers and cloud computing. Driving methodology for power estimation and power convergence for server chips at 3nm node. Streamline execution flow for emerging nodes by working closely with foundry and adopting design/process co-optimization techniques.
- Leading the RTL power validation effort for server SoCs to provide early feedback to designers on the quality of the RTL and estimate the achievable power. This initiative provides a short loop between logic changes and the impact on power, rather than waiting for post-route power data after construction. Close collaboration with the tool vendors helped detect power bugs in design and led to many tool enhancements for better quality of results and runtime improvements. Parallel execution of power validation by both IP and SoC designs ensures a predictable power for each IP when integrated into SoC.
- Lead the implementation activities of Intel Nervana family of Neural Network Processors for deep learning ASICs. Responsible for floor planning, power optimization and analysis, full chip integration of the hardware accelerator chips using high bandwidth memories. Worked with foundries, geographically diverse design teams, multiple IP and ASIC vendors to deliver chips in a schedule intensive environment.
- Evaluation and enablement of technologies at 14nm/10nm/7nm/3nm/18A/14A nodes by interfacing with foundry, tool vendors and set up integration methodology for processor cores and IPs that enable die-to-die interconnect of multiple chiplets within a package.
- Involved in the scalable design methodology initiative within the company to address the engineering challenges in cutting-edge silicon process validation amid increasing complexities, heterogeneous products, and rapid technological advancements.
- Involved in the hiring, training, and leading a team of junior engineers to success.

Sandforce / LSI Corporation **2012 - 2014**
Principal Engineer

- Physical implementation of flash memory controller chips for solid-state drives (SSDs) using TSMC 28nm and 40nm process technology – responsible for physical synthesis, floor planning, place and route, timing analysis, noise analysis, power analysis, eco implementation and physical verification for top level and some major complex blocks.
- Engaged with EDA tool vendors as beta customers to benchmark tools and integrate these tools in the chip production flow.

Broadcom Corporation **2010 - 2011**
Physical Design Consultant

- Worked on the physical design of a low power wireless chip at 40nm process technology.
- Implemented various power saving techniques to reduce dynamic and leakage power consumption of the chip – clock gating, multiple threshold voltage cells, voltage islands, power shut-off using power gating cells, dynamic voltage frequency scaling (DVFS).
- Performed static and dynamic power analysis, EM and IR drop analysis.
- Responsible for parasitic extraction, timing closure, crosstalk, and noise analysis.

Tabula, Inc. **2007 - 2009**
Senior Staff Engineer

- Led the physical design activities for a family of programmable chips with high speed SerDes and DSP capability using 40nm TSMC process technology.
- Set up the flow and methodology from scratch for the digital logic blocks.
- Implemented novel design techniques to achieve desired speed and power requirements.
- Co-ordinate between circuit and logic designers to ensure optimal progress of digital and analog teams towards meeting project schedule.

ATI Technologies **1999 - 2006**
Senior Engineer

- Worked on the physical implementation of several generations of the high-performance Radeon family of graphics processors (GPUs) and video game console chips, across various process technologies ranging from 1.5um to 65nm.
- Set up the DFM flow and methodology to mitigate manufacturing risks arising due to process variations in the smaller geometries.
- Evaluate and benchmark commercial EDA tools and flow deployment using them.
- Developed and supported new in-house utilities to facilitate the production flow.

EDUCATION:

M. Phil. in Microelectronic Engineering and Semiconductor Physics, Cambridge University, UK
B. Tech. in Electronics Engineering, University of Calcutta, India