NEH PRATIKKUMAR PATEL

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Education

MS: Electrical Engineering, 2021
San Jose State University

BE: Electrical Engineering, 2019
Gujarat Technological University

Work Experience

Senior Silicon Design Engineer, 01/2022 to Current
AMD

- Debugged C/C++-based random stress test patterns for FPGA functional verification, resolving setup/hold time, temperature, and voltage failures to ensure pattern reliability across 7nm, 14nm, and 16nm devices.
- Generated and validated JTAG, UART, SCAN, MEM CLEAR, BIST, BISR, and MBIST patterns, supporting ATE handshake and FPGA integration via Vivado.
- Developed Python and tcl scripts to automate test workflows, boosting team efficiency.
- Collaborated with cross-functional teams to align test patterns with DFT objectives, enhancing SoC testability for ARM A78/A72 dual/quad-core CPUs.

Digital Test Development Intern, 06/2021 to 08/2021
Analog Devices

- Validated JTAG using Teradyne's Ultraflex Tester, enhancing test coverage and pattern efficiency.
- Debugged and refined failing patterns generated from wgl files, demonstrating strong problem-solving skills.
- Conducted SPI functional testing and characterization using the Ultraflex Tester, contributing to robust testing methodologies.
- Developed, verified, and validated tester patterns while utilizing waveform tools.

Projects

High-Performance Cache Controller

- Developed a cache controller for a CPU, integrating prefetching and cache coherency protocols to minimize access latency and maximize hit rates.
- Optimized the design for power, performance, and area (PPA), ensuring efficient resource utilization while meeting performance targets.
- Collaborated with cross-functional teams to refine the microarchitecture and ensure alignment with functional and physical implementation goals

Timing Closure for ALU Block

- Performed timing analysis and optimization for an Arithmetic Logic Unit (ALU), using synthesis and place-and-route tools to meet critical timing constraints.
- Implemented clock gating and other power-saving techniques to reduce dynamic power consumption while maintaining performance.
- Ensured the design met area, reliability, and testability requirements, addressing key physical design challenges in CPU subsystem implementation.

4-Bit Counter with Scan Chain

- Developed a 4-bit counter with scan chain insertion using Verilog and OpenROAD, verified functionality via test benches in Icarus Verilog, targeting VLSI testability.

Skills

Languages: Verilog, SystemVerilog, C/C++, Python

VLSI: DFT (Scan Chains, BIST, MBIST), DV (Testbenches, Assertions), Static Timing Analysis, Digital Logic Design

Tools: Vivado, Icarus Verilog, OpenROAD, Teradyne UltraFLEX, Waveform Tools

Concepts: CMOS, Low Power Design, JTAG, Computer Architecture