NATHAN MAI

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SKILLS AND EXPERTISE

Design & Verification Tools: VCS, DC compiler, LINTRA, Verdi, Debussy, DVE, JasperGold
Programing Languages: Verilog, System Verilog, C, PERL, Shell-Scripting
Methodologies: OVM/UVM, OOPs concept, Constraint Driven Verification, Formal Verification

- Expertise in all aspect of UVM methodology for the purpose of ASIC/CPU Design Verification
- Strong background in ARM architecture and associated verification strategies
- Experienced with using JasperGold for formal verification
- Ability to lead small teams and mentor junior engineers in a collaborative environment
- Strong debugging skills - with emphasis on exposing bugs, regression triage, coverage hole analysis and achieving tapeout closure

WORK EXPERIENCE

Ampere Computing

Cpu Verification Engineer *February, 2018 – Present*

- Work on functional verification of the Front-End Instruction Fetch Unit of ARM-based CPU cores, owning multiple sub-block features within Branch Predictor and Fetch units
- Built a unit level testbench from the ground up (with emphasis on re-use at chip-level DV) that includes: DV environment, passive & active agents, BFM, checkers/scoreboards, regmodel, and stimulus generation
- Derive Testplans from features design specifications and responsible for maintaining regressions with the focus on exposing RTL bugs and driving coverage closure all the way to tapeout milestone
- Lead workgroup to debug & triage, identifying RTL bug root causes and coordinating fixes with design team
- Developed a test generator to serve as the primary stimulus provider for the Instruction-Fetch Unit, yielding diverse and effective randomized stimulus to thoroughly exercise the ICF
- Use JasperGold formal verification tool (SVA) to assist with: assertion coding and proofing, coverage analysis and enhancement, ensuring high-quality first-pass code during development
- Conduct Performance correlations to debug and triage, exposing bugs around clock-gating logics

Qualcomm Inc. (Modem Group)

Senior Verification Engineer *August, 2016 – February, 2017*

- Ownership of block-level verification development for the modem's decoder 3G/4G block
- Responsible for bring up and maintain of test bench components and development of complex checkers/scoreboards from scratch using UVM components
- Developed assertion (SVA) to ensure design pipeline throughputs meet the requirements
- Develop directed tests using vectors, constraint random tests using DPI-based stimulus from input generator, and maintain target regressions according to the test strategy for each milestones

Intel Corporation

Senior Verification Engineer *August, 2011 – July, 2016, February, 2017 - February 2018*

- Part of the Intel's Data Center Group that owned Intel's enterprise networking SoC products
- Assumed various digital verification roles that spans across full-chip SOC to unit-level development
- Responsible for test plans development and driving test plans execution to tape-out

EDUCATION

Master of Sciences in Electrical Engineering
San Jose State University, San Jose, CA Graduated: June, 2011

Bachelor Degree in Electrical Engineering
University of California, Riverside Graduated: June, 2008