RAJASEKHAR NARALA

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SUMMARY

- Design Verification Lead with 10+ years of experience in validating high-performance GPUs and accelerators.
- Expertise in UVM-based testbenches, optimizing verification flows, and driving successful product launches.
- Proven track record in verifying complex GPU subsystems such as shaders, rendering pipelines, and compute units, consistently improving verification efficiency and product quality.

TECHNICAL SKILLS

Verification Methodologies	:	UVM, System Verilog, Verilog HDL
Programming Languages	:	C++, Perl, Python, TCL
Version Control & Collaboration	:	Git, Perforce, JIRA
Simulation & Debug Tools	:	VCS, Verdi, Jasper Formal
Graphics APIs & Emulation	:	OpenGL, DirectX, CUDA, ZEBU Platform

PROFESSIONAL EXPERIENCE

Staff GPU Design Verification Engineer ***Intel, Folsom CA*** *Nov 2021 – Present*

Shader (GPU/ML Core) Subsystem

- Led design verification of the SIMD dispatch and instruction execution sub-system, improving verification efficiency by 50% through testbench migration to UVM and reducing regression cycles.
- Defined verification plans and coverage with architects to expedite feature validation.
- Served as the primary contact for GPU simulation triages and post-silicon bug reproduction, resolving critical issues.
- Optimized testbench with the PPA team for power and performance micro-tests, enhancing testing efficiency.
- Developed end-to-end checks for silicon performance events, identifying and resolving functional issues.

MTS GPU Verification Engineer ***AMD, Orlando FL*** *Jan 2020 – Oct 2021*

Performance analysis via HW Emulation

- Executed game frames in HW EMU, resolving critical functional and performance issues for left shift validation.
- Ran compute workloads on the graphics core, generating performance data to optimize the MI200 Platform.
- Captured performance data and debugged firmware to enable RISCV adoption in next-gen command processor.

Design Verification of Geometry Sub-system (RDNA3)

- Developed C++ test content for new features, including test plans and coverage analysis for full validation.
- Updated fixed-function shader test suites for next-gen ISA, enabling rigorous testing of the new geometry pipeline.

Senior GPU Design Verification Engineer ***Intel, Folsom CA*** *Jul 2015 – Dec 2019*

RTL Design: Pixel Shader Scheduler

- Co-led micro-architectural changes, interface definitions, and design spec implementation details.
- Expert in pipeline design, data synchronization, muxing, assertions, and observation architecture.
- Implemented logic solutions for timing convergence through synthesis report analysis.
- Developed and implemented unit-level clock gating and formal verification, reducing power consumption by 30% and improving timing convergence.
- Collaborated with the physical design team on partitioning, placement optimization, timing, and gate savings.

Design Verification: Pixel Front-End Sub-system

- Led functional verification and debugged failures ensuring compliance with specifications.
- Created test plans, monitors, C++ checkers, and developed functional coverage from the ground up.
- Developed Perl subroutines to auto-randomize register programming and generate tests based on design changes.
- Doubled compilation and simulation speed by optimizing log dumping and coverage bins.
- Managed weekly regression runs and automated large-scale testing, ensuring efficient logging.

PROJECTS AND ACHIEVEMENTS

- Published Verification Methodology: Intel's *"Design for Test and Technology Conference" (DTTC)* 2019.
- Contributed to validation of advanced features like Variable rate shading and Variable registers per thread.

EDUCATION

Master of Science in Electrical Engineering *Arizona State University, Tempe* *Aug 2013 – May 2015*

BE Electronics and Instrumentation *BITS, Pilani* *Aug 2009 – May 2013*