Summary:

Shreya Mahetaliya is a Master's student in Electrical and Computer Engineering at the University of Washington, Seattle, specializing in ASIC design and computer architecture. She has experience in RTL design, verification, and low-power architectures, with a focus on ARM-based processors and hardware accelerators. She has also worked extensively with tools like Vivado, Synopsys DC, and Cadence for synthesis, timing analysis, and physical design.

Name: Shreya Mahetaliya

Email: shmahetaliya@gmail.com

Phone: 2063803859

Location: Seattle

Country: USA

Position Category: Design: Logic design, Verification: Design verification, Architecture

Desired Job Role: ASIC Design Engineer

University: University of Washington, Seattle, K. J. Somaiya College of Engineering, Mumbai, India

Degree: MS in Electrical and Computer Engineering, Bachelor of Technology in Electronics

Graduation Year: 2025, 2021

Years Experience: 2

Notable Companies: JumpStartCSR, Seattle, USA, Accenture, Mumbai, India

Top Skills: Programming languages: C, C++, Java, Python, Verilog/SystemVerilog, HTML, CSS, SQL, RTL Design, Coverage, Microprocessors and Microcontrollers, Tools and Software: Cadence (Genus, Innovus, Conformal LEC, Tempus), ModelSim, Quartus, MATLAB, LTspice, AutoCAD, Arduino IDE, SAP, Linux, Proteus, Eagle

Job Intention: full-time

Visa Status: --

Able: yes

Subject: Inquiry About Full-Time and Spring Internship Opportunities

Date Sent: 03-19-2025

Resume: Yes