NIKHIL PILLAI

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Highly motivated and experienced CPU physical design and STA engineer with 9+ years of experience involved in designing high speed CPU and server designs with expertise in Synthesis to GDS flow and timing convergence. Very well versed with logic equivalency verification (FEV) and debugging. Seeking challenging opportunities to develop my skills and grow in my career.

INTEL COPORATION (Hillsboro, OR)

- **CPU Physical Design Engineer** **March 2016 – Present**
  - Experience in full back-end flows, RTL-to-GDS, for high frequency designs in the GHz range and 1M+ gates consisting of RTL Logic Synthesis, floor-planning, place-and-route and Static Timing Analysis using Primetime.
  - Experience in Clock Tree Mesh, Multi-Source Clock Tree and traditional Clock Tree Synthesis flows, their tuning and debug to achieve good clock latency and reasonable clock skew and ECO flows.
  - Experience in feasibility analysis for critical micro-architecture paths and power analysis using PTPX.
  - Understanding of methodologies like the AOCVM, Path Based Timing Analysis (PBA).
  - Responsible for debugging Logical non-equivalency (FEV) using the Cadence Conformal LEC tool for multiple partitions and giving feedback to RTL/SD team to rectify the issues.
  - Self-sufficient with debugging issues in any underlying flows and good understanding in process variation and their impact in Power, Performance and Area.
  - Savvy with automation & scripting (TCL, Perl, Python and UNIX shell scripting).
  - Experienced in tech nodes: 14nm (Intel Xeon Phi server product) to 1.8nm (Xe4 graphics architecture)

HONORS AND AWARDS:

- **Division Recognition Award** **April 2024**
  - Created the project's (High performance CPU Core) first power maps which is usually done by other cores far later in the design. This enabled the project to aggressively address the thermal challenges that are increasingly the performance limiter of other cores.
- **Division Recognition Award** **July 2022**
  - Development and Deployment of Several Enhancements to Existing FEV Flows and methodology.
- **Superior Achievement** **August 2019**
  - For forming a multi-geo effort to dive into a critical gap in the project's FEV tool flow, methodology, and collateral and then conducting project-wide training and execution facilitation.

TECHNICAL SKILLS:

- Scripting: Tcl, Perl, Shell, Python
- Tools: Synopsys Fusion Compiler, Primetime, PTPX, Cadence Conformal LEC

EDUCATION:

- Master's in computer engineering, Arizona State University **May 2015**
- Bachelor of Engineering, University of Mumbai **May 2012**