# CURRICULUM VITAE

**First name / Surname:** ALIN PETRU PARCALAB

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**Date of birth:** OCTOBER 29, 1998
**Place of birth:** ORADEA, ROMANIA
**Citizenship:** ROMANIAN
**Marital status:** MARRIED

**Experience:**

- ALLENGRA GmbH – Microarchitecture & RTL Design – "Arcino: Ultra-Low Power RISC-V IMC uC, 180nm". 2018 – 2019.
- ALLENGRA GmbH – Lead Developer – Microarchitecture & RTL Design – "ALLI01: Universal Measurement ASIC, Very High-Resolution TDC & ADC Based". 2019 – 2022.
- ALLENGRA GmbH – Lead Developer – Microarchitecture & RTL Design – "Bynar5: 2 Issue OoO RISC-V IMFC Core, 180nm". 2021 – 2022.
- Capgemini Engineering – Senior Design Engineer – RTL Design – "High Speed Signal Processing Unit (HSSP)". 2022
- Capgemini Engineering – Senior Design Engineer – RTL Design – "Processor Subsystem Automatic Generation Methodology". 2022
- Capgemini Engineering – Senior Design Engineer – Integration – "IO Subsystem for Automotive application". 2023
- Capgemini Engineering – Senior Design Engineer – Microarchitecture & RTL Design – "CHI RN-F Bridge". 2024

**Skills and knowledge of tools:**

- **Programming languages:** C, C++, Python, Pearl, Assembly (x86, RISC-V).
- **Programming development tools:** Visual Studio, Eclipse, Matlab & Simulink, Make Files.
- **Hardware description languages:** VHDL, Verilog, System Verilog.
- **Hardware development tools:** Xilinx Integrated Software Environment (ISE), Xilinx Vivado, Mentor Graphics ModelSim DE, Mentor Graphics Questa Pro, Mentor Graphics Oasys-AMS, Mentor Graphics Leonardo Spectrum, Tanner S-Edit, Tanner T-Spice, Tanner L-Edit, Mentor Graphics Calibre, Synopsys VCS, Synopsys Prime Time, Synopsys Prime Power, Synopsys Spyglass, Synopsys Design Compiler (DC), Synopsys Formality Equivalence Checking, Verilator.

**Skills:**

- RTL Design
- Schematics Analog & Digital
- Static Timing Analysis (STA)
- Clock Domain Crossing (CDC)
- Logic Equivalence Checking
- Synthesis (DC-Compiler)
- Low Power Design
- Asynchronous Design
- Micro Architecture

**Knowledge of:**

- Cache Architecture
- Virtual Memory
- Memory Models
- Micro-Op Fusion
- Branch Predictors (2BC, Gshare, Tage, Perceptron, Loop Predictor, BTB)
- AI Accelerators
- Super Scalar Core
- OoO Scoreboard Back-end
- OoO The Data-in-ROB Design (Implicit Renaming)
- OoO The Physical Register File Design (Explicit Renaming)
- Very High-Resolution Time to Digital Converters (TDC)
- Delta Sigma / Flash / SAR Analog to Digital Converters
- AXI4, Tile Link, Avalon, CXL, CMN-700, CMN-600, NIC-450, UCIe
- SPI, I2C, XTAL, UART, JTAG
- Memory Controller
- RISC-V

**Papers of interest:**

- Design Issues and Tradeoffs for Write Buffers - Kevin Skadron and Douglas W. Clark
- Virtual-Channel Flow Control - William J. Dally
- A High-Performance Hierarchical Ring On-Chip Interconnect with Low-Cost Routers - Chris Fallin, Xiangyao Yu, Gregory Nazario Onur Mutlu
- Implementing Precise Interrupts in Pipelined Processors - James E. Smith and Andrew R. Pleszkun
- Data Cache Prefetching Using a Global History Buffer – Kyle J. Nesbit and James E. Smith
- An Overview of Virtual Machine Architectures - J. E. Smith and Ravi Nair
- Complexity-Effective Superscalar Processors - Subbarao Palacharla, Norman P. Jouppi, J. E. Smith
- Select-Free Instruction Scheduling Logic - Mary D. Brown, Jared Stark, Yale N. Patt
- The Microarchitecture of Superscalar Processors – James E. Smith and Gurindar S. Sohi
- On Pipelining Dynamic Instruction Scheduling Logic - Jared Stark, Mary D. Brown, Yale N. Patt

- Dynamic Speculation and Synchronization of Data Dependences – Andreas Moshovos, Scott E. Breach, T. N. Vijaykumar, Gurindar S. Sohi
- A Study on Memory Dependence Predictor - Danni Wang and Yuting Liu
- Memory Dependence Prediction using Store Sets - George Z. Chrysos and Joel S. Emer
- A Primer on Memory Consistency and Cache Coherence - Daniel J. Sorin, Mark D. Hill, David A. Wood
- THE ALPHA 21264 MICROPROCESSOR – R. E. Kessler
- The Alpha 21364 and 21464 Microprocessors: Continuing the Performance Lead Beyond Y2K - Shubu Mukherjee
- Runahead Execution: An Alternative to Very Large Instruction Windows for Out-of-order Processors - Onur Mutlu, Jared Stark, Chris Wilkerson, Yale N. Patt
- IEEE Standard for Floating-Point Arithmetic
- Modern Processor Design – John Paul Shen Mikko H. Lipasti
- Design Issues and Tradeoffs for Write Buffers - Kevin Skadron and Douglas W. Clark
- Value Prediction Focalized on CPU Registers - Lucian Vintan, Arpad Gellert, Adrian Florea
- Focalising dynamic value prediction to CPU's context - L.N. Vintan, A. Florea and A. Gellert
- The Predictability of Data Values - Yiannakis Sazeides and James E. Smith
- Single and Multi-CPU Performance Modeling for Embedded Systems - Trevor Conrad Meyerowitz
- Trace Scheduling: A Technique for Global Microcode Compaction - JOSEPH A. FISHER
- Dynamic Branch Prediction with Perceptrons - Daniel A. Jiménez, Calvin Lin
- Take A Way: Exploring the Security Implications of AMD's Cache Way Predictors - Moritz Lipp, Vedad Hadžić, Michael Schwarz, Arthur Perais, Clémentine Maurice, Daniel Gruss
- Cache Write Policies and Performance - Norman P. Jouppi
- Flexible Register Management using Reference Counting - Steven Battl, Andrew D. Hilton, Mark Hempstead, Amir Roth
- Checkpoint Repair for Out-of-order Execution Machines – Wen-mei W. Hwu and Yale N. Patt
- A Survey of Techniques for Dynamic Branch Prediction - Sparsh Mittal
- Evolution of the Samsung Exynos CPU Microarchitecture - Brian Grayson, Jeff Rupley, Gerald Zuraski Jr., Eric Quinnell , Daniel A. Jiménez, Tarun Nakra, Paul Kitchin, Ryan Hensley, Edward Brekelbaum, Vikas Sinha, and Ankit Ghiya
- Two-Stage, Pipelined Register Renaming – Elham Safi, Andreas Moshovos and Andreas Veneris
- A case for (partially) TAgged GEometric history length branch prediction - Andre Seznec, Pierre Michaud
- PRINCIPLES AND PRACTICES OF INTERCONNECTION NETWORKS – William James Dally and Brian Towles


**Education:**

- Bsc (Present): in Electronics and Computer Science, October 2019, at University of Oradea, Romania.

**General knowledge:**

- Microsoft Windows / Linux
- Microsoft Office / Only Office
- x86
- Bashrc
- Hyper transport technology

**Languages:**

- Romanian: native speaker.
- English: fluent.
- German, French: very basic.

**Interests and hobbies**:

- Violin
- Processor Cores (OoO Implementations)
- RISC-V
- Programming Language Analysis