Dear Hiring Team,

My name is Harshith, and I am a Hardware Design Engineer with over 3 years of experience specializing in FPGA/SoC architectures and RTL-to-GDSII ASIC design flow. I bring hands-on expertise in RISC-V, MIPS, and ARM-based systems, with practical experience in subsystem design, integration, and custom IP development aimed at optimizing performance, power, and area (PPA).

Having contributed to multiple tape-outs and worked extensively on RISC-V-based SoC projects, the idea of building CPU core from ground up is always intriguing. The open-source nature of RISC-V makes every engineer a potential contributor and a competitor. I strongly believe RISC-V will define the future of computing, and Im excited to help push those boundaries forward.

I am eager to contribute to your growth story and making your success story a part of mine. I've attached my resume for your review and would welcome the opportunity to connect further.

Looking forward to hearing from you.

Best,

Harshith Reddy