Jesús Francisco Sánchez-Blanco

Contact

+52 33 1332-3544

chuchoblanco69@gmail.com
jesus.sblanco@academicos.udg.mx

LinkedIn
www.linkedin.com/in/jesús-francisco-sánchez-blanco-a128031

Objective

Continue working on research and development of electronic and computing systems, mainly focused in the analysis, design, implementation, execution, and debug of tests that support their quality, verifiability, and validity; all by using advanced and innovative technics

Summary

I am Electronic & Computing Engineer with more than 9 years of experience in SW testing for embedded systems within the automotive sector, more than 7 years of experience in functional validation of leading mission critical and microserver microprocessors, and 6 years of experience in the design of automatic control systems and telecommunication products.
Throughout my working life I have worked with many programming languages and development tools such as: C, C++, Python, Prolog and batch scripting, among others.

Work Experience

CONTINENTAL Automotive

San Pedro Tlaquepaque, Jal, MX. 2015-2024

Senior Staff SW Test Engineer. 2019-2024

- Leading SW test activities for R&D FPC team.
- Developing unit, component, integration, system, and acceptation SW tests for automotive Linux based embedded systems.
- Implementation of such SW tests using Google Test, C language, Python, and batch shell scripting.
- Test plans, test specifications, and test strategies realization.
- SW testing training of new entrance engineers.

Senior SW Test Engineer 2016-2018

- Design and implementation of functional tests to verify/validate the SW of a family of automotive digital clusters.
- Enabling automatic test execution.
- Debugging issues for a Linux based SW platform for automotive applications which was coded in C and C++.
- Issues solving implementation.
- Participation on innovation tasks.

SW Test Engineer 2015-2016

- Designing and implementing PRQAC QAC based static code analysis for Linux based C code.
- Developing SW unit tests for Linux based C code by using Cantata++ and GCOV tools.
- Process development for automatic test execution into the product electronic board.
- Designing, enabling, and executing SW manual tests for automotive digital clusters.

INTEL Tecnología de México

San Pedro Tlaquepaque, Jal, MX. 2007-2014

System Validation Engineer

Perform system validation activities for the next products:

- **Denverton** 2013-2014
  SoC 14nm Atom based cores.
  - ✓ Tests definition for validating SMBus, HSUART, and RASUM features.
  - ✓ Make test plan to perform SMBus, HSUART, and RASUM post-silicon validation.
  - ✓ Participating in test platform design.
  - ✓ Emulation execution of the tests plans.
- **Avoton** 2012-2013
  C23XX, C25XX & C27XX SoC 22nm Atom based cores.
  - ✓ Tests definition for validating SMBus, Legacy block, and RASUM features.

In parallel, I have maintained a continuous academic life of more than 28 years teaching undergraduate and graduate level courses, having 10 publications and 2 thesis as an advisor.

Specializations

- SW Testing.
- µP System Validation.
- Linux C programming.
- Scripting, Python, C, and C++ programming
- DES Control

Languages

- Spanish (native).
- Proficient in English (B1-B2).

Certifications

- ISTQB Certified Tester – Agile Tester Foundation Level Extension. 2019.
- ISTQB Certified Tester, Foundation Level. 2019.

Diploma

- Interactive Pedagogy. Universidad del Valle de Atemajac. 2004.

Additional Trainings

- ISTQB Test Manager.
- Advanced Linux, 2022.
- Machine Learning.
- Leadership Development Program – Level 1.
- ISTQB Agile SW Testing Methods.
- Scrum Methodology.
- ISTQB SW Testing Foundations.
- Creativity & Neurosciences.
- Problem Solving.
- Linux, 2016.
- UML, 2015.
- iA64 Architecture, INTEL GDC, 2010.

  - ✓ Make test plan to perform SMBus, Legacy block, and RASUM post-silicon validation.
  - ✓ Enabling and emulation/post-silicon execution of the tests plans.
- **Briarwood** 2011-2012
  S12XX SoC family 32nm Atom based cores.
  - ✓ Tests definition for validating SMBus and RASUM features.
  - ✓ Make the test plan to perform SMBus and RASUM post-silicon validation.
  - ✓ Enabling and emulation/post-silicon execution of the tests plans.
- **Poulson** 2010-2011
  Itanium 9500 series 32nm mission critical µP.
  - ✓ Tests definition for validating Memory RASUM features: **Demand & Patrol Scrubbing, Rank & DIMM Sparing, Memory Line Sparing, Memory Mirroring, Memory Migration,** and **Memory Hot Add/Remove.**
  - ✓ Tests definition for validating System RASUM features: **CPU/IOH Hot Add/Remove,** and **System Partitioning.**
  - ✓ Tool support for validating RASUM features.
- **Tukwila** 2007-2009
  Itanium 9300 series 64nm mission critical µP.
  - ✓ Tests definition for validating Memory & System RASUM features.
  - ✓ Make test plan to perform both Memory & System RASUM post-silicon validation.
  - ✓ Enabling and emulation/post-silicon execution of the tests plans.
  - ✓ Debugging issues and reporting bugs.
  - ✓ Tool support for validating RASUM features.

Previous Jobs

1992-2000

AgroInTec S.A. de C.V.

Puebla, Pue, MX. 1998-2000
Control System Engineer

MIXBAAL

Zapopan, Jal, MX. 1997-1998
Firmware Development Engineer

Sistema de Información y Comunicación del Estado de Puebla – Government Office

Puebla, Pue, MX 1996-1997
Head of the Data Network Area

Dirección General de Tránsito del Estado de Puebla – Government Office

Puebla, Pue, MX. 1995-1996
Informatic Area Leader

Automatización Avanzada de México

Puebla, Pue, MX. 1993
Automatic Systems Development Engineer

Soft Skills

- Teamwork.
- Problem-solving.
- Critical thinking.
- Emotional intelligence.
- Customer service.
- Goal-setting.
- Empathy.
- Innovation.
- Resilience.
- Strategic thinking.

Hobbies

- Scientific reading.
- Hiking.
- NFL fan.

PEPSI Co. – Grupo Herdomo
Puebla, Pue, MX. 1992
Engineer Jr

Education

Ph.D. Electrical Engineering
Centro de Investigación y Estudios Avanzados del Instituto Politécnico Nacional.
Guadalajara Jal, MX, 2001-2005 – Not completed.

M.Sc. in Electronics
Instituto Nacional de Astrofísica, Óptica y Electrónica.
Tonantzintla Pue, MX, 1993-1997.

Bachelor in Electronics Engineer
Universidad Autónoma Metropolitana – Iztapalapa
CDMX, MX, 1988-1992.

Teaching

Universidad de Guadalajara 2000–

- *Fault Tolerant Computing*, *Logical & Functional Programming*, *Linear Algebra*, et. al..

Universidad del Valle de Atemajac 2000-2007

- *Combinatorial and Sequential Logic Circuits*, *Analogic/Digital Control*, *Automation*, et. al..
- Two thesis as advisor.

Publications

- J. F. Sánchez-Blanco, A. Ramírez-Treviño, y A. Santoyo, **"Multiple Specification Regulation in Interpreted Petri Nets"**, IEEE International Conference on SMC 2004, La Hague, Netherlands, October 2004.
- J. F. Sánchez-Blanco, A. Ramírez-Treviño, y A. Santoyo, **"Regulation Control in Interpreted Petri Nets Using Trace Equivalence"**, IEEE International Conference on SMC 2004, La Hague, Netherlands, October 2004.
- J. F. Sánchez-Blanco, A. Ramírez-Treviño, and L. E. López-Mellado, **"Building Supervisory Controllers from Global Specifications Using Labelled Petri Nets"**, International Symposium on Robotics and Automation 2002, Toluca, Edo. Mex., México, September 2002.
- Other 7 mexican conference papers.