Samuel Ayodiran

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Education

University Of Illinois Urbana-Champaign

Bachelor of Science in Computer Engineering — *August 2021 – May 2025*

- Current Coursework: Applied Parallel Programming and Advanced Computer Architecture
- Relevant Coursework: Computer Organization and Design, Computer Systems Engineering, Data Structures and Algorithms, Intro to Algorithms & Models of Computation, Digital Systems Laboratory, Emerging Memory and Storage Systems, Sensors and Instrumentation, and Communication Networks

Experience

Software Engineering Intern — June 2024 – August 2024

Sumitomo Mitsui Banking Corporation — *New York City, NY*

- Developed an ATM app using Java and JPA with a Derby database, implemented core banking functions, and managed data transactions with a RESTful API.
- Enhancing the development portal on the Azure API management platform.

Undergraduate Course Assistant for Digital Systems Laboratory — January 2024 – Present

University of Illinois Urbana-Champaign — *Champaign, IL*

- Hosting office hours to aid students in designing and verification for FPGA digital design course.

Projects

RISCV-32M Out-of-Order Processor | *SystemVerilog, Synopsys VCS, RVFI, Git* — March 2024 – May 2024

- Collaborated in a 3-person team to develop an Out-of-Order processor compliant with the RISCV-32M spec using Explicit Register Renaming.
- Implemented a dynamic branch predictor that utilized a branch target buffer, 2-bit saturating counters, GShare/GSelect, and RAS.
- Designed and integrated a pipelined L1-cache with next-line prefetching, and a variation of a Dadda multiplier.
- Validated processor compliance by integrating RVFI, running benchmarks such as CoreMark, and then comparing commit logs against Spike, a RISC-V Simulator.

Valgrinders OS | *C, x86, Git, GitLab, Qemu, GDB* — October 2023 – December 2023

- Worked with a group of 3 other students to create a simple Linux like Operating System.
- Implemented round-robin scheduling, multiple terminals, a read-only file system, Keyboard driver, RTC driver, and PIT driver.
- Setup the interrupt descriptor table (IDT), basic paging support for tasks, separate 4 MB pages for the kernel and applications.
- Wrote a system call interface with 10 system calls to communicate with user-space programs.

RISC Architcture on FPGA | *SystemVerilog, Git* — February 2023 – March 2023

- Implemented and verified a 16-bit RISC ISA (LC-3) using SystemVerilog on an Intel MAX 10 FPGA.
- Successfully tested functionality of QuickSort program that sorted inputted values from the MAX10 switches and output the correctly sorted values using on-board HEX displays
- Verified accurate behavior through test benches and ModelSIM.

Involvement

Member — August 2022 – Present

National Society of Black Engineers — *Champaign, IL*

Technical Skills

Languages: C/C++, SystemVerilog, SQL(MySQL), x86, JavaScript, Python
Developer Tools: Git, GitLab, GitHub, Docker, Google Cloud Platform, Quartus