Rudakiya Mayank

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- Objective:
  - As a semiconductor professional with over 3 years of hands-on experience on RTL Design of various protocol. Skilled in using industry-standard tools to deliver high-quality solutions. Seeking to contribute my technical expertise and problem-solving abilities to a dynamic team while further developing my skills in RTL design.
- 3 Years Work Experience:
  - 3 years of experience as RTL Design Engineer using Verilog and System Verilog.
  - Experience of working on RTL Design from scratch and modify to add new feature.
  - Protocol Knowledge: TL-UL, TL-UH, I2C, UART, AXI, AXI Stream, UCIe FDI bus
  - Tools: JasperGold, Xcelium, VCS, Verdi, VC Formal, vManager
  - HDL Programming Language: Verilog, System Verilog, Chisel
  - Verification & Methodologies: System Verilog Assertion (SVA), Formal Verification, UVM, and key domain-crossing techniques (CDC, RDC, Lint).
  - Programming Language: Python, C++, Tcl
  - Processor Knowledge: Ibex
- Responsibilities included:
  - Read the specification and understand the design requirements.
  - Extract features from the specification that need to be implemented.
  - Draw the FSM diagram.
  - Write directed tests and static assertions to check the design.
  - Mentor new team members to help them get up to speed with the ongoing project.
  - Collaborate with the verification team.
  - Have good communication skills and be accustomed to working with multi-disciplinary teams.

- Experience Details:
  - Associate Engineer at Cisma Consultants (Verikwest Inc) | March 2022 – Present
- **Project Details**

Project 1	RTL Design of TL-UH from TL-UL Protocol in OpenTitan SOC
Location	Bangalore
Responsibility	• OpenTitan is an open-source SoC (System on Chip). • Read and understood the specifications of the TL-UL and TL-UH protocols.TL-UL is a protocol used in the OpenTitan SoC. • We aimed to integrate a Machine Learning Accelerator IP into the SoC, so we extended the TL-UL protocol by adding the TL-UH feature. Used FSM to write the RTL code. • Observed the Ibex processor of the OpenTitan SoC.
Company	Cisma Consultants

Project 2	RTL Design of AXI Protocol for UCIe Protocol layer
Location	Bangalore
Responsibility	• Read and understood the specifications of the AXI and UCIe protocol layers. • Designed the AXI Master and AXI Slave from scratch to enable communication with the UCIe protocol layer. • Acted as the lead contributor in the project and managed a team of 5 colleagues. • Successfully converted AXI transactions to UCIe flits and vice versa, converting UCIe flits back into AXI transactions. • In the first version, we implemented up to the UCIe FDI bus only.
Company	Cisma Consultants

Project 3	RTL Design of I2C Protocol
Location	Bangalore
Responsibility	• First Project at Cisma Consultants. • Read and understood Specification of the I2C protocol. • Written RTL Code of I2C protocol. • Written Directed Test cases.
Company	Cisma Consultants

Project 4	RTL Design of Cache Controller
Location	Bangalore
Responsibility	• Read and understood Specification of the Cache Requirement. • Used Set Associative Way to Implement Cache. • Implemented Look through cache and Write Back method to Design cache.
Company	Cisma Consultants

Project 5	RTL Design of Arbiter
Location	Bangalore
Responsibility	• Implemented a priority-based arbiter in Verilog code. • Learned to use Jasper tools such as FPV and Superlint to check lint errors, and Jasper CDC to detect metastability during CDC and RDC. • Implemented an asynchronous FIFO with separate clocks for writing and reading. • Used Gray code and a synchronizer to minimize metastability.
Company	Cadence (Client Project, On site)

Project 6	RTL Design using Chisel
Location	Bangalore
Responsibility	• Added a new feature to the internal IP of the SiFive Processor. • Implemented a Round Robin Arbiter into Chisel Code. • Used the AXI Stream protocol to exchange data with arbiter.
Company	SiFive (Client Project, On site)

- Education:
  - **Bachelor of Engineering in Electronics**
    Faculty of Technology and Engineering,
    The Maharaja Sayajirao University of Baroda, Gujarat. (2017-2021) CGPA = 7.99/10
  - **Advance VLSI Design & Verification Training**
    Maven Silicon October 2021 to February 2022