Summary:

Harshith Reddy Surakanti is a Hardware Design Engineer with over three years of experience in RTL to GDSII, FPGA/ASIC development, and workflow automation. He has hands-on experience in accelerator design for edge inference and image processing using FPGAs and SoCs. He also has expertise in RTL and physical design, including processor tapeouts (RISC-V & MIPS) and IP development. He is familiar with the evolving RISC-V ecosystem and reconfigurable computing paradigms.

Name: Harshith Reddy Surakanti

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Phone: +1 (317) 332-9086

Location: Dublin, CA

Country: USA

Position Category: Design: Logic design, Design: Physical Design

Desired Job Role: Hardware Design Engineer

University: Purdue University Indianapolis

Degree: MS in Electrical and Computer Engineering (VLSI)

Graduation Year: 2024

Years Experience: 3

Notable Companies: Integrated Test Range, DRDO, NTT Data GDS

Top Skills: Verilog, SystemVerilog, Lint, VHDL, Linux, CUDA, TCL, Git, MATLAB, Python, C, SQL, Python, TCL, Bash(Ubuntu), PowerShell, JavaScript, Cadence tools Xcelium, Genus, Innovus, Modus DFT, Virtuoso, OpenLane, Altium PCB Design, Xilinx ISE, Modelsim, Simulink, SILVACO TCAD, I2C, SPI, AXI4, UART, USB, Ethernet

Job Intention: full-time

Visa Status: --

Able: no

Subject: Job Application at AheadComputing

Date Sent: 04-19-2025

Resume: Yes