Summary:

VLSI AMS engineer with experience in Design, Verification and Silicon Validation of Serdes, DDRphy and high speed blocks. Hands on expertise in Analog and Physical design flows from concept to GDSII. Has worked with cross-functional teams worldwide in several countries and locations.

Name: Eliseo Torres Casales

Email: ecasales@gmail.com

Phone: +52 3310553261

Location: Zapopan, Jal. Mexico

Country: Mexico

Position Category: Design: Physical Design

Desired Job Role: Senior Physical Design Engineer - CPU PPA Optimization

University: Instituto Nacional de Astrofisica, Optica y Electronica, Instituto Politecnico Nacional

Degree: Master of Science with specialty in Electronics Integrated Circuits Design, Electronics and Communications Engineer

Graduation Year: 2005

Years Experience: 20

Notable Companies: Intel, Wipro Technologies, Freescale Semiconductor, NXP

Top Skills: VLSI AMS Engineering, Design, Verification, Silicon Validation, Analog and Physical Design, Technical Supervision, Schedule and Execution Management, Change Control Board Analysis, Physical Verifications, GDSII Tape-out

Job Intention: full-time

Visa Status: --

Able: yes

Subject: Working at AheadComputing

Date Sent: 03-19-2025

Resume: Yes