VARSHINI NARAYANA

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EDUCATION

Syracuse University | Master's In Computer Engineering | *GPA – 3.81* **August 2022 - May 2024**

Coursework: Advanced Computer Architecture, System Verification and Testing, System on Chip Design, Discrete and Integrated Circuits, Digital Electronic Circuits, Special Problems in Computer Engineering (Machine Learning), Advanced Data Structures in C++, Power Electronics.

PROFESSIONAL EXPERIENCE

Syracuse University **May 2024 - Present**

Research Assistant at ECS Lab *Syracuse, NY, USA*

- Worked with cross-functional teams in designing a 16-node bidirectional Network-on-Chip router, optimizing routing logic, virtual channel allocation, and flow control mechanisms to enhance multi-core data communication.
- This design uses a NOC ring made up of 16 bidirectional routers, each connected to a 4-stage pipelined CPU featuring a custom 23 instruction ISA, including special instructions like Branch Equal to Zero, Branch Not Equal to Zero, and Rotate by Half. Integrated a Network Interface Component to efficiently connect each processor to its corresponding router for seamless multi-core communication.
- Optimized load/store operations by reducing memory access latency through data forwarding techniques, minimizing stalls, and improving instruction throughput. Implemented two forwarding units: one from Writeback to Execution Stage and another from Writeback to Instruction Decode Stage, significantly enhancing pipeline efficiency and reducing instruction delays in high-throughput NoC architectures.

Arcom Digital **May 2023 - August 2023**

Hardware Engineer Co-op *Syracuse, NY, USA*

- Designed and executed JTAG debugging protocols for FPGA-based systems, ensuring pin-level accuracy and functional verification using automated Python test scripts for fault detection, real-time debugging.
- Troubleshot and resolved PCB-level issues debugging Wi-Fi transceiver modules, Analog-to-Digital converters (ADC), FPGAs, Microprocessors, GPS modules, RAM, and ROM components, enhancing system performance, data throughput, and overall functionality.
- Conducted comprehensive validation assessments on new hardware designs using VNA, Power Analyzers, electronic load, Spectrum Analyzers, and Oscilloscopes, Signal Generators.
- Performed Physical & Environmental, EMC/EMI/RF compliance tests on 20+ signal leakage detection devices within a span of four months, ensuring 99% reliability in accordance with Cable Telecommunications industry regulations and FCC compliance standards.

PROJECT EXPERIENCE

Design of High-Performance Convolutional Neural Network Hardware Accelerator **May 2024 – August 2024**

- Designed a hardware-optimized CNN accelerator using Verilog RTL, integrating a pipelined architecture to achieve a 10% reduction in area utilization while improving energy efficiency for real-time data processing in embedded AI applications.
- Implemented a parallel multiply-accumulate (MAC) structure to reduce computation latency by 15%, ensuring fast and scalable processing.
- Developed a finite state machine for control logic, reducing memory bottlenecks, a key consideration in real-time hardware solutions.

Asynchronous FIFO Design & Process Optimization for High-Speed Data Transfer Using C++ **May 2023 – August 2023**

- Designed a parameterized asynchronous FIFO with configurable depth and width, integrating gray-code pointers for reliable clock domain crossing and implementing handshaking mechanisms to ensure metastability-free data transfer between independent clock domains.
- Constructed and executed over 100 test scenarios in UVM to validate FIFO behavior under extreme conditions, including full, empty, and various corner cases. Created randomized test sequences to stress-test FIFO depth, latency, and throughput performance.
- Accomplished 90% functional coverage for timing accuracy, and boundary conditions using coverage groups and cross coverage analysis. Validated reset behavior, write-read synchronization, and handling of read-write operations in multi-clock high-speed hardware systems.

Cache Design & Memory Hierarchy Optimization for Large-Scale Data Processing **January 2023 – May 2023**

- Devised a trace-driven flexible cache and memory hierarchy simulator for L1, L2, and Victim Cache using C++ in a Linux-based environment using Least Recently Used (LRU) and Write Back Write Allocate (WBWA) replacement policy.
- Performed quantitative analysis for different cache sizes, associativity, and block sizes, analyzed the design trade-offs like miss rate, average access time, memory traffic, and area, evaluating associativity, block sizes, and replacement policies, ensuring optimized memory.

Verification of Low Power RISC V 32-bit Microprocessor **August 2022 – December 2022**

- Verified a low-power 32-bit processor, improving processing speed by 30% and reducing power consumption by 20%. Enhanced test coverage of ALU, memory controllers, and branch prediction units using UVM-based constrained-random stimulus generation.
- Performed UVM-based low-power verification using Unified Power Format (UPF) to validate power gating, voltage scaling, and multi-domain power management techniques, identifying critical power optimization opportunities for large-scale automation systems.
- Performed formal verification using property checking techniques with System Verilog Assertions (SVA) and model checking tools like JasperGold to validate ALU operations, and branch prediction accuracy, ensuring corner-case robustness and eliminating functional ambiguities.

DDR3 Memory Controller for Micron DDR3 RAM **January 2022 – May 2022**

- Assembled a Verilog-based DDR3 memory controller, verified in Xilinx, achieving a maximum operating frequency of 333MHz, and achieved static timing analysis timing closure without relying on external Synopsys Design Constraints files.
- Focused on implementing and optimizing core read/write operations to enhance performance and data throughput. Verified using UVM-based testbenches to ensure correct functionality, including boundary checks and corner case handling.

Design & Verification 16nm FinFET Low-Power SRAM **January 2021 – July 2022**

- Designed a 6 Transistor SRAM bit-cell, optimized for low power and high-density implementation in a 16nm Fin-FET technology node.
- Integrated word line drivers, bit line pre-charge circuits, sense amplifiers, and write drivers to ensure reliable read and write operations.
- Utilized fin-based transistor sizing techniques to balance read stability (SNM), write margin, and leakage power consumption.
- Designed a high performance CML based D Flip Flop operating at 112 GHz used for SERDES IP.
- Verified the functionality of a high-performance SRAM using mixed-signal verification, Verilog, and SPICE, ensuring accurate operations.

SKILLS

- Programming Languages: Python, C, C++, Verilog, System Verilog, VHDL, SQL, MATLAB.
- Communication Protocols: SPI, I2C, UART.
- Hardware Design & Development: RTL Design, Layout Design, Logic Synthesis, PCB Design & Debugging, High-Speed Digital Design.
- Testing & Verification: JTAG Debugging, UVM, ASIC Development, Functional Verification, Design for Testability, Static Timing Analysis.
- Tools & Technologies: Cadence Virtuoso, Synopsys Design Compiler, Synopsys PrimeTime, Xilinx Vivado, KiCad, Altium Designer, Linux, git.