Adwyck Gupta

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EDUCATION

Columbia University — New York, NY
M.S. in Electrical Engineering | Tesla Scholar 2024 — Expected Dec 2025
Courses Fall'24: Formal Verification, Computer Architecture, Digital VLSI, SoC Platforms
Courses Spring'25 (In Progress): Embedded Systems, Embedded Scalable Platforms, Embedded AI

Vellore Institute of Technology — Vellore, IN
B.E. in Electrical and Electronics Engineering | GPA: 3.98/4.0 — May 2024
Courses: VLSI Design, Digital Design with FPGAs, Object-oriented Programming, Analog and Digital Circuits

SKILLS

Core: Verilog/ SystemVerilog, SVA, VHDL, Perl, Python, C/C++, System C, tcl, MATLAB, R
Software: Cadence JasperGold, Cadence Virtuoso, Quartus-Prime, Vivado, Catapult HLS, Cadence PSpice, Eagle
Hardware: Arria10 SoC dev-kit, STM32, Raspberry Pi, TI LaunchPad, ESP32/8266

PROJECTS

Formal Verification of FPGA-Based Game Graphics and Sprite Controller — Sep 2024 - Dec 2024
- Verified VGA controller module using JasperGold, ensuring sprite logic, priority encoding, and RAM consistency
- Developed SystemVerilog assertions for tile mapping, sprite prioritization, and display output verification
- Optimized verification by crafting assumptions, using abstraction and improving proof convergence

Digital VLSI design: Accumulator-based Microcontroller Core (TSMC 65nm) — Sep 2024 - Dec 2024
- Designed a 8-bit microprocessor core, including an SRAM block using TSMC 65nm technology
- Integrated the core with the bus driver, memory, arithmetic, and control unit and devised PLA to test the logic
- Developed a DRC/LVS clean layout using Cadence Virtuoso

SoC Platforms: Design and Optimization of FPGA-Based CNN Layer Accelerator — Sep 2024 - Dec 2024
- Architected HLS design for CNN accelerator, optimizing area, latency, and accuracy for scalable AI/ML workloads
- Integrating accelerators designed in SystemC into SoC with customized memory and precision strategies
- Achieved Pareto-optimal design with 100% accuracy, 93% latency reduction, and 2.1% FPGA resource usage

Configurable Power Management for SoCs with Temporary Sprinting — Jan 2025 - Ongoing
- Implementing a coin-token algorithm based decentralized PMS with temporary sprinting for heterogeneous SoCs
- Designing load accelerator in Verilog, and firmware to validate sprinting-aware DVFS via token exchange

WORK EXPERIENCE

Bhabha Atomic Research Centre — Mumbai, IN
System-on-Chip Design Intern — Jan 2024 - Jun 2024
- Designed high-speed digitization and data acquisition SoC-FPGA, with 1Gbps throughput from PCIe ethernet
- Performed Static timing analysis of the synthesized RTL design in Intel Quartus Prime pro
- Worked with AMBA AXI, Avalon protocols, and JESD204b interfaces, ensuring scalability and compatibility
- Integrated Verilog modules and IP blocks in Arria-10 SoC to initiate data transfer from external FIFOs to OCM

Maven Silicon Softech Ltd — Bangalore, IN
VLSI Trainee — May 2023 - Jul 2023
- Modeled RTL based SPI master core, Wishbone master, and SPI slave modules
- Configured SPI Design protocol in Verilog and verified using MODEL SIM
- Coded testbench for verification of sub-modules and top-modules under various RX/TX conditions

Computational Intelligence Laboratory, IISc — Bangalore, IN
Research Intern — May 2023 - Jul 2023
- Spearheaded development of a compact distributed IMU sensor for state estimation in GPS-denied UAVs
- Designed a custom circuit schematic and PCB layout, ensuring signal integrity and functionality