SIDDHARTH MOHAN

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Citizenship India

Education

MS (Masters) in ECE	2021-2023	University of California, San Diego, USA
B. E. (Hons.) Electrical & Electronics	2007-2011	BITS Pilani, Pilani Campus, India

I am an Electrical Engineer with a Masters (MS) from University of California, San Diego (UCSD) in Electronics Circuits & Systems with 11+ years of industry experience ranging from PCB to Chip level design, analysis, testing and productization. I am a non-US citizen who is legally authorized to work in the USA.

Organisation Name	Project Work
Qorvo, Sr. Electrical, Engineer (Present)	➢ Design, Verification and Validation of Analog & RF blocks for cellular products using industry standard chip-package design & characterization tools. ➢ Supporting Hardware test- both manual and ATE based for chip & board bring-up.
Intel, Failure Analysis Engineer (14 Aug'23 – 29 Dec'23)	➢ Responsible for identifying and researching silicon failures to improve product yield, quality and/or reliability. ➢ To assist product engineers with defect observation and yield improvement in high-volume production. ➢ Familiar with Lab tooling operations such as SEM/TEM, testers etc ➢ Writing FA plans for XTEM/PTEM/IREM to isolate the possible defect location on the die
UCSD, MS Student ECE	➢ Pursued ECE Courses for MS program from Sep 2021 – July 2023
Globalfoundries India, MTS Design Methodology (Level 7) (27 July 2020 – 20th Aug 2021)	➢ IC-Package Co-design & Co-simulation Enablement for mmWave application using **Cadence VRF & EMX**, Ansys **HFSS**, , **Keysight ADS** tool flows. ➢ Creating **Antenna In Package** (AIP) demonstrator vehicle using 28Ghz patch antenna and FC-CSP package for enabling the GF 45RFSOI Assembly design Kit (ADK) for IC-Package co-design within Virtuoso (VRF) cockpit. ➢ Imparted the VRF & ADK training on the demo designs for IC and Package designers and deployed the environment. ➢ Bandgap Reference integrated circuit design and simulation in GF 45RFSOI.
Cadence Design System India, Lead Product Engineer, System Analysis group (2nd July 2018- 15th Apr 2020)	➢ Product Engineering for Reliability EDA module and it's integration inside Cadence PCB design tool System Capture. ➢ Customer demo and presentations on Cadence EDA products. ➢ PCB Schematic design, **familiar with board bring-up and testing.** ➢ PCB Signal Integrity & Thermal analysis. ➢ Worked with Standards including MIL-217, IEC62308, IEC61508, ISO26262 for Functional Safety (FuSa), MTBF predictions & FMEDA ➢ Cadence Tools used : **Sigirty**, **Virtuoso, Spectre**, **Orcad**, **Pspice**, **Windchill (PTC)**
Keysight Technologies India R&D Engineer Advanced, Spice Modeling & Simulation(4th Apr 2016- 29th June 2018)	➢ Designing & Automating **SPICE simulation models** for various semiconductor components like transistors, Regulators, **CMOS** Opamps, diodes) ➢ **Run spice simulations over board** to check for power up & transient issues. ➢ Thermal modeling & stress /Reliability (MTBF). ➢ Tools used : LTSpice, Hspice, Mentor Expedition, **ADS**, **IC-CAP** ➢ *Hardware EMI/EMC, life-cycle, thermal testing* ➢ Python based Automation of existing operations
Tata Steel Ltd. India, Manager – Electronics in Automation department (15th May 2012- 31st March 2016)	Project involves Design, Development & Testing of circuit for plant automation. ➢ Designed SMD circuit for the previous non-SMD versions ➢ PLC , Drive , Instrumentation & Control plant commissioning. ➢ Direct Interaction with customers for all design & quality issues. ➢ Production Line management, Sampling, Failure Analysis. ➢ Micro controller MSP430 & AT89S52(C programming) for sensor interfacing

Development Engineer , Embedded Systems , Kritikal Solutions Pvt. Ltd. India IIT Delhi Incubated Startup (6th June 2011- 2nd May 2012)	➢ Worked on FPGA design EDA tools(Xilinx-ISE, Lattice_Diamond, Altera-Quartus). ➢ Developed a LINUX based automated build environment [using shell scripting] for generating netlist for different communication protocols. This involved studying the FPGA EDA tool design flow, understanding the various commands for carrying out synthesis/translation etc..

Internships	Learning/ Experience as an Intern
Qorvo USA Design Engineer, Intern (3 months) , Summer 2022	➢ Improving second harmonic improvement of ASW (antenna switch) for cellular handsets by employing various possible techniques verified through ADS-Cadence dynamic simulations. ➢ Improving time taken in RF simulations having multiple states and corners for performance verification for example LNAs with multiple gain states across temperature and process.
World Mobile Group, Spring 2023 (3 months)	➢ To design, build and test a mobile multi-band broadband wireless antenna for the WMG international network. The antenna being designed and fabricated at UC San Diego will be deployed on tethered airships.
ST Microelectronics India Analog Design Intern , 2010 (6 months)	➢ Work involved Design & optimizing LDO Voltage regulator circuit at the transistor level using 180nm TSMC PDK using Cadence tool set.

Publication & Patent

- US Patent (19PA073US01) on “Systems and Methods for Computing Electrical over-stress of devices, associated with Electronic Design.”
- Authored a paper on – “Electrical Overstress Estimation for Printed Circuit Board design.” which was presented at 2020 IEEE RAMS conference.
- Authored a paper on – “Retroreflection with Amplification for Long Range mmWave Sensing” which was presented at 2023 ACM mmNets conference.
- Authored a paper on – “Unique Airborne Wireless Communication System for Connecting the Unconnected” which was presented at 2024 IEEE International Symposium on Phased Array Systems & Technology.

Awards & Honors

- Excellent Collaboration Material for Reliability Analysis at Cadence Design Systems in 2018.
- Appreciation Award at Globalfoundries in 2021 for exceptional performance in ADK project.
- An Appreciation award at Cadence for giving Training sessions to R&D team from Bangalore & Noida