Summary:

Pre silicon verification engineer with 3 years of experience in diverse ASIC verification areas.

Name: Juan Luis Magaa Paz

Email: Opomola@gmail.com

Phone: +52 312 210 1393

Location: Zapopan, Jalisco, Mexico

Country: Mexico

Position Category: Verification: Design verification

Desired Job Role: CPU Verification Engineer

University: TECNM CAMPUS COLIMA, ITESO

Degree: MECHATRONICS ENGINEER, PRE SILICON VERIFICATION DIPLOMA

Graduation Year: 2021

Years Experience: 3

Notable Companies: INTEL, NXP

Top Skills: C, C++, Python, Perl, Bash scripting, GNU Makefile, UVM, System Verilog, System C, Synopsys, VCS, Verdi, Cadence, Vmanager, Quartus, Eclipse DVT, Git, Linux, Windows

Job Intention: full-time

Visa Status: --

Able: yes

Subject: CPU verification engineer job open

Date Sent: 02-20-2025

Resume: Yes