Roman Kapur

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Education

Carnegie Mellon University — Pittsburgh, PA
Masters of Science in Electrical & Computer Engineering — December 2025

Carnegie Mellon University — Pittsburgh, PA
Bachelor of Science in Electrical & Computer Engineering — May 2025
Coursework: Computer Architecture, RTL Design & Verification, Analog Design & Layout, FPGA & ASIC Design, Computer Systems

Skills Summary

- **Programming/HDL Languages**: SystemVerilog, C, Python, Rust, Perl, TCL, C++, Java
- **Tools/Skills**:Cadence Innovus, Genus Synthesis, Linux, Git, RTL, Cadence EDA, Synopsys Yield Explorer, Scripting, MATLAB, EDA, Excel

Work Experience

Advanced Micro Devices — Austin, TX
Hardware Engineering Intern — June 2024 - August 2024

- Analyzed TSMC and AMD Automated Test Equipment test and bin data using Synopsys Yield Explorer to correlate failure causes with fabrication steps enabling greater granularity and adaptation in manufacturing processes resulting in increased yield
- Leveraged Snowflake databases and Python to create adaptive web-app in JS to make Yield Explorer data more accessible

Carnegie Mellon University — Pittsburgh, PA
Lead Teaching Assistant for 18-220: Electronic Devices and Analog Circuits — August 2023 - Present

- Proctored weekly lab sessions which provide students the chance to apply their knowledge from class to real projects. Demonstrated how to use and debug issues with oscilloscopes, bench-top power supply, waveform generators, and multimeters.

Sandia National Laboratories — Albuquerque, NM
Systems Research & Design Intern — May 2023 - October 2023

- Developed a C communication protocol for nuclear weapons flight data that resolved potential confidentiality risks and increased efficiency of analyzing flight data wave forms by 33% through concurrent packet processing in C++ and MATLAB.

Relevant Project Experience

Analog Mixed Signal PLL Design — Pittsburgh, PA
18-725: Advanced Digital Integrated Circuit Design — January 2025 - Present

- Designed a Delta Sigma Fractional-N AMSPLL and fully synthesizable digital PLL on the same die for comparison in TSMC 28nm.
- Tuned PLLs for 1 GHz - 2GHz operation range from board level reference clock of 20MHz through Cadence Virtuoso AMS Simulator
- To be fabricated May 2025

256x16b Single-Port SRAM — Pittsburgh, PA
18-622 Digital Integrated Circuit Design — August 2024 - December 2024

- Designed and implemented an SRAM cell with an access time of $\leq$30 FO4 inverter delays and achieved a total area of $\leq$20M^2 with $\geq$50% cell area efficiency, integrating a compact decoder, I/O, and control circuitry.
- Conducted post-layout simulations using Spectre and Spectre FX for critical path analysis and specification validation.

Pixel Sensor Interface Tapeout — Pittsburgh, PA
18-620 Design, Integration, and Tapeout of IoT Systems — August 2024 - December 2024

- Developed time-to-digital (TDC) analog to digital converter (ADC) on TSMC 65nm technology
- Designed and laid out Current Steering DAC, Operational Amplifier, and Pulse Counter (using Innovus Foundation Flow)
- Completed chipfloor plan, I/O pinout, and biasing network for final GDSII file

USB 2.0 Protocol — Pittsburgh, PA
18-341 Logic Design & Verification — November 2023 - December 2023

- Designed and implemented a USB 2.0 host controller in SystemVerilog.
- Developed a layered system of synthesizable state machines across physical, data link, and transaction layers to encode, decode, and process data packets.

Network on Chip — Pittsburgh, PA
18-341 Logic Design & Verification — October 2023 - November 2023

- Implemented store and forward switching communication network system in SystemVerilog, created Nodes and Routers featuring multi-packet processing and fairness.

Out of Order Processor Simulator — Pittsburgh, PA
15-346 Computer Architecture — August 2023 - December 2023

- Developed a customizable FOCO processor simulator in C, enabling detailed configuration and performance analysis.
- Features dynamic tuning of cache attributes, branch predictors, number of processors, processor specifications, interconnect types, and coherency protocols. Supports highly customized and comprehensive bench marking with splash2.