Vishal S Rao

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EDUCATION:

M.S. | Electrical Engineering | University of Minnesota, Twin Cities **(Aug 2014 - May 2016)**

SKILLS:

Programming Languages: Verilog, PERL, C++, System Verilog
EDA tools: Synopsys VCS/DC, Power Artist, Lint, Multi2sim

WORK EXPERIENCE:

Staff Design Engineer | Condor Computing | San Jose, California **(Nov 2023 – Present)**

- Duties involve:
  - Micro-architecture design lead of memory management unit compliant with RISC-V spec
  - RTL implementation, documentation and standalone as well as higher level verification and debug
- To communicate efficiently with the Architects, RTL design teams, verification engineers, and management as the product advances from implementation through tape-out

IP Logic Design Engineer | Intel Corporation | Santa Clara, California **(May 2020 – Nov 2023)**

- Duties involve:
  - micro-architecture design of on-chip interconnects, cache coherency controller and AXI protocol NOC IP
  - RTL implementation, documentation and standalone as well as higher level verification and debug
- To communicate efficiently with the Architects, RTL design teams, verification engineers, and management as the product advances from implementation through tape-out for the multiple ASICs

Silicon Design Engineer | Advanced Micro Devices | Boxboro, Massachusetts **(Aug 2016 – May 2020)**

- Duties involve:
  - micro-architecture design and documentation of texture block in graphics pipeline
  - RTL implementation, standalone as well as higher level verification and debug
- To communicate efficiently with the Architects, RTL design teams, software driver teams, physical design teams, verification engineers, and management as the product advances from implementation through tape-out for the multiple ASICs we typically have in-flight
- Assist with the block power management by implementing low power design methodologies through assistance of EDA tools (Power Artist and PTPX)

CPU Performance Intern | Intel Corporation | Austin, Texas **(June 2015 – Dec 2015)**

- Worked on bring-up of performance monitoring infrastructure; validation of events and developing a post processing tool to facilitate comparative analysis of monitors' health after each regression
- Performed analysis of c-model regression with pre-silicon RTL
- Infrastructure setup of the pipeline tracing tool and debug of simulator bugs/failures

ACADEMIC PROJECTS:

Managing Last Level Cache in a Heterogeneous Multiprocessor Environment in Multi2sim

- Modified multi2sim to implement heterogeneous mem-system shared cache and integrate HeLM replacement Policy; compared results against standard LRU and DRRIP policies

RTL implementation of FFT processor for MIMO-OFDM Baseband transceiver

- Realization of RTL design flow including Verilog based design, Simulation, Synthesis and Verification of an 8-point DIF-FFT processor for a MIMO-OFDM baseband transceiver