Hello AheadComputing,

I am Saugat Sharma, a Post bachelor PhD candidate in computer engineering. I will be graduatingthis semester and have been looking around for an RTL design and verification role.

I have extensive experience in writing RTL design (CPU, Outof order processor) using system verilog. Currently I work as an FPGA design engineer designing RTL IP for DNN activation function and custom convolutional layers. I have experience in UVM for design verification. I was wondering if there is an opportunity at ahead computing and If I can be a fit for it. I have attached my resume for your reference. I hope to hear from you soon.

Thank you!

Regards,

Saugat Sharma