CARLOS RODRIGO FERNANDEZ GARCIA

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SUMMARY

Pre-Si verification engineer with 7+ years of experience on diverse ASIC verification areas.

PROFESSIONAL EXPERIENCE

NXP Semiconductors / Guadalajara, México (November 2024 – Present)

- ***Senior Digital Verification Engineer –*** Testbench development, test planning and feature ownership of mixed signal technologies for automotive applications, focused on power management.

Intel Corporation / Guadalajara, México (June 2017 – October 2024)

- ***CPU Design Verification Engineer -*** Testbench development and feature validation focused on Power Management for a processor based in x86 architecture.
  - Ownership of verification test plan for the following areas:
    - Core disable state and its related events.
    - Dynamic Voltage and Frequency Scaling.
    - Error handling and survivability.
    - Dynamic clock gating.
  - Focus on implementing SVA checks and created control blocks for dynamic SVA enablement segmented by power domains.
  - Ownership of data integrity efforts for processor's control registers.
    - Implemented UVM scoreboard and simulation checks to ensure boot flow reflects the proper configuration values.
    - Led efforts to ensure data coherency and access policy is maintained based on register attributes and endpoint data paths based on the processor's functional states.
  - Implemented reusable UVM, C++ and Python testbenches for emulation consumption and post-simulation processing.
- ***Pre-Si Verification Engineer -*** Ownership, integration and validation of compression/decompression codec IPs.
  - Implementation of testbench and integration of third-party VIPs.
  - Ownership of decompression test plan for the following areas:
    - Power management.
    - Reset.
    - Clock gating.
    - Error handling and survivability.
  - Led triage and error categorizing efforts for decompression team.
  - Ownership of memory BFM dedicated to initialization flow for simulation optimization.
  - Engaged in active communication with vendor and transnational collaborators, requesting fixes or adjusting validation efforts based on the received feedback.
- ***Pre-Si Verification Engineer -*** Feature validation and integration of a PCIE 4.0 VIP.
  - Contributed with debug efforts to identify data corruption.
  - Focus on Physical and Data Link layers.

EDUCATION

Master's Degree in Electronic Design at Instituto Tecnológico y de Estudios Superiores de Occidente (ITESO). (August 2020 - Present).

Bachelor's Degree in Electronic Engineering at Instituto Tecnológico y de Estudios Superiores de Occidente (ITESO). (August 2013 - May 2018).