KUSHAL MANJUNATH

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EDUCATION

Master of Science in Electrical Engineering **May 2025**
George Washington University, Washington, DC 3.5 GPA
Relevant Courses: VLSI design, High-level RTL design, Computer Architecture, Advanced Microarchitecture, HPC

TECHNICAL SKILLS

VLSI Design : Full custom design, Physical design, Analog/Mixed-Signal Integration, CAD for VLSI, ASIC/FPGA design flow, RTL, Clock-domain crossing, FSM, Low-power, DSP, STA, CTS, Logic design, Analog circuit design
Programming Languages : C/Embedded C, C++, Python, Shell scripting, Assembly, CUDA, UPC
EDA Tools : OrCAD, Cadence Suite (Virtuoso, Xcelium, Innovus), MATLAB
HDL : SystemVerilog, Verilog
Embedded Systems : Real time systems, driver development, IOT, Microcontroller Programming (NXP S32G, NRF52, Raspberry Pi, Beagle bone Black), Embedded Linux, YOCTO
Automotive : AUTOSAR (Classic and Adaptive), QNX RTOS
Advanced Computing : Neural Networks, neuromorphic computing, HPC design, Scientific computing
Computer Architecture : ISA (X86, ARM, MIPS, RISC-V), pipeline design, cache and memory design, CPU design, tools (WinMIPS, Dinero, GEM5, ScaleSim, SimpleScalar)

PROFESSIONAL EXPERIENCE

Research Assistant | **Adam Lab, George Washington University, Washington, DC** **Jun 2024 – Aug 2024**
- Leveraged NVIDIA CUDA to accelerate computational tasks, improving simulation speed for large-scale spiking neural networks by 25%.
- Implemented neural activity models using CARLsim, a GPU-accelerated neural network simulator; achieved enhanced data processing speeds that supported the analysis of up to 1 million neuron interactions simultaneously.

Senior Automotive Engineer/Tech Lead | **Luxoft Pvt Ltd, Bengaluru, India** **Nov 2021 – Jul 2023**
- Revamped on-chip resource management for NXP S32G SoC, accomplishing efficient memory controllers and interconnects to boost overall system performance.
- Led a team of three to develop a custom ASIC for automotive infotainment, integrating secure boot, OTA updates, power gating, and clock domain techniques for reliability and security ensuring robust operation in automotive environments.
- Created edge computing applications on Linux-based automotive systems for real-time decision making, decreasing real-time processing latency and execution time to meet strict timing and power constraints.
- Recruited and coached 15 interns and launched a mentorship program for new joiners in the Bengaluru office.

Automotive Engineer | **RealThingks Automotive, Bengaluru, India** **Feb 2020 – Apr 2021**
- Architected, and tested firmware for automotive-grade microcontrollers leveraging embedded C & C++, ensuring enhanced code execution and resource efficiency, cutting down code execution time by 20%.
- Developed hardware interfaces for NVM controllers and GPIO in automotive ASICs, integrating precise timing control and reliability features to meet stringent industry standards.
- Researched and formulated on-chip communication protocols for signal-to-service translation in heterogeneous automotive SoCs; findings enabled cloud-connected architectures, and next-gen automotive ecosystems.

Intern | **RealThingks GmbH, Bengaluru, India** **Aug 2019 – Feb 2020**
- Designed high-power PCBs for smart furniture, optimizing layout and component placement to ensure efficient power distribution and signal integrity, reducing verification time by 80%.
- Devised an on-chip bootloader module for IoT-focused ASICs, leading to the resolution of common initialization failures that affected over 100 devices in field tests.

ACADEMIC PROJECTS

Network on chip design Dec 2024
- Investigated architectural adaptations for Network-on-Chip designs on heterogeneous multi-core systems; findings helped mitigate traffic congestion by 25%.

Machine learning accelerator Dec 2024
- Crafted a novel analog-mixed-signal architecture for efficient machine learning inference, improving energy efficiency by 35%.

Binomial low pass filter Dec 2023
- Designed and simulated a 6-tap binomial low-pass filter(circuit and layout) in Cadence Virtuoso. Built Python scripts to automate testing, cutting verification time by 50%.

Digital communication system Dec 2023
- Developed an RTL-based digital communication system with symbol mapping, up-sampling, and filtering with built-in SPI module and deployed clock-domain-crossing for synchronization, maximizing for timing, area, and power. Synthesized and implemented design in Cadence Innovus and verified the system on an FPGA.