Summary:

Binal Nasit is a seasoned IP Logic Design Engineer with close to 10 years of experience in IP design and micro-architecture. They have worked at Intel Corporation, where they led the development of the Industry first Computer Express Link .Cache .Mem controller IP. They are skilled in languages such as Verilog, Perl, and Python, and have experience with tools such as Spyglass, Synopsys VCS, Verdi, VCLP, VCLint, and Cadence Jasper.

Name: Binal Nasit

Email: binal.c.nasit@gmail.com

Phone: +863-266-1274

Location: Cumming, GA 30040

Country: USA

Position Category: Design: Logic design

Desired Job Role: CPU Micro-architecture and RTL Design Engineer

University: University of Southern California, College of Engineering, Pune

Degree: Master of Science in Electrical Engineering, Bachelor of Technology in Electronics and Telecommunication

Graduation Year: 2015, 2012

Years Experience: 10

Notable Companies: Intel Corporation

Top Skills: Verilog, Perl, Python, Spyglass, Synopsys VCS, Verdi, VCLP, VCLint, Cadence Jasper, Logic design, UPF, Clock domain crossing, Post-Si debug, Low power design

Job Intention: full-time

Visa Status: --

Able: no

Subject: Resume - CPU Micro-architecture and logic design engineer

Date Sent: 04-05-2025

Resume: Yes