Rohit Shriram Joshi

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Education

University of Michigan, Ann Arbor, USA **Expected: Apr 2025**
Masters of Science in Electrical and Computer Engineering **(GPA 4.0/4.0)**
Key courses include: VLSI Design I (ongoing), Microarchitecture (ongoing), Computer Architecture, VLSI for wireless communication and machine learning

University of Mumbai, India **Jun 2023**
Bachelor of Technology in Electronics Engineering **(CGPA 9.52/10)**
Key courses include: Digital Circuit Design, Electronic Devices and Circuits I & II, VLSI Design, Digital Signal Processing, Design of Linear Integrated Circuits

Project Experience

2-way MIPS R-10K Style Out-of-order Single-Core Processor in SystemVerilog **Dec 2024**
- Designed, tested, and synthesized a 2-way superscalar CPU with RISC-V RV32IM ISA, using Synopsis VCS, Verdi and DC.
- Designed and optimized critical backend RTL modules such as Reservation Station (32 entries), Reorder Buffer (32 entries) and Store queue to enable efficient dynamic instruction scheduling.
- Developed comprehensive testbenches for Reservation Station, Reorder Buffer, Store queue and Functional Units.
- Integrated CPU frontend and backend, resolving interface challenges and branch misprediction for seamless pipeline communication.
- Attained average cycles per instruction (CPI) of 3.96 and clock period of 26 ns, meeting all specifications and passing all test programs.

Convolutional Neural Network Accelerator with Sparse Winograd Algorithm **Dec 2024**
- Designed and implemented the BWT (Input Transformation Unit) with integrated ReLU, using shift and add operations to minimize the critical path delays and generate four 6x6 matrices efficiently.
- Developed the SIU (Squeeze and Indexing Unit) to process sparse matrices, removing zeros and generating Multibit Mask (MBM) encodings for optimized sparse data representation.
- Validated module integration via Verilog simulations, ensuring accurate sparse data flow for subsequent pipeline stages.

Pipelined RISC-V Processor Design with Hazard Management **Sep 2024**
- Implemented hazard detection and forwarding logic in a 5-stage pipelined RISC-V processor, optimizing instruction execution efficiency.
- Engineered data forwarding paths to resolve data hazards, optimizing processor performance and reducing stalls during processing.
- Created comprehensive RISC-V assembly unit tests, ensuring correctness and reliability of overall processor functionality.

UART Serial Communication Module Design in Verilog **Apr 2023**
- Developed an UART module in Verilog, handling both transmission and reception of serial data using an FSM approach
- Designed transmission logic to serialize parallel data and reception logic to deserialize incoming data into parallel format.
- Implemented state driven logic for serial data transmission, including start, stop and data bits, with proper handling of bit synchronization.

Digital Circuit Design and Verification using CPLD **Jul 2021**
- Participated in workshop on the Krypton v1.1 CPLD board developed by IIT Bombay.
- Gained hands-on experience programming the CPLD board using UrJTAG Standard and Quartus software.
- Simulated and tested the functionality of digital components, including logic gates, ALU, multiplexers using VHDL.
- Engaged in practical projects involving real world applications such as traffic signal control, digital alarm clocks, electronic voting machines (EVM) which enhanced problem solving skills under tight deadlines.

Work Experience

University of Michigan **Oct 2024 - Present**
Research Assistant | Astronomical Computing at L2 Ann Arbor, USA
- Collaborating on research in Astronomical Computing at L2 under Prof. Nathaniel Bleier as part of his collaboration with NASA.
- Achieved 2000x2000 matrix multiplication on radiation-hardened FPGA in 27 seconds using High Level Synthesis and Vitis.
- Currently exploring further reductions in computation time for large-scale matrix operations on FPGA platforms.

SR Systems **May 2024 – Jul 2024**
Electrical Engineering Intern Mumbai, India
- Developed and optimized control algorithms for automated industrial systems, enhancing system reliability and real time performance.
- Collaborated with cross-functional teams to integrate hardware and software, ensuring seamless operation and minimizing latency.

Meshnet Electronics **Jun 2022 – May 2023**
Electrical Engineering Intern Mumbai, India
- Designed and implemented an isolation circuit for a paint dispersion system using IC 555 timer, comparator and 4N25 optocoupler.
- Validated functionality of 100+ fabricated PCBs through rigorous hardware testing and debugging.

Indian Institute of Technology, Bombay **Jan 2022 - Nov 2022**
Student Intern Mumbai, India
- Engineered an innovative EMG Signal Controlled Wheelchair, translating paraplegic users' EMG signals into precise wheel actuation.
- Developed the EMG signal acquisition and conditioning circuitry which consisted of buffer, amplification, Schmidt Trigger and rectification circuit.
- Integrated ESP32 microcontroller, battery, motor driver, and motors into the wheelchair system while managing space constraints.
- Received a grant of INR 5,50,000/- (USD 6616) under the TIH-IoT CHANAKYA Graduate Internship Program 2021-22.

Technical Skills

- Programming languages: System Verilog, Verilog, VHDL, MATLAB, C, TCL, Python, Assembly Language Programming
- Proficient in: Vivado, Verdi, Cadence Virtuoso, AutoCAD, LTSpice, Quartus, AVR Studio, Easy EDA, Cisco Packet Tracer