Binal Nasit

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CAREER OBJECTIVE

Obtain a challenging RTL design and microarchitecture position in a high-quality and dynamic engineering environment where my resourceful experience and skills will add value to organizational operations.

TECHNICAL SKILL SET

Languages: Verilog, Perl, Python
Tools: Spyglass, Synopsys VCS, Verdi, VCLP, VCLint, Cadence Jasper
Skills: Logic design, UPF, Clock domain crossing, Post-Si debug, Low power design

PROFESSIONAL EXPERIENCE

Intel Corporation **July 2015 - Present**
IP Logic Design Engineer
Design Lead for CXL Cache-Mem Controller IP. Defined microarchitecture and logic implementation of CXL Cache-Mem Controller IP across multiple generations. Worked with Verification team for IP bring up, debug tests and analyze coverage metrics. Closely collaborated with Physical Design team on floorplan decisions and timing closure.

CXL 3.0:
- Worked on architecture definition of new features defined in CXL Spec for the IP.
- Defined and set up new partitions for the IP as cell count grew. Led an effort to reduce inter-partition wire crossings within the IP to help SD team.
- Led 5 design engineers to complete implementation of new RTL features/enhancements.
- Microarchitecture definition and implementation of Error Isolation feature in the IP.

CXL 2.0:
- Microarchitecture definition and logic implementation of encryption and link-subdivision features for the CXL Cache-Mem Controller IP.
- Developed modules for functions used commonly across design. Libraries being used across the IP for several generations.
- Worked closely with Product and System engineers during the bring-up of products, helping resolve various post-silicon issues through software workarounds and ECOs in the IP.
- Led multiple interns to complete short term projects for the IP design team.
- Set up UPF and VCLP for the multi-power domain IP.
- Set up OSXML for next generation of the IP to enable new features.

CXL 1.1:
- Worked on logic implementation of flow control and transaction layer queues for first generation CXL Cache-Mem Controller IP from scratch.
- Extensive experience in fixing timing issues in front-end logic without compromising latency and delivering a state of the art IP.
- Developed automated flow to define registers from Excel spreadsheet to OSXML to replace hand-coded RDL.
- Implemented Performance monitor and corresponding events for the IP.
- Set up usage of Verilog-Auto for IP to simplify and automate module instantiation and port connection across modules.

Die to Die Link Subsystem integration and verification

- Worked on integration of Multiple IPs into Die to Die Link Subsystem.
- Verified Logical to physical link interface at subsystem level testing out inter-IP operability.
- Worked closely with the IP teams to resolve issues and make quick forward progress

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EDUCATION

University of Southern California **May 2015**
Master of Science in Electrical Engineering **GPA: 3.8/4**

College of Engineering, Pune (COEP, affiliated to University of Pune, India) **May 2012**
Bachelor of Technology in Electronics and Telecommunication **GPA: 8.6/10**

PATENTS

System, Method and apparatus for reducing latency of receiver operations during a containment mode of operation - US20230020359

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