PAVAN KIRAN REDDY KOTLA

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EXPERIENCE

AMD, Santa Clara, CA — *CPU Formal Verification Engineer*

December 2023 - January 2025

- Built formal testbenches and test plans from ground up, primarily for the Load Store unit of x86 based CPU cores.
- Developed and deployed SystemVerilog Assertions (SVA) to exhaustively verify functional properties for Load Ordering and Out of Order Buffers, using VC Formal/Jasper to uncover corner case bugs.
- Developed high-level formal models and abstractions for complex CPU logic blocks by simplifying the behavior of surrounding logic, allowing for more targeted and efficient verification.
- Optimized convergence rates in formal property verification (FPV) by integrating targeted cover point checks, effectively resolving inconclusive results across complex design states.
- Partnered with RTL design and microarchitecture teams to analyze and debug counterexamples, refine SVA constraints, and elevate formal verification methodologies.
- Enhanced verification infrastructure and automation processes through Python scripting, streamlining workflows.

Arteris IP, Austin, TX— *Design Verification Intern*

September 2023 - November 2023

- Developed and refined a scalable testbench reference model in SystemVerilog for the Tree-based PLRU Cache Replacement Algorithm, enabling comprehensive verification of various cache configurations.
- Contributed to the verification process by creating module-level testbenches in SystemVerilog, and identifying RTL design bugs.
- Enhanced productivity by assisting in the development of automation scripts using JavaScript to streamline simulation execution and, optimizing the verification workflow and reducing manual effort.

PROJECTS

Design and Verification of AMBA AXI-3 Bus protocol using SystemVerilog — *Jan 2023*

Developed SV based class-based layered testbench with Transaction, Generator, Driver, Monitor, and Scoreboard. Employed constrained random testing, and assertions to verify the custom-built AXI-VIP architecture

SKILLS

Programming: System Verilog, Verilog, SVA, UVM, C, JavaScript, Python(scripting language), TCL.

Tools: VC Formal, Jasper, VCS, Verdi, Mentor Questa, ModelSim, Quartus Prime, MATLAB.

EDUCATION

University of Houston, — *M.S in Computer Engineering*

August 2021 - May 2023

Coursework: Advanced Computer Architecture, Advanced Digital Design and Verification, VLSI design, Advanced Hardware Design.

Osmania University, — *B.Engg in Electronics and Communication Engineering*

August 2016 - May 2020

Coursework: Microprocessors and Microcontrollers, Embedded Systems, Real Time Operating Systems, Object Oriented Programming.

AWARDS

Received full-ride merit scholarship for Bachelor's degree awarded by the Telangana State Government for securing a top 3% rank in the State Engineering Entrance Exam.