Tejashree Kulkarni

984-286-2339 | tkulkar@ncsu.edu| LinkedIn| GitHub| Raleigh, NC

EDUCATION

North Carolina State University | Raleigh, NC **August 2022 - May 2024**
Master of Science, Computer Engineering
Relevant coursework: Advanced Verification with UVM, ASIC & FPGA Design with Verilog, Architecture of Microprocessor
Maharashtra Institute of Technology WPU | Pune, India **July 2018 - May 2022**
Bachelor of Technology, Electronics and Communication Engineering

EXPERIENCE

North Carolina State University | **Research Assistant |** RTL Design, System Verilog, UVM, layered-testbench **July 2024 - Present**

- Spearheaded the development of an end-to-end **RTL design** and **functional verification** solution for convolutional neural network accelerators (FSM/Test Plan/BFM/ Coverage/ Scoreboard)
- Optimized a convolution **MAC operation** by incorporating additional **pipeline stages**, improving design **throughput by 35%** while maintaining area efficiency through synthesis and performance analysis.

Behr-Hella Thermocontrol (BHTC) | Product Development Intern| HIL System, CAN protocol **December 2021- May 2022**

- Engineered and validated emulated virtual ECU modules and sensors for **HIL testing**, ensuring realistic replication of physical behavior on **CAN** bus networks, reducing **debugging time by 70%.**
- Automated testing workflows using **Python** and **C**, slashing test execution time from **9–10 hours** to just **6 minutes**, significantly improving resource utilization and overall efficiency.

PROJECTS

- **Functional Verification of LC3 Microcontroller with UVM** Link
  Technology used: SVA, UVM methodologies, Layered testbench, OOPS, Mentor graphics
  - Created class-based **UVM** testbench agents of **environment, monitor,** and **driver** BFM for decode & execute stages of LC3.
  - Implemented **UVMF** into a chip-level UVMF test bench integrating other stages of RISC Processor
  - Developed a functional coverage model involving **CRV** and **directed tests** to obtain functional coverage of **98%**.
- **Functional Verification of I2C Multiple Bus Controllers** Link
  Technology used: SVA, SVTB, CRV testing, Layered testbench Arch, OOPs
  - Created a test plan, generated necessary **constrained random stimulus**, and placed **SVA checkers** to close functional coverage on a wishbone to i2cdevice.
  - Implemented **Layered testbench components** such as Generator, Drivers, agents, Monitors, Scoreboard, and Predictor.
  - A **virtual interface** between the design and testbench was used to establish and drive the ports on a signal-level basis.
  - Successfully achieved **97.54%** of Functional Coverage and **80%** Code Coverage.
- **ASIC Design of Deep Neural Network** Link
  Technology used: RTL Design, Verilog, Timing Analysis, FSM Design, Design Vision, Synthesis
  - Designed and implemented **RTL** for a multi-stage deep neural network accelerator, integrating convolutional, ReLU activation, and max pooling layers with an **FSM-driven control path** to enable **efficient and scalable computation.**
  - Optimized performance metrics using STA & Design Vision, achieving a **9ns** clock period and a logic area of **7759.2 µm²**.
- **Tomasulo's Algorithm for Out-of-Order Execution** Link
  Technology used: C++, OOPs concepts, instruction stages implementation
  - Simulating a fully **pipelined CPU** that implements Tomasulo's algorithm for **out-of-order execution** of instructions.
  - Modeled out-of-order **superscalar processo**r that processes N instructions per cycle and studied performance by measuring IPC. The model eliminated **false dependencies** by using **Register renaming** with the help of the **Reorder buffer**.
- **64 Bit(16x2) Port synchronous SRAM at 3nm Node** Report
  Technology used: Synopsys custom compiler, FreePDK3 library, 3nm Process
  - Designed **gate-level** logic for a **3nm** SRAM with an **8-bit cell array**, TSPC clocking, row & column decoders, and pre-charge circuit, simulating successful component integration.
  - Completed **physical layout** with **DRC, LVS**, and netlist extraction, achieving a **0.08ns** clock period, **982 transistor**s, 10.93µm² area, and an **EDA metric** of **75pJ-ns-µm²**.
- **Performed Physical Design and Optimized Area*Delay*Layer metric** Link
  Technology used: Physical Design, Tcl, Make, Python, Unix
  - Developed script in **Unix**, **Python**, **Perl**, and **Tcl** to extract key metrics from ICC2RM results.
  - Executed physical design with **zero DRC and setup/hold violations**, while optimizing **area*delay*layer** metric.

SKILLS

Programming Languages: System Verilog, UVM, Verilog, VHDL, C, C++, System C, Assembly Language, Python, Tcl, Shell, Make.
Tools: Questa-mentor graphics, Xilinx-Vivado, Cadence Virtuoso, Synopsys Design Compiler, ModelSIM, MATLAB Simulink