Hello,

I am Jessica Vaz, a first-year master's student at the University of Illinois, Urbana-Champaign. I am reaching out to express my interest in summer internship opportunities related to computer architecture and RTL design at AheadComputing.

Before joining UIUC, I worked as an ASIC design engineer at SiFive, where I contributed to the development of reference platforms for flagship RISC-V processors. My experience includes:

Designing an SoC based on SiFives automotive-class processor E6-AB, featuring a dual-core lockstep processor (DCLS) for functional safety

Enhancing SoC security through a hardware-based trusted execution environment, World Guard

Integrating NVIDIAs deep learning accelerator (NVDLA) with SiFive's X280 processor

Hands-on experience with tools like Xilinx Vivado, Synopsys VCS, and Verdi, and FPGAs like Xilinx VCU118 and Arty-A7-100T

At UIUC, I am a Research Assistant working with Prof. Kirill Levchenko on hardware-based trusted execution environments (TEEs) and bitstream reliability. Additionally, I have worked on a few projects using System Verilog:

A fully functioning RV32IM out-of-order processor featuring register renaming with a reorder buffer architecture. It also has some advanced features like early branch recovery and split load-store queue

A five-stage pipelined RV32I core with full forwarding.

A two-stage pipelined write-back, write-allocate cache with a pseudo-LRU replacement policy

TAGE branch predictor

I am excited about the possibility of working at AheadComputing. I have attached my CV for your reference. Please let me know if you require any additional information.

Thank you for your time.

Best Regards,

Jessica Vaz