Vignesh Sankararaman

☎ (+1)984-480-6596 ✉ vignesh.sankararaman@gmail.com LinkedIn

Education

North Carolina State University Expected : May 2026

Masters of Science in Computer Engineering - GPA: 4/4

Relevant Coursework: Microprocessor Architecture, Parallel Computer Architecture, ASIC and FPGA Design, Advanced Microarchitecture, Data Parallel Processors, Compiler Optimization and Scheduling

Indian Institute of Technology Tirupati Dec 2020 – May 2024

Bachelor of Technology in Electrical Engineering - GPA: 8.9/10

Relevant Coursework: Computer Organization, VLSI Circuits for Signal Processing, Digital VLSI Design

Technical Skills

Programming Languages: SystemVerilog, C/C++, Python, Verilog, Perl, Linux CLI, RISC-V Assembly, Git
Tools: Xilinx Vivado, Mentor Graphics Questasim, Synopsys VCS, Synopsys Design Compiler, Champsim Architectural Simulator, Gem5 Architectural Simulator

Internship Experience

Computer Architecture Special Interest Group Jan 2024 – Mar 2024

Memory Architecture Research Intern

Remote

- Modelled the behavior of STT-RAM technology for the shared Last Level Cache(LLC) in Champsim architecture simulator.
- Evaluated and implemented various bypass and victim cache algorithms to reduce the miss penalty and improve the average access time in STT-RAM cache as compared to traditional SRAM cache.
- Created a denial-of-service attack against the STT-RAM based LLC and utilized various cache bypass techniques to lessen its impact on the average access time.

Academic Projects

Superscalar Out-of-Order Processor Simulator |*C++* Nov 2024

- Modelled the behaviour of all 9 pipeline stages of an ARF+ROB based Out-Of-Order Processor, with support for superscalar processing of instructions.
- Evaluated system performance (IPC) using SPEC CPU benchmark traces while varying Issue Queue and Reorder Buffer sizes, and adjusting the instruction issue width from 1 to 8 instructions per cycle

Transformer Self-Attention Hardware Unit | *SystemVerilog,Python* Oct 2024

- Designed the compute units required to compute the Scaled Dot-Product Attention activation function and implemented the design in SystemVerilog without using any extra scratchpad memory.
- Tested the design using random input sequences generated by a python script and verified the DUT results with outputs from a golden reference model.
- Pipelined the design for better performance per unit area and synthesized the design using the Synopsys Design Compiler to obtain a clock period of 6 ns and area of 9400 um^2.

Branch Predictor Performance Modelling | *Gem5, C++, Python* Sept 2023

- Utilized the system emulation features of the Gem5 architectural simulator to characterize 3 branch predictors-Never Taken branch predictor, bimodal predictor, and Global History branch predictor.
- Scripted configuration files in python and analysed performance in terms of average BTB hits for various traces, which showed that the global history predictor performed better than the 2 bit saturating counter.

Prefetecher Optimization | *C++* Mar 2023

- Tested out in-built prefetchers in the champsim simulator and implemented the prefetch algorithm prescribed by the paper "CAFFEINE: A Utility-Driven Prefetcher Aggressiveness Engine" to observe performance improvements in single core processors - IPC improved by 7 percent compared to the base prefetcher.
- Analysed the effects of varying prefetcher aggressiveness and stride as per the CAFFEINE algorithm in multicore (4 cores) and observed an average IPC improvement of 2 percent on various different traces.

RISC-V Pipelined Processor Design | *Verilog, C++* Dec 2022

- Designed and verified the function of a 5 stage in-order pipeline RISC-V Processor with a seperate I-cache and D-cache and an ALU supporting basic arithmetic and logical functions in verilog.
- Implemented a simple simulator in C++ to simulate the in-order pipeline.
- Developed and verified an additional CORDIC based computational unit in verilog which allows the computation of more complex math functions such as exponential functions, logarithmic functions, and trigonometric functions.