Chandan Gireesha
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EDUCATIONAL BACKGROUND

Master of Science, Electrical & Computer Engineering
San Francisco State University, CA, US | GPA: 3.94/4.00 | Fall 2025
Relevant Coursework: Advanced digital design, Static Timing Analysis, Digital Design Verification, Computer Systems Architecture, Embedded Systems, Advanced Computer Networks, Neural Machine Interface and AI in Engineering.

Bachelor of Engineering, Electronics & Communication Engineering
Visvesvaraya Technological University, India | GPA: 8.42/10.00 | Fall 2023
Relevant Coursework: VLSI design, Microcontrollers, Verilog HDL, Analog Circuit Design, Electronic devices

TECHNICAL SKILLS AND CERTIFICATION

Concepts: Floorplanning, Placement & Routing (PnR), Static Timing Analysis (STA), Clock Tree Synthesis (CTS), Power Optimization, DRC/LVS, Parasitic Extraction, Reliability Analysis.
EDA Tools: Synopsys (ICC2, Design Compiler, PrimeTime, StarRC), Cadence (Innovus, Virtuoso, Quantus, Tempus), Mentor Graphics (Calibre, Questa).
Languages & Scripting: TCL, Python, Shell Scripting, Verilog, C++
Certificates: VSD – Physical Design Flow, Static Timing Analysis.

WORK EXPERIENCE

Hardware Engineer Intern | OpenQQuantify. **August 2024 – November 2024**
- Developed AI-driven design tools for hardware architecture optimization, integrating RISC-V, Linux kernels, and OpenCL-based acceleration.
- Designed and validated processor schemas, pin maps, and hardware interaction models to improve automation in circuit and layout design.
- Conducted performance tuning and power optimization, leveraging machine learning for predictive analysis of processor interactions.
- Debugged and refined hardware-software communication using Python-integrated AI models, enhancing system reliability and efficiency.

Research Assistant | San Francisco State University. **January 2024 – June 2024**
- Designed ML-based timing models to predict interconnect delays, enhancing STA accuracy.
- Extracted and analyzed 10+ key circuit features to enhance prediction accuracy by 15-20%.
- Curated large-scale datasets and reduced simulation runtime by 50%, integrating AI-assisted predictions into EDA workflows.

Graduate Technical Intern | RV Skills Centre for Emerging Technologies **January 2023 – May 2023**
- Assisted in generating timing constraints for critical macros, improving setup/hold margins by 80ps for faster closure.
- Performed post-layout STA using PrimeTime and ICC2, reducing post-routing violations by 15% across multiple process corners.
- Implemented ECO fixes, optimizing high-fanout nets and critical paths, cutting violations by 20% through buffer insertion and logic restructuring.
- Reduced congestion by 20% via strategic macro/standard cell placement and partial blockages, improving routing efficiency.

Graduate Teaching Assistant | San Francisco State University **January 2025 – Present**
- Delivered hands-on instruction for ENGR 301 (Microelectronics Lab) focused on semiconductor devices, MOSFET characterization, and SPICE simulations.

ACADEMIC PROJECTS

Advanced Physical Design of motion estimator in 14 nm library/SHA256 Encryption Algorithm. **Spring 2024**
- Developed a full VLSI backend flow for a Motion Estimator targeting a 16x16 reference block and 32x32 search area, meeting timing at 1.8 GHz
- Conducted floorplanning, placement, clock tree synthesis (CTS), and routing, optimizing congestion and timing closure
- Applied PPA optimizations, reducing area by 10% and dynamic power by 12% through techniques like multi-bit register banking, clock gating, power gating, and multi-VT libraries
- Executed post-layout verification (DRC, LVS, LPE) and extracted parasitics for final timing validation, ensuring tape-out readiness.

Power Aware Physical Implementation using 14nm FinFET Process Design Kit (Synopsys) **Fall 2023**
- Implemented low-power design techniques such as Integrated Clock Gating (ICG) and Multi-Bit Register Banking to optimize power and area.
- Achieved 80% total power reduction and 70% area reduction by applying advanced power-aware optimizations.
- Designed placement and floorplanning hierarchy, ensuring optimal congestion and timing performance.
- Performed physical implementation including placement, clock tree synthesis (CTS), routing, and post-route optimizations
- Generated and analyzed Timing, Area, and Power (TAP) reports, validating improvements through signoff checks.

Design and Characterization of non-volatile latch using resistive memory technologies in 28nm CMOS **Fall 2023**
- Conducted in-depth analysis and RTL design of a non-volatile latch using resistive memory in 28nm CMOS, optimizing power, performance, and area (PPA) with Verilog.
- Analyzed HDL netlist of ReRAM using HSpice and scaled down write transistor widths to meet setup and hold time requirements, achieving significant power reduction.
- Optimized power and delay trade-offs, focusing on reducing active power by slowing down the sense amplifier frequency and minimizing area overhead.
- Utilized Synopsys Design Compiler and Cadence Virtuoso for synthesis and characterization, ensuring adherence to industry standards and achieving robust performance metrics.

ACTIVITIES

- Electrical Team Member | SAE E-Baja India 2022 – Designed and tested power systems for electric vehicles.