Anurag Desai

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Education

Texas A&M University, College Station **Aug 2022 - May 2024**
Master of Science in Computer Engineering ***CGPA 3.73/4***
Relevant coursework: Digital IC Design, Computer Architecture, Advanced Digital System Design, Advanced Computer Architecture, Advanced Hardware Design Functional Verification using UVM, Introduction to Physical Design Automation

Vellore Institute of Technology, Vellore **July 2016 - June 2020**
Bachelor of Technology in Electronics and Communication Engineering ***CGPA 8.74/10***
Relevant coursework: VLSI System Design, Digital Logic Design, Computer Organization and Architecture, Semiconductors Devices and Circuits, Micro-controllers and its Applications, Linear Integrated Circuits, Applied Linear Algebra

Technical Skills

- **Skills:** RTL Design, Digital IC Design, CDC, Design Verification, UVM, AMBA Protocols, STA, Low Power Design
- **Languages:** Verilog HDL, SystemVerilog, C, C++, Python, TCL, BASH
- **EDA Tools:** Xilinx Vivado, Cadence Spectre, Virtuoso, Innovus, vManager, Synopsys PrimeTime, ModelSim

Academic Projects

ASIC Design and Layout of an 8-bit Pipelined Adder with H-Tree | *Cadence Virtuoso* | *SPICE* | *Synopsys PrimeTime*
- Designed a 8-bit pipelined adder by creating schematics and layouts of its standard cell components in Cadence Virtuoso, and ran SPICE simulations using Spectre to analyze AC/DC characteristics such as rise-fall delays and RC parasitics.
- Implemented design using TSMC180nm technology and performed post layout simulation optimizing Power and Delay.
- Performed Static Timing Analysis using Synopsys PrimeTime and achieved timing error margin within 10%.
- Carried out delay optimization of critical path by using logical effort method and gate sizing techniques.
- Cleared DRC/LVS errors at gate-level and sub-block level using Cadence Assura and TSMC rule deck.

Design and Synthesis of Cruise Control System | *Synopsys DC* | *Cadence Innovus* | *Verilog*
- Designed a FSM based cruise control system in Verilog and created a test-bench for the design using NCVerilog.
- Synthesized the RTL design and generated netlists using Synopsis Design Compiler and obtained the area, constraint reports and register count from the gate level netlist.
- Performed Static Timing Analysis using Synopsis PrimeTime to find timing violations.
- Used Cadence Innovus to perform placement and routing of the netlist, computed total number of standard cells and vias, total wire length in the design optimizing PPA of the chip and made sure the design did not exceed 70% utilization.

Custom Design and Characterization of a D Flip-Flop | *Cadence Virtuoso*
- Designed transistor level schematic and layout of a D Flip-Flop using TSMC02 library (180nm).
- Performed post-layout simulations to deduce the rise and fall delays with varying loads across the range of 1fF to 100fF.
- Optimized logical effort and resized the transistors to reduce variation between rise and fall delays across different loads.
- Determined the setup time for rising and falling transitions as well as the clock-to-Q delay of the Flip-Flop.

RTL Design and Verification of a Pipelined MIPS Processor | *Verilog* | *Xilinx Vivado*
- Designed and simulated a 5-Stage Pipelined 32-bit MIPS Processor using Verilog.
- Eliminated Data and Control hazards while also reducing stalls using operand forwarding and hazard detection units.
- Implemented Caches, Subroutine Calls and a Static Branch Predictor to increase the throughput of the Processor.
- Synthesized the design on Virtex5 FPGA platform optimizing the critical path and obtained a maximum frequency of 135 MHz. Also verified the functionality using SystemVerilog testbenches.

Functional Verification MESI Based Multi-Core Cache Coherent System | *Cadence Incisive* | *SystemVerilog* | *SimVision*
- Developed verification test plans for 4-core MESI based L1 cache & L2 cache utilizing pseudo-LRU replacement policy.
- Wrote randomization scenarios both-directed and constrained random testing in UVM.
- Performed simulation and debugging in Cadence Incisive and used SimVision for analyzing the waveforms.
- Added SystemVerilog assertions to check the consistency of the design and cover points to measure functional coverage.
- Analyzed code and functional coverage using Cadence vManager and implemented design fixes for bugs uncovered.

Functional Verification of Hyper Transport Advanced X-Bar (HTAX) | *Cadence Incisive* | *SystemVerilog*
- Designed UVM based testbench components like driver, sequencer, monitor, scoreboard using SystemVerilog and performed simulation and debugging in Cadence Incisive and used SimVision for analyzing the waveforms.
- Verified the design using SystemVerilog assertions and constrained random stimulus and added cover points to measure functional coverage. Used Cadence IMC to analyze the coverage.

- Implemented the verification plan using Cadence vManager, ran regressions to identify edge cases and fix bugs in the design. Achieved coverage closure with 97% functional coverage and 95% code coverage through regressions.

Modelling and RTL Design of an Image Processing System | *SystemC, Synopsys Design Vision, Vista*

- Designed Canny Edge Detector, UART, SRAM and integrated the sub-modules using System Bus to form image processor system using SystemC and Verilog.
- Verified the individual sub-modules of the unified system with SystemC test-benches using Vista tool.
- Implemented the sub-modules in RTL using Verilog and synthesized it using Synopsys Design Vision, optimizing area.
- Performed pre and post synthesis simulation to verify the design using Verilog test-benches on VCS.

Optimization of Parallel Processing In Heterogeneous Multi-core Systems | *C* | *OpenMP* | *CUDA* | *Grace*

- Performed various computational tasks such as Vector operation, Sorting and Matrix Multiplication using OpenMP.
- Implemented a CUDA C program to compare the speedup of those tasks for different parallel computing techniques such as Adaptive Mapping, Workgroup size selection and Task Division.
- Carried out performance analysis of the implementation and determined the MKI to be significantly better compared to hashed perceptron and gshare.

Parallel Computing of Strassen's Recursive Matrix Multiplication Algorithm | *C++* | *OpenMP* | *CUDA* | *Grace*

- Developed a parallel implementation of Strassen's matrix-multiplication algorithm using OpenMP on the Grace cluster.
- Designed a GPU-based version of the algorithm that leverages CUDA and CuBLAS to parallelize workload onto GPU threads, as well as a CPU-based serial version as the baseline for performance comparison.
- Achieved 140× speedup when multiplying 1024 × 1024 matrices on NVIDIA RTX 6000 GPU compared to CPU version.

Professional Experience

Changing The Present **July 2024 – Present**
Computer Engineer *Austin, USA*

∗ Developing tools to automate various tasks such as report generation and data collection using Python, thus improving team efficiency by eliminating redundant activities.

Oracle Corporation **Sept 2020 – June 2022**
Associate Consultant *Bangalore, India*

∗ Developed user interfaces for company stakeholders using Oracle APEX tool with HTML, CSS, PL/SQL, JavaScript.
∗ Experienced in designing the architecture for database-driven applications by understanding the technical requirements.
∗ Obtained hands on experience on Oracle Cloud Infrastructure (OCI). Migrated APEX applications from on-premises to Oracle Cloud and transformed spreadsheets into scalable, secure, responsive, web applications.

Siemens **Apr 2019 – May 2019**
Trainee *Verna, India*

∗ Worked on end-to-end PCB Fabrication process and on MODBUS Protocol software for Digital Relays.
∗ Tested and debugged Relay devices and established a ping command between Relays and PCs.
∗ Worked on applications of the Omicron Device in the Technical Consultant Team using DIGSI and VINCI software.

Certifications

- Cadence RTL-to-GDSII Flow Training
- Cadence Digital Physical Design Domain Certification Training
- Cadence Verilog Language and Application Training
- Cadence SystemVerilog for Design and Verification v21.10 Exam
- Cadence SystemVerilog Accelerated Verification with UVM v1.2.5 Exam

Awards

- Received certificate of appreciation and funding for my research project from Defense Research and Development Organisation (DRDO), a premium R&D organization of India in a project named: 'Design and development of a multi-purpose reversible data hiding in wavelet domain for defense applications', May 2020.
- Received a scholarship for displaying meritorious performance in SSC, Nov 2014 and HSSC, Oct 2016.