ABDULLAH AL OWAHID
Cell: 205-563-9305, Email: owahidcse99@gmail.com, Location: Austin, Texas, USA

OBJECTIVE:

I am currently working full-time in a CPU power and performance team for 7 years. This is a cross-functional team, where I seamlessly transition between pre-silicon, emulation, and post-silicon domains for performance features validation and performance prediction. My work includes focused test writing for functional validation of the features related to performance and identifying failures. I also work on emulation-based performance projections for next-generation cores. My academic research is on computer architecture for power and performance efficiency. I am seeking an RTL design position in the CPU pipeline after years of experience in verification.

EDUCATION:

Ph.D., Electrical Engineering, The University of Texas at San Antonio, January 2015 – May 2022, GPA 3.83
M.S., Computer Engineering, The University of Texas at San Antonio, August 2013 – December 2014, GPA 3.63
M.S., Electrical Engineering, Auburn University, January 2010 - May 2012, GPA 3.25
B.S., Computer Science & Engineering, Chittagong University of Engineering & Technology, January 2001 - December 2005

ACADEMIC PUBLICATION:

Abdullah A. Owahid and Eugene B. John, "Instruction Profiling Based Predictive Throttling for Power and Performance," in *IEEE Transactions on Computers*, vol. 72, no. 12, pp. 3532-3545, Dec. 2023, doi: 10.1109/TC.2023.3306079.
Abdullah A. Owahid and Eugene B. John, "Instruction Profiling Based Fetch Throttling for Wasted Dynamic Power Reduction, "*2019 31st International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD)*, Campo Grande, Brazil, October 15-18, 2019, pp. 29-32, doi: 10.1109/SBAC-PAD.2019.00018.
Abdullah A. Owahid, Eugene B. John, "Wasted Dynamic Power and Correlation to Instruction Set Architecture for CPU Throttling," *The Journal of Supercomputing,* vol. 75 pp. 2436-2454 May 2019.
Abdullah A. Owahid, Eugene B. John, "RTL Level Instruction Profiling for CPU Throttling to Reduce Wasted Dynamic Power," *The 2017 International Symposium on Parallel and Distributed Computing and Computational Science (CSCI-ISPD),* Dec 14-16, 2017.

WORK-RELATED PUBLICATION:

Abdullah A. Owahid, David M. Pawlowski, Carlos M. Giraldo, "HGS+ Validation Using Snippet Methodology," *Intel 2024 Design Test and Technology Conference*, published as a featured journal (top 5%), Santa Clara, USA, July 15-17, 2024.
C. Augustine, A. Afzal, U. Misgar, **A. Owahid**, A. Raman, K. Subramanian, F. Merchant, J. W. Tschanz, M. M. Khellah, "All-Digital Closed-Loop Unified Retention/Wake-Up Clamp in a 10nm 4-Core x86 IP," *2021 Symposium on VLSI Circuits*, Kyoto, Japan, 2021, pp. 1-2, doi: 10.23919/VLSICircuits52068.2021.9492376.

EXPERIENCE:

1. Member of Technical Staff, May 2022 – Present and Sr. Engineer, June 4, 2018, to April 2022, Intel Corporation, Austin, TX
    - Emulation-based performance prediction and directed functional tests
        i. Responsible for performance prediction of E-cores for SPEC workloads using Long Instruction Traces (LIT)
        ii. Debugged and correlated performance-related issues for the LIT snippets using traces and in FSDB
        iii. Directed test writing using in-house tools for E-core's functional validation of architectural, security, and power optimization features
    - Mixed signal verification
        i. Responsible for Clocking, Digital Thermal Sensor, Tunable Replica Circuits, Power Gates and Retention Clamp, and Voltage Droop Detector analog IP validations in the mixed signal environment for E-core
        ii. Mixed signal simulation and debug in digital and analog blocks, Analog and Mixed Signal (AMS) hacks for intentional signal force, and test development for focus validation
    - Silicon execution
        i. Silicon execution/Power-on support for E-core silicon and static and dynamic power data collection
        ii. Verified different power optimization features in silicon execution
    - Collaborated with different stakeholders – within and outside of team members at multiple sites and with different orgs.
    - Mentored junior engineers and enabled them by removing roadblocks
    - Participated in team building, interviewing, and hiring new team members
2. Austin MS/Ph.D. Level Intern – Mixed Signal Verification – Intel Corporation, September 21, 2015 – May 7, 2018
    - Responsible for full chip mixed mixed-signal verification of analog IPs
3. Digital Design Summer Internship - Automotive Core/Platform Design Intern, Auto MCU, Product Development and Hardware R&D, Freescale Semiconductor Inc, Austin, TX, June 2, 2014 – August 15, 2014
    - Responsible for effective power reduction methodologies in IP Design - for low-power IP release
    - IP Power optimization – worked in the design team for generating power-optimized RTL using low power tool Calypto PowerPro and ran regression for verification using VCS and functional equivalence check using SLEC PRO
    - Synthesized optimized IP and original IP for ΔPower analysis using cadence RTL compiler

TECHNICAL SKILL:

Synopsys – dc shell, Design vision, VCS, Verdi, CustomXA, Primetime PX and Nanosim. Cadence - RTL compiler, SoC encounter, Virtuoso, Analog artist, Spectre simulation, Cadence layout XL, Assura for DRC and LVS. Mentor Graphics - ModelSim, Questa, Design Architect, DFTAdvisor, and Fastscan. Calypto – PowerPro, SLEC Pro. OS – Linux and Windows.

PROGRAMMING LANGUAGE:

C, C++, Verilog, SystemVerilog, SPICE, Assembly x86. Linux shell scripts, Tcl/Tk, Perl and MATLAB.