

Hello,

I know youre busy, so Ill be super quick.

Im Nilesh Suryavanshi, a final-year MS Computer Engineering student at the University of Texas at Dallas. Srikanth Srinivasan mentioned to write to you, and I was excited to reach out.

Experience in RTL design and verification, with a focus on CPU microarchitecture and performance optimization.

Developed a UVM-based testbench to verify RISC-V pipeline stages, implementing checks for hazards, forwarding, and branch prediction.

Hands-on experience with Verilog/SystemVerilog, Synopsys & Cadence tools, and static timing analysis (STA).

Strong interest in out-of-order execution, instruction scheduling, and performance analysis of CPU subsystems.

Your teams work on high-performance CPU design perfectly aligns with my expertise and passion.

Id love to contribute and learn from your experience. Would you be open to a quick chat?

Looking forward to your thoughts!

Best,

Nilesh Suryavanshi

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Portfolio

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LinkedIn