Summary:

Keshava Reddygattu is a Master's graduate in Electrical and Computer Engineering from the Illinois Institute of Technology, specializing in VLSI Design and Microelectronics. He has experience as an RTL Design Intern at the National Institute of Electronics & Information Technology and as an FPGA Hardware Acceleration Intern at Maven Silicon. He has strong skills in RTL design, functional verification, and FPGA hardware acceleration.

Name: Keshava Reddygattu

Email: kreddygattu@gmail.com

Phone: (312) 684-1096

Location: Chicago

Country: USA

Position Category: Design: Logic design, Verification: Design verification

Desired Job Role: RTL Design Engineer

University: Illinois Institute of Technology

Degree: Master of Science in Electrical and Computer Engineering (VLSI Design & Microelectronics)

Graduation Year: 2025

Years Experience: 2

Notable Companies: National Institute of Electronics & Information Technology (NIELIT), Maven Silicon

Top Skills: RTL Design, Functional Verification, FPGA Hardware Acceleration, Synopsys Design Compiler, Cadence Innovus, Cadence Virtuoso, Xilinx Vivado, Mentor Calibre, QuestaSim, ModelSim, UVM, Gate-Level Simulation (GLS), Assertion-Based Verification (ABV), Testbenches, Code and Functional Coverage Analysis, Formal Verification, Low Power Design (Clock Gating, Power Gating, MTCMOS), Logic Synthesis, Static Timing Analysis (STA), DFT (Scan Insertion, ATPG), Equivalence Checking, Floor planning, Placement & Routing (PnR), Clock Tree Synthesis

(CTS), IR Drop Analysis, Parasitic Extraction, Power/Timing Closure, DRC/LVS Verification, Verilog, System Verilog, VHDL, Python, C, C++, Tcl, Perl, Shell Scripting, MATLAB, PyTorch, TensorFlow, FPGA-based ML Acceleration, HLS Optimization, Systolic Arrays

Job Intention: full-time

Visa Status: --

Able: no

Subject: Inquiry About Entry-Level Opportunities at AheadComputing

Date Sent: 02-21-2025

Resume: Yes