Summary:

Hardware Design Engineer with 3+ years of experience specializing in FPGA/SoC architectures and RTL-to-GDSII ASIC design flow.

Name: Harshith Reddy

Email: harshith.surakanti@gmail.com

Phone: --

Location: Dublin, CA

Country: USA

Position Category: Design: Logic design

Desired Job Role: FPGA Design Engineer

University: Purdue University Indianapolis

Degree: MS in Electrical and Computer Engineering (VLSI)

Graduation Year: 2024

Years Experience: 3

Notable Companies: Integrated Test Range, DRDO, NTT Data GDS

Top Skills: Verilog, SystemVerilog, TCL, Python, FPGA/SoC architectures

Job Intention: full-time

Visa Status: --

Able: no

Subject: Application for Job opportunities at Ahead Computing

Date Sent: 04-08-2025

Resume: Yes