Nilesh Suryavanshi

Email: nilsuryavanshi46@gmail.com
Address: Austin, Texas, 78736
Mobile: +1 9455274828
Portfolio: int-nilesh.github.io/Hello
LinkedIn: linkedin.com/in/nilesh-suryavanshi

Summary: Seeking Internship/Full-Time opportunity in silicon verification, validation, and Design for Testability(DFT).

EDUCATION

The University of Texas at Dallas, TX, USA **Graduating May 2025**
Master of Science, Computer Engineering *GPA 3.741/4*
Coursework: VLSI Design, Computer Architecture, Machine Learning, Testing and Testable Design (DFT), Advance Digital Logic, Design and Analysis of Reconfigurable System, Microprocessor and Embedded Systems, Functional Verification.

University Of Mumbai, India **August 2013 – May 2017**
Bachelor of Engineering, Instrumentation *CGPA 8.55/10*

TECHNICAL SKILLS AND CERTIFICATION

HDL: Verilog, SystemVerilog.
Programming/Framework: Python, C, C++, Git, Jira, Linux.
Tools: Synopsys (DesignVision, VCS, PrimeTime, HSPICE, WaveView, TetraMAX), Cadence (Virtuoso, Innovus), QuestaSim, Xilinx (Vivado), Intel (Quartus Prime), MATLAB.
Methodologies: Logic Synthesis, Static Timing Analysis (STA), Clock Domain Crossing (CDC), Logic Equivalence Check.
Cadence Certifications: Basic Static Timing Analysis (01/2024 - Present, RTL-to-GDSII Flow (3/2024 - Present)

ACADEMIC PROJECTS

Fault Analysis on Digital Circuits (DFT, Tetramax) **Spring 2024**
- Performed Scan insertion using **Design Compiler** and **ATPG** using TetraMax.
- Implemented gate-level circuit to detect **stuck-at-faults** and assess fault coverage.

Standard Cell Library Design (62nm CMOS Technology, Verilog) **Fall 2024**
- Synthesized RTL design of Matrix Vector Multiplier with **custom standard library**, also Created the **Schematic and Layout** of 13 Standard Cells including **D-Flip-Flop** in cadence Virtuoso.
- Performed **DRC/LVS/PEX** and simulated gates using **SPICE** to verify functionality.
- Generated **liberty files** using Synopsys PrimeLib and Place and Route using Cadence INNOVUS
- Performed **Static Timing Analysis (STA)** using Primetime to obtain the optimal clock for the design.

32-bit Processor Design and Verification (SystemVerilog, UVM) **Summer 2024**
- Defined the architecture and executed RTL design to create CPU using **RISC-V Instruction Set**, and **Pipelined Architecture.**
- Enhanced design efficiency through the implementation of **Data Hazard handling** and **Branch Detection.**
- Implemented the **Verification Plan** and Test Plan for the processor, using SystemVerilog and UVM.

Artificial Neural Networks to Recognize Handwritten Numbers (FPGA, Verilog, Python, C) **Fall 2024**
- Wrote C code functioning as **high-level system** managing user input, accessing MNSIT database, passing neurons to ANN.
- Developed the code for **trained model of ANN** including the hidden layers and **synthesized** it to map the design on FPGA.
- Achieved goal of designing a complete **HW/SW** system, where ANN mapped on the FPGA acted as a **Hardware Accelerator.**

Performance Analysis of Cache Configuration and Branch Predictors (gem5, Python)) **Fall 2023**
- Assessed **effects of cache parameters** like associativity, size, block size to determine efficient configuration for **minimal CPI.**
- Evaluated the effects of parameters like predictor size and branch target buffer on accuracy for multiple **branch predictors.**

Finding Shortest Timing Paths in ISCAS'85 Benchmark Combinational Circuits (C++) **Fall 2023**
- Developed **C++ Script** for parsing **netlist** and extracting critical design parameters like input/output gates, fan-in/fan-out.
- Created the **weighted directional graph** from input to output with corresponding fan-outs as path delay.
- Implemented **Dijkstra's algorithm** to find the shortest path between input and output of given circuit with respect to fan-out

PROFESSIONAL EXPERIENCE

CE Lab Assistant, University of Texas at Dallas, Richardson, Texas **December 2023 – Present**
- Working with a professor to implement **HLS designs on FPGAs** and explore hardware utilization for optimized solutions.
- Managed circuit board printing machine **LPKF S64**, Used **EasyEDA tools** to design the single and double-layer circuits, and updated given circuits according to machine requirements.

Firmware Engineer, Bosch, Bangalore, India **September 2022 – August 2023**
- Led complete **Firmware design** of cooperative regenerative braking function and incorporate **functional safety.**
- Integrated, tested and maintained firmware of **CRBS ECU** to ensure software functionality and performance.
- Created **Python test modules** and scripts to optimize hardware testing processes.

System Engineer, Tata Consultancy Services Limited, Mumbai, India **January 2019 – September 2022**
- **Led a team of 6 engineers** to develop **AUTOSAR** compliant MATLAB Models using Simulink, Integrated MATLAB models and performed **unit testing, functional testing**, and **static code analysis** using Polyspace.
- **Onsite coordinator** for PFSM ECU, handling everything from model design to deployment and in-betweens.
- Established communication between MATLAB and Blender using Python for 3D model visualization.