

Dear Hiring Manager,

I am excited to apply for the Formal Verification Engineer position. With a strong background in Computer Architecture, Design Verification, UVM I am eager to contribute to ensuring the correctness and efficiency of high-performance RISC-V cores.

My experience includes hands-on work with formal verification techniques for both data and control paths, as well as proficiency with model-checking tools. I thrive in collaborative environments and am highly motivated to develop innovative verification flows that enhance design correctness.

I would welcome the opportunity to discuss how my skills align with your team's needs. Please find my resume attached for your review.

Nilesh Suryavanshi, MS CE

Student Assistant, ECE Labs

The University of Texas at Dallas