SAI SRIKAR DOKKA

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EDUCATION

B.Tech in Electronics and Communication Engineering Dec 2021 - Present
VNR Vignana Jyothi Institute of Engineering and Technology, Hyderabad, Telangana, India CGPA: 8.1

EXPERIENCE

Undergraduate Project Intern, Mars Lab, IIT Guwahati Aug 2024 - Present
Project Title: Performance Improvement of Multicore Processors Using Wireless On-chip Interconnects

- Designed and implemented a wireless on-chip communication model in gem5, emphasizing token management in Wireless NoCs.
- Integrated and evaluated MAC protocols, including FDMA and TDMA, to mitigate congestion in wireless router networks.
- Developed a dynamic token-passing mechanism that optimizes token cycle allocation, reducing token wastage and improving performance efficiency.

Summer Intern, Mars Lab, IIT Guwahati Apr 2024 - Jun 2024

- Conducted detailed performance modeling and analysis of multicore CPU architectures.
- Leveraged Gem5 simulator, C++, Python, and Ubuntu to create and test architectural simulations.
- Designed and integrated AES and Prince cipher RTL blocks with the Garnet network interface to encrypt data flit-wise, ensuring secure and efficient packet transmission

PROJECTS

Development of a Wireless On-Chip Communication Framework:

- Enhanced the gem5 architectural simulator by integrating wireless communication features using C++ and Python.
- Implemented packet broadcasting across wireless routers within an 8x8 Network-on-Chip (NoC) framework.
- Developed a dynamic token-passing mechanism that adjusts the round-trip time and allocates token cycles dynamically, significantly reducing token wastage.

Design and Implementation of an L1 Cache Simulator:

- Created an L1 Cache Simulator in C++ supporting direct-mapped, fully associative, and set-associative cache designs.
- Incorporated LRU and PLRU replacement policies alongside Write-Back Write-Allocate mechanisms for precise emulation of modern cache behavior.
- Ensured reliability and accuracy by validating functionality using SPEC2017 application trace files.

Bursty Traffic Simulation in 8x8 Network-on-Chip (NoC)

- Designed a bursty traffic generation model that simulates CPU memory access patterns under varying loads within an 8x8 mesh NoC.
- Implemented an algorithm to randomly select bursty routers and generate traffic spikes at varying intervals, mimicking real-world traffic bursts from cpus.
- Optimized the model to ensure diverse burst patterns by adjusting burst durations, intensities, and intervals for comprehensive congestion analysis and routing efficiency testing.

Enhancements in Garnet Network: Buffer Monitoring and Acknowledgment Packet Generation:

- Designed and implemented a buffer occupancy monitoring feature for virtual channel buffers within input units, utilizing the Garnet standalone network router.
- Captured detailed statistics on buffer usage across the network, generating comprehensive files for tracking and analysis.
- Developed and integrated an acknowledgment packet generation feature to automatically send acknowledgment packets from the destination router back to the source upon successful packet delivery.

Implementation of AES RTL Blocks for Garnet Network Interface:

- Designed and developed RTL blocks for AES and Prince ciphers to provide encryption capabilities.
- Integrated the encryption blocks into the Garnet network interface, enhancing secure data communication.
- Ensured seamless operation of the network interface with the newly integrated cipher blocks through rigorous testing and validation.

SKILLS

- **Certification and Coursework:** Multi-Core Computer Architecture Elite NPTEL Certification, NoC interconnect optimizations, Cache, Speculation and Branch Prediction
- **Programming Languages:** C, C++, Verilog, Python
- **Developer and Simulator Tools :** Gem5(Cycle-accurate simulator), Vivado, MATLAB, Linux, Windows

EXTRA-CURRICULAR ACTIVITIES

IOT Club Technical Lead

- Organized VNRVJIET's Openhouse at VNR VJIET and been a part of internal team.
- Organized IOT 2k23 hackathon at VNR VJIET and mentored various projects in the hackathon.

REFERENCES

Dr. John Jose Email: johnjose@iitg.ac.in
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