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SUMMARY

Currently providing DV support to the defense industry in tandem with improving processes and best practices to be more efficient based on commercial industry experiences. Additionally, developing HPC technology to move compute speeds to 100Ghz and provide a pathway to get to 1.0THz clock speeds. Planned out the architecture for a USB HUB SoC chip design that will drive three separate 4K displays. Learned the in's-n-out's of **RRAM** technology, at TSMC, as well as providing verification support for both the technology and product development efforts. Recently finished a **Full-Stack** development program for cross-platform application development. Discovered the true power and *beauty* of the **ESP32 IoT** modules! Successfully used **AWS Cloud FPGAs**! Co-inventor on seven **A.I.** & Autostereoscopic related patents that were granted between Nov. 2018 and July 2021. I have been involved in the design (at both the system-level and low-level), micro architecture, verification, validation and testing of semiconductors ICs. This includes: ASICs, **FPGAs (Xilinx/ Altera/ Lattice/ Actel)**, SOCs, Microcontrollers, Microprocessors (68K/X86/ARM/MIPS), **Microprocessor design from scratch** (**dsPIC & SnapDragon**), Memory (SRAM & Flash), Data Converters (A/D & D/A) and interfacing with MEMS Based Sensors (Accelerometers, Gyroscopes & Magnometers from ST, Freescale & Analog Devices). I have made the transition from **Verilog** to **SystemVerilog** for both Design and Verification (UVM Based) efforts. I have also gained knowledge of: Video (NTSC, PAL, HDMI, DPort, LVDS, etc.), 3-D Stereoscopic & Auto-Stereoscopic Displays, 2-D to 3-D Video Conversion, *High & Low Level* Knowledge of USB**,** PCI/PCIexpress, **MIPI (DSI & CSI)**, Analog Design, Layout For Matching, DSP concepts and RF (Analog & Digital) concepts. In addition, to semiconductor design I have also done PCB/PWB design and software development mainly in Assembly Language along with some tasks done in Visual Basic, SQL/dBase, Perl, **Python**, JavaScript, HTML, CSS, C and C++. I have also acquired significant knowledge and skills in ***Machine Learning*** and the design of **Artificial Neural Network (ANN)** functional blocks into high-performance real-time hardware logic designs. Aside from my technical skills, I am an experienced public speaker who is also comfortable giving technical or non-technical presentations. I am also passionate about **collaboration** being the only true approach to achieve *success* in the growingly complex world, which also includes being a champion for educating and mentoring the next generation of engineers; both inside and outside the professional environment! My **technical leadership mindset is based on** sharing my knowledge with others as I enjoy being an educator and **the belief that GREATNESS lies within everyone**; **it just needs help to be brought to the surface**! Additionally, I am a SUPER ADVOCATE for SCRUM and AGILE Programming Practices!!!

PROFESSIONAL EXPERIENCE

HONEYWELL CORP – Aerospace Group, Clearwater, FL (Remote from Portland, OR) **Aug. 2023 – Present**
Design Verification Engineer

- Performing mainly verification with some design efforts at Honeywell for the defense industry targeting Xilinix FPGA platforms as well as ASIC.
- Responsible for Full-Chip Gate-Level sims, both post Front-End (FE) synthesis @ 0-delays and post Band-End (BE) work (i.e. clock-tree, scan and BIST insertion) with SDF annotation. This also includes the generation of **SAIF** files for super accurate chip power analysis using Prime Power.
- Debugging/working with code written in Verilog, SystemVerilog and VHDL
- Mentoring other engineers to bring commercial industry experiences to the defense industry on various projects.
- Coding up: UVM Drivers, Agents, Monitors and Predictors from scratch along with planning to properly handle error injections.
- Now comfortable with being able to develop a UVM based testbench from scratch!!!
- From scratch, wrote an Excel based VBA script to parse and analyze two other active sheets that contained I/O pad planning related information to then generate another sheet that contains a "physical" representation, i.e. Top/Bottom/Left/Right, sides of the ASIC bonding pads along with coloration for pad groups, the I/O Planner Tool.

TECHNOLOGY LEARNING LABS, LLC, Portland, OR **Nov. 2010 – Present**
Consultant, Engineer & Educator

- Developed a new type of computing system (Computing 2.0) that will bring super computing to the masses with compute speeds easily in the 100GHz range while also laying down the pathway to get to 1.0THz compute clock speeds.
- Provided architectural support for the design of USB HUB chip SoC design with Silicon Motions with the goal to drive three separate 4K displays simultaneously.
- Developed a novel omni-directional autostereoscopic display technology

- Worked on the development of an Augmented Reality gaming platform that brings together Video Gaming with Remote Control Devices using the **ESP32** IoT modules, specifically the **ESP32-WROOM** and **ESP32-CAM** modules.
- Providing consulting services (design and verification) to help in all aspects of technology develop in the semiconductor industry. From the circuit and chip-level on up to system (SoC) and product levels.
- Developed a hardware solution to accelerate **Machine Learning**, by focusing on adding hardware acceleration to the implementation of the back propagation equation used during the training of **Artificial Neural Networks (ANN)** thus significantly accelerating the overall training time of **ANNs**!
- Providing an award-winning STEM workshop to Portland-Metro area school to help expose student to engineering well before they get to college. While exposing them to all the different types of engineering, the workshop goes in depth into electrical engineering, with the students building their own A.M. radio, and A.M. radio station, from scratch!
- Moved beyond the technical aspects of the Agile mindset and can see the connections to operations and business thanks to the "The Age Of Agile" book!

CIRRUS LOGIC, Austin, TX (Working Remote in Portland, OR) **Aug. 2022 – Mar. 2023**

Design-Verification Engineer

- Started off on a technology development project to evaluate the performance of the RRAM (Resistive-RAM) technology being offered from TSMC and as part of my involvement I discovered that TSMC was not properly characterizing the RRAM, which means that their other memory arrays might not be properly characterized as well...a possible industry wide oopppss!!!
- Eventually moved to a project that was using the RRAM technology in an actual audio chip product for a MAJOR customer, where my main roles was to provide chip-level verification support for the RRAM interface and control logic, along with security related aspects not present in the technology development effort.
- Developed RRAM Verification Plan for both the RRAM Technology Development effort and the audio chip product effort
- Developed a base randomized test case for the RRAM block IP that is then used with selective constraints to carry out a bulk of the verification plan and still provide randomization.
- Added functional coverage as related to the RRAM block for the audio chip product.
- Provided general debugging support for other blocks, as there were dependencies to access the RRAM block, as well as provide TB debug support as well given that there is an entirely separate team and resource assigned to handle testbench related matters.
- Also mentored other engineers from interns to experienced engineers, just something I like to do and more often than not, it is not long before they too are helping me! ;-)

HEWLETT-PACKARD, CORP. (HPQ), Vancouver, WA **June 2021 – March 2022**

NOTE: Denied Religious Exemption From Vaccination => Administratively Terminated

Expert Digital ASIC Design Engineer

- Provide design and verification of digital ASICs used in laser and inkjet printer products.
- Provide overall design and verification support as well.
- Only after three weeks on the job, including spin-up time, caught and fixed a bug that made it into two prior chips
- Just after two months verified and finished a design feature that had not been reviewed for more than two years and is not operational in the prior two chip designs.
- Working as part of a VERY global team worked with a design engineer in Korea to remove two timing-loops from their design and as a result developed a method to quickly locate the source of the timing loop in RTL code.

MEGH COMPUTING CORP, Hillsboro, OR **Jan. 2020 – Mar. 2020**

A.I./RTL/FPGA Engineer (DIRECT CONTRACTOR)

- Reviewed and documented the AWS Cloud FPGA workflow, which involved resolving I.T. infrastructure issues, particularly challenges encountered with regard to VNC connections.
- Worked on integrating current in-house FPGA shell wrapper with the AWS Cloud FPGA (Xilinix's **Alveo U200**) workflow targeting Video and A.I. FPGA based code acceleration.
- Independent of the FPGAs being in the cloud, successfully generated PCIe bus transactions from the FPGA to both read and write from the system's Host memory, which involved converting the Host's allocated memory's virtual address into a physical address, which is then provided to the FPGA. This effort included RTL coding as well as writing Host code in C, as well as working to create "huge" continuous page allocations, i.e. greater than 4KB, via mmap().

INTEL CORP, Hillsboro, OR **May 2018 – May 2019**
SoC Design Engineer

- As part of the DDG (Device Development Group) provided validation of the next generation mobile SoCs
- Worked to help improve the practices and processes to be more in line with industry current practices.
- Discovered and got training on SCRUM and Agile practices (via Robert Martin a.k.a. "Uncle Bob" videos and more) and made the connection of such practices beyond Software engineering and became an advocate for such practices.

INTEL CORP, Hillsboro, OR **Mar. 2017 – Sept. 2017**
Validation Engineer (CONTRACTOR – Via Oxford)

- Providing Validation support for HPC Networking Switch Technology (STL/APR – Project Initials), which includes Full-Chip gate-level simulations and error injection using a UVM flow. Also helped out with overall verification process flow challenges and providing mentoring support to other engineers; especially the less senior engineers as needed!

NORTHWEST LOGIC (NWL) CORP, Beaverton, OR **June 2015 – Mar. 2017**
Verification Engineer (DIRECT CONTRACTOR)

- Responsible for the MIPI CSI-2 D-PHY/C-PHY Verification IP (VIP) integration with the NWL MIPI CSI-2 Design IP.
- Worked through issues encountered with SmartDV VIP deliveries.
- Developed MIPI RX & TX C-PHY Behavioral Models in SystemVerilog
- Successfully executed a system-level performance analysis, along with direct customer support & reporting, as related to the effort, for a MAJOR customer that involved the integration and verification of two D-PHY models, one RX and one TX, provided from two different PHY vendors.
- Provided both internal and external support for MIPI CSI-2 and DSI IP technologies
- Assisted in the development of a MIPI targeted UVM based Testbench from scratch!
- Mentored and trained up three new engineers on MIPI CSI-2 technologies, including detailed training on the MIPI D- and C-PHYs. This included the development of the curriculum to perform the necessary training…aside from technology, I enjoy mentoring and teaching in both a professional capacity and in the community at-large! ;-)

VEFXI CORP, Hillsboro, OR (*** **START-UP COMPANY** ***) **Feb. 2014 – June 2015**
Vice President/TECHNICAL LEAD (DIRECT CONTRACTOR)

- Responsible for taking the 2D-to-3D Image/Video conversion algorithms developed in Processing/Java and mapping the algorithm to realizable digital hardware targeting ASIC product development, but first using **FPGA** for prototype development. Using the **Xilinx Vivado** tools, the design placed in the **Xilinx KC705** – Kintex7 FPGA Ref. Brd.
- Developed a design automation script in Python from scratch that would take a JSON description, whose data structure was also defined from scratch, of an **Artificial Neural Network (ANN)** that would then generate the necessary RTL code (in Verilog/SystemVerilog) that can be synthesize/mapped to fundamental digital logic building blocks.
- Responsible for the **Machine Learning** process to ensure that the system's **ANN** gets the appropriate parameter values in order to properly convert 2D Images/Video to 3D Images/Video real-time including support for 4K video resolutions.

NORTHWEST LOGIC (NWL) CORP, Beaverton, OR **May 2012 – Feb. 2014**
Verification Engineer (DIRECT CONTRACTOR)

- Integrated the OVM/UVM based SmartDV VIP with NWL's (MIPI) DSI IP using SystemVerilog to verify both the NWL DSI Host and Peripheral design IP. Reviewed prior SmartDV VIP integration efforts with NWL's (MIPI) CSI IP.
- Put together PCIe DMA tests along with setting up nightly regressions for the NWL PCIe IP.
- Developed processes using Python to automate the generation of RTL code and documentation for DDR IP Registers. Along with adding initial register design efforts for CSI-2 IP via automated RTL code generation.

OREGON INSTITUTE of TECHNOLOGY (OIT), Portland, OR **Jan. 2012 – June 2012**
Adjunct Professor (DIRECT CONTRACTOR)

- Taught Digital Logic and Computer Architecture courses using Verilog to implement the designs during labs using CPLDs / FPGAs. (**Lattice MACHXO2 FPGA** Boards)

TERADYNE CORP, Tualatin, OR **Aug. 2011 – Feb. 2012**

Design &Verification Engineer (CONTRACTOR – Via CDI)

- Designed one new module from scratch and designed one module as a re-work of a legacy module for a J750 tester system. The two modules are part of a Parametric Measurement **FPGA**. Finished 1st design in one month and 2nd design in just under 2 months later!
- Shifted to Verification to help out with the verification effort backlog by carryout verification of OTHER design modules within the same Parametric Measurement **FPGA** using System Verilog via OVM/UVM.

CYPRESS SEMICONDUCTOR, Beaverton, OR **Apr. 2011 – Aug. 2011**

Silicon Validation Engineer (CONTRACTOR – Via Oxford)

- Developed tests to validate the **USB** and SIO & GPIO Functionality on the PSoC5 first silicon using C, C++, C# and Python using the PSoC Development Kit and an internally developed desktop test system (VTS).

DIGITAL DATA INNOVATIONS LLC, Portland, OR (*** **START-UP COMPANY** ***) **Dec. 2008 – Apr. 2011**

CEO & Founder / Systems Architect

- Drawing from my microprocessor and digital communication experiences, developed a novel Digital Communication Packet Processor Architecture that is both protocol and medium agnostic. Developed the design using an Architectural Description Language (ADL) called LISA (Language for Instruction Set Architecture). Successfully generated the receive path packet processing core using LISA and simulated it in an independent simulation environment from the CoWare environment to ensure auto-generated Verilog code was valid. Also got the design to synthesize into an Altera Stratix II. Initial development focused on the Ethernet protocol from 1Mbps up to 10Gbps rates and standards, which included related PHY layer research.
- Developing a consumer fitness monitoring product from scratch, using readily available components, that leverages current MEMS based sensors to enhance workout experiences in order to achieve the optimal performance during competition or simply more optimally achieving an individual's fitness goals when working out at the gym or at home.

FOCUS ENHANCEMENTS CORP, Hillsboro, OR **Feb. 2008 – Sept. 2008**

Senior Staff Engineer

- Responsible for indentifying architecture issues for the WiMedia/Wireless**USB** MAC digital sub-system using an ARM946 processor core targeting the Ultra Wide Band (UWB) space of the RF spectrum. Also involved in design custom hardware acceleration where needed to ensure system timing performance objectives were being met. Responsible for the review and optimization of the system's memory sub-systems (TCM, Cache, SRAM, etc.). Involved in the negotiations to get an ARM946 RTL license (with PDTrace RTL code) to replace the hardcore license currently being used; for less than the cost of the hardcore.

AVNERA => SKYWORKS, Beaverton, OR (*** **START-UP COMPANY** ***) **Sept. 2006 – Sept. 2007**

Senior Staff Engineer

- Responsible for the architecting and design implementation of the Application Core sub-system using the **MIPS32 processor core (4KEp)** for use in wireless audio application system. This also included the custom design of a DMA engine to interface to different Color LCD modules, a multiplexed external memory controller and architecting the memory sub-system which included Instruction and Data Cache memories. Design responsibilities also included the integration of other standard peripheral IP such as SPI, I2C, GPIOs, etc. While working on this project, I was very involved in the microprocessor selection and the actual negotiations for the final MIPS core selection.
- Responsible for the architecting and design implementation of the MAC digital sub-system using the **MIPS32 processor core (4KEp)** for use in 2nd wireless audio system. Worked closely with the firmware engineer to debug and resolve system level issues in both SW & HW. Unique from the prior project was the need to support multiple clock frequencies for the MIPS while running the peripheral bus at a lower frequency. Design responsibilities include the custom design of a master timer event unit and the integration of other standard peripheral IP such as SPI, GPIOs, etc. However, leveraging the MIPS Core experience with the prior project, from the time that I started on the project to silicon on hand took just 16 weeks with first pass success. This work also involved working closely with the radio portions of the system in which we used a custom communication protocol that combined Frequency Hopping with an OFDM/256-Pt. QAM modulation scheme thus avoiding interference with Wi-Fi, as the system used the same ISM band at 2.4GHz, with the full digital portions of the radio simulated in NC-Verilog. This effort included bringing up the design using **Xilinx FPGAs** for pre-silicon system-level verification. ALL culminating in an "emotional" first-pass success of a rather complex single-die system (i.e. Radio (including small PA), DSP (Comm. & Audio), Audio Amps, Power Management, Memories and Microprocessor on the same die)!

STEXAR CORP, Beaverton, OR (*** **START-UP COMPANY** ***) **Sept. 2005 – Aug. 2006**
Staff Engineer

- Provided CPU design and verification of a X86 in-order processor core.
- Responsible for Integer Unit (Logical/Addition/Multiplication), Segmentation Logic within the memory sub-system and some of the logic for Load/Store Conversion X87 instructions.
- Generated a number of directed X86 assembly test cases.

QUALCOMM, INC., Cary/Research Triangle Park, NC **Mar. 2004 – Feb. 2005**
Senior Design Engineer

- With an ARM Architectural License, I was part of the initial team that provided CPU design and verification of an advanced ARM architecture which is known as the **Snap Dragon Processor**
- As part of the Execution Unit team, designed and verified the RTL logic for the following ARM instructions: CLZ, SEL, REV, REV16, REVSH, RBIT, SSAT, SSAT16, USAT, USAT16.
- Designed the microarchitecture logic within the Execution Unit to control the in order dispatching of instructions for a dual issue multistage (14 & 16 stages) CPU instruction pipelines.
- Shared responsibilities for implementation of the RTL logic for the core "multiplication" instructions.
- Generated a number of ARM assembly test cases.

MICROCHIP TECHNOLOGY, INC., Chandler, AZ **July 1999 – Dec. 2003**
Senior Test Engineer (2002 – 2003)

- After helping to design and validate the dsPIC CPU Core, joined the Product & Test group for the same project (dsPIC) to help take the product to production.
- Responsible for developing procedures and strategies for any "special" testing needs which included: generating Perl scripts to automate the generation of test patterns, generating memory test patterns for both FLASH and SRAM memory structures using the J750 Tester microcode, generated high-speed testing approach to test the dsPIC microcontroller modules at full-speed (120MHz+) using a 100MHz ATE with the ability to go up to 1.6 GHz using the same 100MHz ATE.

Senior Design Engineer (1999 – 2002)

- Successfully introduced and integrated initial Verilog based design synthesis with current schematic based design practices while working on the ROMLess 16-bit Instruction/8-bit Data PIC Processor architecture.
- Designed the microarchitecture of the **dsPIC CPU** Core with shared responsibilities for the overall CPU design.
- **Particular CPU design assignments** included the RTL implementation of the following CPU sub-modules using Verilog: Instruction Decode, Sequencer and Register; Program Counter; Looping Control and Status Register.
- Project Manager (PM) for the development of the methodology and tools to enable integrated generation of design and production test vectors into a single development effort. This involved the generation of perls scripts to automate the process.
- Served as PM for the development of application test cases for the dsPIC CPU Core which included the generation of IIR, FIR and FFT application test cases. This served as a crucial verification effort of the overall dsPIC Core.
- Managed internal and external (contract) design engineers.
- Areas of design experiences include: 16-bit DSP Processor Core, Debugger/Emulation, A/D (SAR Architecture), SRAM (Sense-Amp & Array Topology), Flash Memory, I/O Pads.

INTERSIL CORPORATION (Formerly Harris Semiconductor)**,** Palm Bay, FL **May 1997 – June 1999**
Senior Applications Engineer

- Worked on the design of a video evaluation board system and associated FPGA (Actel), used to demonstrate video decoder and encoder chips, which included providing application support in customer designs.
- Received formal training on the PCI specification to support a PCI based video decoder.
- Provided application support for ADCs and DACs, which included application of DSP, RF and Mixed-Signal concepts.
- Developed a method from characterizing DAC's using a R&S Spectrum Analyzer, the ADC characterization system was already in place.

HARRIS CORPORATION (GASD), Palm Bay, FL **Jan. 1996 – May 1997**
ASIC Designer

- Worked on the Solid-State Compression Recorder (SSCR) project where I was responsible for the design of a flow control **FPGA (Actel)** & ASIC that was used in conjunction with a 50MbPS serial communication switch.

- Designed the PWB/PCB boards for both the flow control and serial communication boards. Assisted with the development of a DRAM controller ASIC.
- Responsible for integrating the flow control design and another design into a single ASIC to help reduce costs, which involved the multiplexing of pins and the removal of a ripple counter from the other design.

PRE-DEGREE/DURING COLLEGE WORK EXPERIENCE

DATA COMMUNICATION TECHNOLOGY, RTP, NC (*** **START-UP COMPANY** ***) **1995 – 1995**
Design Engineer – Design cell library blocks for Differential Cascode Voltage Logic.
NCSU MATERIAL SCIENCE DEPARTMENT, Raleigh, NC **1993 – 1995**
Research Assistant – Designed a Laser Reflection Interferometry system using a Keithley Metrabyte Data Acq. Board to assist in the monitoring of diamond growth in the lab.
SYMBIOSIS CORPORATION, Miami FL (*** **START-UP COMPANY** ***) **1988 – 1992**
Programmer Analyst – *[MEDICAL DEVICE START-UP]* Production automation using dBase III+/Informix-4GL & mechanical machine validation for laparoscopic and biopsy related medical devices. VERY successful exit, but I was still in high-school and college during this time and got a very small equity position…enough to finish my degree with very little debt, but a very cool experience just the same!
DOW-CORNING WRIGHT THERATEK, INC., Miami Lakes, FL (*** **START-UP COMPANY** ***) **1988 – 1990**
Software Developer – *[MEDICAL DEVICE START-UP]* 6805 Assemble Coding for angioplasty instrumentation that operated on veins & arteries via a roto-rooter medical device. Quasi-successful start-up exit!

TECHNICAL SKILLS

HARDWARE: Microcontrollers, Microcontroller Emulators, PCI, ETHERNET, I2S, I2C, USB, MIPI (DSI & CSI), PCIe, SPI, JTAG, Logic Analyzers, Spectrum Analyzers, Network Analyzers, Oscilloscopes, Multimeters, PCs, MACs, Unix Workstations, Video Pattern Generators (Phillips), Video Analyzers (Tektronix), Data Acquisition Boards, Teradyne J1750 Testers, **FPGAs (Xilinx/Altera/Lattice/Actel), SDF, SAIF**, Arduino & RasberryPi boards, **AWS Cloud Services, AWS Cloud FPGAs**.

SOFTWARE: Microsoft Office Tools, Microsoft Project, FrameMaker, AutoCAD, vi, Unix, USB Host-Side Coding, Cadence Tools, Aldec Tools, Mentor Graphics Tools, Synopsys Tools, Debussy/NOVAS tools, CVS, SubVersion, **GIT,** PerForce, Matlab/Octave, Magma Synthesis & Physical Design tools. Web application development for both FrontEnd and BackEnd.

PROGRAMMING LANGUAGES: LISA (An ADL), Verilog (95, 2k & SystemVerilog), OVM/UVM, VHDL, **Assembly Language** for a large number of 8, 16 & 32 bit µCs and µPs (from Z-80/680x/6502 to 68K/80x86, including **RISC-V**, ARM, MIPS32 and X87), Informix-4GL, SQL, dBase, Spice, Matlab/Octave, **C/C++**, Microsoft Visual Basic, Perl, **Python**, **JSON**, ANTLR, Processing/Java, REACT, Express, MongoDB, Node, NodeJS, **JavaScript**, **HTML** and **CSS**.

PATENTS & AWARD

US 11,070,783 – 3D System Granted July 20, 2021
US 10,721,452 – 3D System Granted July 21, 2020
US 10,277,879 – 3D System Including Rendering With Eye Displacement Granted April 30, 2019
US 10,242,448 – 3D System Including Queue Management Granted March 26, 2019
US 10,225,542 – 3D System Including Rendering With Angular Compensation Granted March 5, 2019
US 10,148,933 – 3D System Including Rendering With Shifted Compensation Granted December 4, 2018
US 10,122,987 – 3D System Including Additional 2D to 3D Conversion Granted November 6, 2018
IEEE*USA – K-12 STEM Literacy Educator-Engineer Partnership Award (2012) – For generating excitement for STEM studies at Cascade Heights Public Charter School through interactive workshops in Milwaukie, Oregon

NOTE: *ALL seven patents involved the use of digital **Artificial Neural Networks (ANN)** in the generation of 3D information*

EDUCATION

Full Stack-Block Chain Developer Program - **Kingsland University** June 22, 2022
https://blockchaincertificate-verify.kingsland.io/certificate/62d79078a6d778d6aad89bbb

C++, VLSI Processing and DSP Graduate Courses, **Florida Institute of Technology**, Melbourne, FL

B.S.E.E. with a Minor in Business, **North Carolina State University**, Raleigh, NC – December 1995