

Summary:

Pre silicon verification engineer with 3 years of experience in diverse ASIC verification areas.

Name: Juan Magana

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Phone: +52 312 210 1393

Location: Zapopan, Jalisco, Mexico

Country: Mexico

Position Category: Verification: Design verification

Desired Job Role: ASIC Verification Engineer

University: TECNM CAMPUS COLIMA, ITESO

Degree: Mechatronics Engineer, Pre Silicon Verification Diploma

Graduation Year: 2021

Years Experience: 3

Notable Companies: INTEL, NXP

Top Skills: C, C++, Python, Perl, Bash scripting, UVM, System Verilog, System C

Job Intention: full-time

Visa Status: --

Able: no

Subject: CPU verification engineer job open

Date Sent: 02-20-2025

Resume: Yes