VIDURA MANU WIJAYASEKARA
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EDUCATION

- Ph.D. in Electrical and Computer Engineering, North Dakota State University May 2016
  - Thesis topic: Equivalence Verification for NCL and Latency-Insensitive Circuits.
- BS in Electrical Engineering (GPA : 3.48/4.00), North Dakota State University Aug 2011

EXPERIENCE

Formal Verification Engineer, FVCTO, Intel Corp. Sep. 2021-present

- Led FPV of TOR in IO coherency agent in server SoC; verified correctness of coherent request flows (e.g. mem ops, snoops) against arch. spec. tables; also verified uarch performance features.
- Successfully executed all phases of the project including: test plan, constraint verification, complexity reduction, coverage, bound analysis, review, and sign-off.
- Provided support for the verification of arch. spec. tables in JG Arch FV.
- Currently leading FV efforts for memory-side coherency agent in server SoC; also leading the activity of formalizing arch. spec. by defining it in a formal table format.
- Verified architectural liveness in client SoC's fabric interconnect in compute block (CCF) that connects cores, LLC, and system bridges.
- Contributed to development of proof structure techniques to enhance FV efficiency and scalability for complex SoC fabric architectures.
- Hands-on experience with multiple IO Sub IP FV projects, demonstrating expertise in formal methodology and memory/IO subsystem architecture.
- Experienced in leading complex projects, including project planning, technical execution, and managing engineers across verification activities.

Digital Design Engineer/Firmware Engineer, Eta Compute Inc. May 2016-Sep. 2021
Eta Compute designs processors that can operate in near threshold (NT) voltage with DVFS capabilities.

- Co-lead in DSP subsystem integration and support.
- Designed an I2S module and asynchronous interface to the DSP in Verilog.
- Integrated 3rd party PDM IP together with timing constraints.
- Written I/O constraints for above peripherals as well as I2C, SPI, and UART.
- Developed synthesis flow, and managed design and timing constraints for 3 successful tapeouts.
- Experienced in MMMC flow, MBIST and DFT insertion; also in low power design, and CPF.
- Managed front end clock tree designs, and worked with backend engineers to resolve CTS issues.
- Performed STA, including statistical STA for NT delay corners.
- Performed gate level simulations with SDF, and power estimations using TCF.
- Wrote kernel functions for DSP subsystem for deployment of neural nets in the platform.
- Developed APIs in C for peripherals in the chip support package.

Research Assistant, ECE Dept., North Dakota State University June 2011-Dec. 2014

- Developed formal equivalence verification methods for NCL and latency-insensitive circuits derived from a synchronous design.
- Built a C++ CAD tool that can verify RTL VHDL code of designs with over 0.5 million gates.