Vivek Ramanathan

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Work Experience

Formal Verification Engineer
08/2023 – 02/2025

Intel Corporation, Advanced Architecture Design Group

- **Formally verified RTL designs** for integer and vector **ALU**s in a next-generation **CPU core**.
- Confirmed correctness of thousands of **micro-operations** executed in the ALUs using the **ACL2 interactive theorem prover**. Performed **symbolic simulation** proofs and traced counterexamples in the RTL code to identify bugs. The counterexamples were converted into **SystemVerilog assertions** for designers to inspect with **JasperGold**.
- Developed an automated **assumption-checking** tool that successfully reduced assumptions for thousands of our datapath proofs, and exposed 26 new RTL bugs. The tool translated ACL2-language assumptions into SystemVerilog assertions and tested them against dynamic validation regressions of an encompassing Design Under Test (DUT) using Synopsys **IDX**. The failures were illustrated and debugged using **Verdi**.
- Streamlined validation of more than 300 formal **x86 ISA** specifications with the development of **NASM** macros and code for **MME** and **XMM** instructions. This validation framework co-simulated and compared our x86 specifications with existing Intel CPUs.

Independent Contractor and Research Assistant
01/2020 – 05/2023

ForrestHunt, Inc. and Formal Methods Research Group, The University of Texas at Austin

- Created a **SPICE**-compatible **circuit simulator** for low-energy, high-speed **Rapid Single Flux Quantum** circuits in the **ACL2 interactive theorem prover**.
- Proved **type safety**, **memory safety**, and **correctness** properties about the simulator's execution using ACL2.
- Optimized the simulator code by inspecting **x86 assembly** generated by the SBCL compiler.
- Implemented techniques involving **functional programming**, **numerical analysis** for linear system solving, and **floating-point** arithmetic/execution.
- Authored a manual explaining the mathematics of **circuit devices**, such as Josephson junctions and inductors.
- Reference: Warren A. Hunt, Jr., Vivek Ramanathan & J Strother Moore: **VWSIM: A Circuit Simulator** (2022). In: Proceedings Seventeenth International Workshop on the ACL2 Theorem Prover and its Applications, EPTCS 359.

Software Engineer I
05/2022 – 08/2022

PRO Unlimited at Meta, Graphics Team, Meta Reality Labs

- Integrated **subdivision surfaces** capabilities into dGdt, a real-time **geometry subsystem** for cinematic-style rendering.
- Implemented **CPU** and **GPU** subdivision in **C++** using the OpenSubdiv library to enable efficient, real-time rendering.
- Developed with **OpenSubdiv**, **CUDA**, and Google FlatBuffers and tested with GoogleTest and Google Logging.

Undergraduate Researcher
09/2018 – 08/2019

Computational Visualization Center, The University of Texas at Austin

- Led an independent research project on using **deep learning** techniques to classify music based on emotion.
- Developed a **neural network**, with **convolutional** and **fully-connected** layers, that used a song's musical features to classify it into one of four emotion categories: happy, tense, dark or bored, pleasant.
- Programmed and tested with **Python Keras** and **scikit-learn**.

Education

The University of Texas at Austin
08/2018 – 05/2023

Master of Science in Computer Science

Bachelor of Science in Computer Science

Bachelor of Science in Mathematics

Programming

C++/C | SystemVerilog | ACL2 Theorem Prover | SystemVerilog Assertions | SPICE Circuit Simulation | x86 | Python | Git