Andrew P. Thomas

Resume

thomasa3@oregonstate.edu Mobile: (971) 716-4882 U.S. citizen
5696 NW 128TH TER, Portland, OR 97229

Interested in Computer Architecture specifically modern CPU, GPU and AI design. Seeking Masters/PhD Program at a leading university.

Education:

Bachelors in Electrical and Computer Engineering — Graduation 2025
with Computer Science Minor (currently 4th year) — 3.99 OSU GPA

Courses:

3.99 OSU GPA in advanced Electrical and Computer Engineering and Computer Science courses.

- ECE 570 - High Performance Computer Architecture — A
- ECE 474 - VLSI System Design — TBD
- ECE 473 - Microcontroller System Design — A
- ECE 417 - Basic Semiconductor Devices — A
- ECE 472 - Computer Architecture — A
- ECE 471 - Energy Efficient VLSI Design — A
- ECE 423 - CMOS Integrated Circuits II — A-
- ECE 422 - CMOS Integrated Circuits I — A
- CS 474 - Operating Systems II — TBD
- CS 374 - Operating Systems I — A
- ECE 375 - Computer Organization and Assembly Language — A
- ECE 372 - Introduction to Computer Networks — A
- ECE 352 - Signals and Systems II — A
- ECE 351 - Signals and Systems I — A
- ECE 323 - Electronics II — A
- ECE 271 - Digital Logic Design — A
- CS 261 - Data Structures — A

Skills & Projects:

- VHDL, System Verilog Design, RISC-V ISA, CPU and GPU Architectures, Cadence Virtuoso, FPGA programming, PCB design, Nix-based Operating Systems, C, C++, Assembly, Spice, Python, JAVA, Analog and Digital Circuit Design
- Created a 90+ dB, 200+ MHz UGBW, with 70+ degree PM Differential in, Differential out Amplifier with stabilizing CMFB thats valid between -45 celsius and 80 celsius corners in Cadence Virtuoso with DRC and LVS valid layout in industry standard 0.18 micron TSMC process.
- Created functional ALU in Cadence Virtuoso with partial layout.
- Coded FPGA to make an external speaker play notes using a Nintendo Controller and included an FSM to play melodies (VHDL)
- Coded FPGA to display a virtual sprite on a computer screen using VGA

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- Coded an FPGA to make an external 7-segment display to act as a timer. The user can set the timer and when it reaches zero an external speaker will sound with different tones.
- Coded AVR board using Assembly to display scrolling strings on LCD screen and implemented fundamental C++ data structures like binary tree
- Server and Client encryption & decryption network setup with multithread and multiprocess capabilities done on a Linux server using C.
- Real-time GPS and Force Modules built on custom PCBs streaming data to the a cloud server at over 100 Hz

Awards (OSU):

- Finley Academic Excellence Scholarship 2021-2025
- Drucilla Shepard Smith Award 2023
  (4.00 GPA)
- Dean's List Oregon State University 2021/22/23/24
  College of Engineering (all quarters - present)