Summary:

Phong Bach is a results-driven Physical Design Engineer with over 20 years of experience in ASIC/SOC IC design. He has worked with Intel Corporation for a significant part of his career, specializing in RTL to GDS physical design implementation. He has a strong skill set that includes ASIC/SOC Design Flows, RTL to GDS Physical Design, Logic Synthesis, Floor Planning, and many more.

Name: Phong Bach

Email: pdbach@yahoo.com

Phone: 971-401-4222

Location: Hillsboro, OR. 97123

Country: USA

Position Category: Design: Physical Design

Desired Job Role: Senior Physical Design Engineer

University: University of Washington

Degree: Bachelors of Science, B.S. Electrical Engineering

Graduation Year: --

Years Experience: 25

Notable Companies: Intel Corporation

Top Skills: ASIC/SOC Design Flows, RTL to GDS Physical Design, Logic Synthesis, Floor Planning, Place and Route (PnR), Static Timing Analysis (STA), Synopsys Fusion Compiler, Design Compiler, Primetime, Synopsys ICC/ICC2, ICC-DP, Conformal FEV (LEC), Functional/Timing ECOs, ICV DRC/LVS Physical Verification, Siliconsmart, Calibredrv, icwbev, TCL, Perl Scripting, Full-Chip and IP Integration, 14nm to 3nm and intel 18A Process Nodes, Leadership and Collaboration

Job Intention: full-time

Visa Status: U.S. Citizen

Able: yes

Subject: Working at AheadComputing

Date Sent: 03-09-2025

Resume: Yes