Hi,

My name is Arpan Raja. I recently finished a year on the Coherent Interconnect team at Samsung Semiconductors. I mainly focused on microarchitecture improvements to save power and increase frequency. My main feature involved an estimated 10% reduction in peak dynamic power.

My main goal right now is to continue interesting microarchitectural work, ideally in the RISC-V ecosystem. Lately I've been researching TileLink, which serves to be a potential alternative to CHI for RISC-V systems. I was looking at the 2 senior positions on the CPU microarch team, for which I believe I am an excellent fit. I did some work a few years back on building a Tomasulo OOO CPU.

I see my skills primary to be of an architect. I came into my Samsung position with little to no interconnect experience and yet I managed to still provide exceptional value to the team and the company. I believe I will do the same here.

In case you are looking for any referrals, I still have a good relationship with the head of SystemIP at Samsung, who has offered to vouch for me.

Position 0:

https://www.aheadcomputing.com/senior-cpu-uarch-execution

Position 1:

https://www.aheadcomputing.com/job-postings

Looking forward to hearing back!

Arpan Raja