NEHA KARUNAKAR RAJU

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College Station, Texas

EDUCATION

TEXAS A&M UNIVERSITY, College Station, TX | Aug 2024 – May 2026 **CGPA:4.0/4.0**

Master of Science in Computer Engineering

Recent Coursework: Microprogrammed control of Digital Systems, Digital Integrated Circuit Design, Advanced digital system design, Advanced Hardware Functional Verification, VLSI Physical Design Automation, Security verification and Validation of Computing Systems

Grader- Electric and Magnetic Fields, Signals and Systems, RF and Wireless Systems

R V COLLEGE OF ENGINEERING, Bangalore, IN | Dec 2020 - Jul 2024 **CGPA: 8.55/10.0**

Bachelor of Engineering- Electronics and Communication Engineering

Relevant Coursework: Analysis and design of digital circuits, Digital system design using Verilog HDL, Microprocessors and microcontrollers, Digital VLSI design, Embedded system design, Low power VLSI, Algorithms for VLSI design and automation, ASIC design, Design for test and testability

TECHNICAL SKILLS

- **Simulation Software:** LTSpice, Proteus, Simulink, MATLAB, Keil µVision, Xilinx Vivado, QuartusPrime, Modelsim, Cadence Genus, Innovus, Xcelium, Virtuoso, Spectre, IMC, Xilinx Vitis HLS, Ansys HFSS, Cadence AWR, Synopsys DesignVision
- **Programming languages:** C, Python, Java, Embedded C, Verilog HDL, x86 assembly, SystemC, Basics of TCL

WORK EXPERIENCE

International Institute of Information Technology, Bangalore (IIITB) | Sep 2023 – May 2024 **[High level synthesis, Hardware Accelerator]**

Research intern

- Development of Verilog code and a parallelized C algorithm for a hardware-accelerated line-following robot, focusing on real-time lane detection using 2D LIDAR SLAM and Hough transform architectures
- Implemented pipelining and optimization techniques, conducted high-level synthesis with Vitis HLS, and validated functionality through co- simulation
- Deployed the final solution on Zynq UltraScale+ MPSoC ZCU104, ensuring real-time performance in image data processing and achieving about 35x speed improvement of the SLAM algorithm

Maven Silicon, Bangalore | Feb 2023 – Mar 2023 **[RTL design, ARM bus protocols]**

Intern

- Designed an AHB-APB bridge to enable efficient data transfer between peripherals and the master in an SoC, ensuring seamless protocol conversion
- Developed a Verilog HDL code using Model Sim and Xilinx Vivado; tested the code across multiple data transfer scenarios, including burst and sequential data transfer. Performed synthesis of RTL hardware using Quartus Prime

PROJECTS

Battery Management System for Electric Vehicle: Application Specific Integrated Circuit |Jun 2023-Mar 2024 **[ASIC Design, RTL-GDS]**

- Developed a Verilog code and testbench for a custom Battery Management System (BMS) control unit using Vivado. Developed the back- end physical design flow Register transfer Level (RTL) to Graphic Design Format II(GDSII) using Cadence tools
  Patent: Filed for patent of ASIC approach algorithm used in the project, Battery Management System for Electric Vehicle at RVCE

Verification of Multi-Core Cache with MESI Protocol and UVM-Based End-to-End Checking | February 2025 **[UVM , Cache coherency]**

- Verified a multi-core cache system using the MESI protocol, implementing end-to-end checking with scoreboards and monitors. Developed UVM components for stimulus generation ensuring robust verification from IP to SoC integration.

Assertion-Based Verification of APB Systems Using Cadence Xcelium and IMC | January 2025 **[Assertion based verification, IP level verification]**

- Performed standalone and IP-level verification of APB Master-Slave systems, including memory and cache components. Utilized Cadence Xcelium for simulation and IMC for coverage analysis, ensuring compliance with protocol specifications and design requirements.

RTL Design & Optimization of a 32-bit Pipelined MIPS Processor **[Verilog, MIPS ISA ,RTL Design]**

- Designed a 5-stage pipelined MIPS processor and its corresponding block components such as Register-File, Data Memory, ALU and Main Control Unit using Verilog HDL. Additionally, optimized the design to detect and mitigate data and control hazards through the implementation of forwarding and hazard detection units

Modeling and RTL Design of an Image Processor System **[Verilog, SystemC]**

- Modeled all sub-modules of a simple image processor system including canny edge detector module, SRAM module, system bus and bus arbiter and integration of the sub-modules to form a simple image processor system using SystemC
  Implemented the sub-modules in RTL using Verilog and synthesis of the design using Xilinx Vivado. Performing pre and post synthesis simulation to verify the design using Verilog test-benches

Custom Design and Layout of an 8-bit Pipelined Adder with Buffered H-Clock Tree **[CMOS Logic,Physical design]**

- Designed schematic and transistor level layout of a pipelined 8-bit adder in Cadence Virtuoso using TSMC02 PDK. Optimized path delay by resizing transistors along the critical path by the method of logical effort

Synthesis and Timing Analysis of Cruise Control Design **[Physical Design, Static Timing Analysis]**

- Synthesized a cruise control design using Design Vision, which involves pre-layout static timing analysis through constraint definition and timing path checks. The synthesized Verilog netlist was utilized for the Place and Route process on a die

RESEARCH PUBLICATIONS

- *Shilpa D R, Sowmya K B, Neha Karunakar Raju, Meghana C S, Shilpa S P*, 'Algorithm for Battery Management System for Electric Vehicles' [Submitted to IEEE ACCESS]
- *Sowmya K B, Shilpa D R, Neha Karunakar Raju, Avaneesh Chintalapati, Dhruv Khare, R Sai Likhith, Vijeth M Satyam*, 'Cell balancing for Electric Vehicles'[Submitted to IEEE ACCESS]