Kumar Subramanian

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Accomplished Principal Engineer with 30 years of expertise in CPU design methodology, and backend implementation. Proven track record of leading the development of high-performance microprocessor components, including Intel Atom/E-core design, spanning multiple generations and process nodes. Expertise in full-stack RTL-to-GDS implementation, PPA optimization, DTCO and collaboration across cross-functional teams, including micro-architecture, physical design, and process technology. Demonstrated ability to lead design studies, drive methodology innovation, and develop cutting-edge automation to enable successful High Volume Manufacturing (HVM) for industry-leading products.

EXPERIENCE

Principal Engineer, Intel Corporation, Austin, TX — 2016-2024

Technical Lead for Intel Atom/E-core design methodology and backend implementation

- Lead for Intel Atom/E-core design methodology and backend implementation, driving the development of Intel E-Core SoftIP (SIP) for multiple CPU microarchitecture generations across process nodes (TSMC N6 - N3, Intel 22nm - 18A).
- Developed a full-featured reference methodology, flow, and design demonstrating achievable PPA for E-Core SIP, encompassing parameterized timing constraints, floor-plans, and convergence recipes. Led implementation of SIP RTL through RTL2GDS (Synthesis, APR + CTS), including sign-off extraction, STA, and power analysis, ensuring a reliable starting point for customer implementations or process node migrations and supporting internal SIP customers.
- Drove the transformation of E-Core from a latch-dominated design to a flip-flop-based architecture, collaborating with micro-architects to re-balance the CPU pipeline to address timing and power challenges, optimizing PPA.
- Led critical design studies on internal and external process nodes, providing recommendations for process node selection based on PPA benefits and technology scaling to Senior Intel management. In addition responsible for convergence of timing/power critical Automatic Place and Route blocks in the CPU subsystem,.
- Spearheaded the design methodology and DTCO for advanced process nodes in collaboration with micro-architects, process technologists, and physical design teams, including the development of automation to address early collateral challenges. This effort drove closure on metal stack, standard cell architecture and design methodology choices.
- Directed multiple test chip implementations, including Intel's first CPU on TSMC process (paving the path for Intel to adopt a dual foundry vendor strategy). Implemented Intel's first CPU featuring Power Via (backside power), but with FinFets, as a de-risking vehicle to decouple the confluence of GAA and Power Via. These test chips were based on E-Core SIP, which has since been adopted by Intel Technology Development team as the vehicle to whet and characterize new process nodes (starting with Intel 18A node). Responsible for evaluating and providing feedback to Technology Development teams on PDK releases from a RTL2GDS implementation perspective, to ensure quality PDK releases to foundry customers.
- Ensured sign-off methodology and closure for timing (including crosstalk, variation), power, and electrical rules, enabling successful CPU tape-outs with zero post-Si escapes. Extensive scripting using native EDA tool API and Perl to data-mine timing models to generate design indicators to track and course correct project progress.
- Developed automation to perform budgeting to derive timing constraints for hierarchical implementation entities from the full-chip context. Performed correlation studies between optimization and sign-off tools, and either worked with EDA vendor or updated tool settings to close the correlation gap, thus ensuring there were no surprises in sign-off. Conducted Spice vs. STA tool simulations to identify bottlenecks in pre-Si to post-Si gaps.

- Developed ECO flows for last mile timing and power closure using a combination of scripting and native EDA tool capabilities, e.g. DMSA based ECO flows in Primetime. Power user of SNPS APR (DC through FC) and STA/Power (PT/Primepower).
- Collaborated with EDA vendors to enhance native tool capabilities, such as Next Generation Latch Analysis (NGLA) in Primetime and SMSCTS in FusionCompiler.

Senior Staff Engineer, Intel Corporation, Hillsboro OR & Austin Tx: 2004-2016

- Architected and implemented the transformation of E-Core backend design from custom internal tools to industry-standard tool suites, increasing transistor density by 1.5X and reducing headcount by 2X.
- Evaluated and implemented MCMM-based optimization flows for high-performance latch-based CPUs, co-developing solutions with EDA vendors to deploy successful HVM products.

Multiple roles leading to Sr. Staff Engineer, Intel Corporation, Hillsboro OR: 1999-2004

- Implemented methodology of cell based design flows for second generation of Pentium4 (Prescott).
- Collaborated with Internal EDA developers to co-develop advanced cell sizing solutions, significantly improving timing and power efficiency, which remain in use across Intel to date.

Sr Design Engineer, TriTech Microelectronics and TriTech Inc: Singapore and Milpitas: 1995-1999

- Responsible for COT designs based on customer netlists, primary customer was Creative Labs.

EDUCATION

- University of Windsor — Master of Applied Science (Electrical Engineering) 1994
- Mangalore University — (Manipal Campus)— Bachelor of Engineering 1990

SKILLS

- Extensive experience in converging high frequency/performance CPU designs, challenged in the PPA domain, and collaborating with micro-architecture and RTL teams.
- Strong track record of collaborating with R&D at EDA vendor, driving vendor to transforming “user scripts” into native tool capabilities in the vendor’s EDA offering.
- Tools, Flow & Methodology development on all aspect of RTL2GDS flows including sign-off flows.
- Synthesis (DC/FC), APR (FC), STA (Primetime), Power analysis (Primepower), TCL and Perl.
- Proven track record of mentoring and grooming junior engineer, helping them grow in the technical track, several of whom are Principal Engineers at Intel and at other companies.

AWARDS/PUBLICATIONS

- Intel Achievement Award (**IAA**), the company’s *highest* recognition: “**Intel Atom Processor on External Foundry**” in 2021. This was for the first full featured Intel Atom processor implemented in an external foundry node (TSMC N5). Recipient of multiple Divisional Recognition Awards.
- Published more than a dozen papers at Intel Design and Test Technology Conference (DTTC). Two external publications, primary author of an invited paper on “High Performance Latch Based Designs” at TAU 2016 and co-author of paper on implementation of a CPU with Power Via presented at VLSI 2023 Symposium, Kyoto.
- Chair of the DTTC “Design” track, handling the submission, review and disposition of over 1200 submissions every conference cycle.