DISHANK DEVENDRA MACHKAR

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EDUCATION

North Carolina State University, Raleigh, NC **May 2025**
Master of Science, Computer Engineering **CGPA 3.85/4**
Relevant courses: Advanced Microarchitecture, Architecture of Parallel Computers, Microprocessor Architecture, Advanced Computer Architecture: Data Parallel Processors, ASIC and FPGA Design with Verilog, Advanced Functional Verification with UVM, ASIC Verification, Computer Networks, ESL and Physical Design

Rajiv Gandhi Institute of Technology, Mumbai University, India **July 2021**
Bachelor of Engineering, Electronics and Telecommunication Engineering **CGPA 8.29/10**

SKILLS AND CERTIFICATIONS

- **Languages:** C++, SystemVerilog, Verilog, Python, Bash, YAML, C#, C, Tcl, VHDL, SQL
- **Software and Tools:** SPEC, UNIX, GPGPU-Sim, Questa Advanced Simulator, Synopsys Design Compiler, ModelSim, Power BI, LTspice
- **Technologies and Frameworks:** CUDA, UVM, UVMF, SystemC, OpenMP, Git, .NET, Microsoft Azure
- **Certifications:** SystemVerilog for Design and Verification Certification v21.10 - Cadence Design Systems, Microsoft Azure AZ-900

ACADEMIC PROJECTS

Register file and renamer module with value predictor
- Simulated structural components including physical register file, active list, free list, register map table and shadow map tables.
- Implemented stride value predictor on C++ with Value Prediction Queue to gain IPC increase with the help of value prediction.
- Performed checkpointing, using global branch mask to handle branch misprediction recovery for the superscalar processor.
- Studied the effect on IPC due to branch prediction, value prediction, memory dependence prediction etc. using SPEC benchmarks.

Cache coherence protocols simulator
- Developed a simulator implementing modified MSI protocol or DRAGON protocol according to input parameters.
- Executed multi cache system coherence protocols in C++ with a configurable number of cores.
- Reported on the performance metrics and analyzed the difference between update-based and invalidation-based protocols.

RTL design and synthesis of quantum computing emulator core
- Emulated a quantum computer, implementing a quantum circuit using operator matrices with complex FP numbers.
- Modelled a device under test on Verilog which interacts with SRAM modules and uses DesignWare components for ALU operations.
- Optimized and synthesized the design using Synopsys to achieve maximum clock frequency of 4.65MHz without timing violations.

Verification of LC3 microcontroller using UVM
- Created a UVM interface package for decode stage of the LC3 microcontroller using SystemVerilog.
- Harnessed UVMF to implement verification for fetch, execute, writeback, memaccess and control stages of the microcontroller.
- Analyzed and obtained functional coverage of 95.50% with the implemented tests using Questa.

Finite Impulse Response (FIR) filter accelerator using SystemC
- Designed a FIR filter Accelerator for use in a SoC with a DMA controller using SystemC.
- Utilized HLS (High Level Synthesis) with Catapult HLS to synthesize the design, achieving timing closure.
- Maximized the speedup (62.5x) of Accelerator implementation with minimal area and least critical path.

Verification of I^2C multiple bus controller core
- Prepared a multi layered testbench for verification of I^2C multiple bus controller with a wishbone master.
- Used SystemVerilog and Questa for simulation and handling the verification process.
- Achieved functional coverage of 97% for the DUT module using random and directed stimulus testing.

PROFESSIONAL EXPERIENCE

Capgemini, Navi Mumbai - India **July 2021 – July 2023**
Senior Analyst/Software Engineer
- Worked as an L3 support engineer using OOP with .NET Core, C#, C++ and SQL to resolve incidents, service and change requests.
- Spearheaded two tech refresh projects and optimized monitoring and health check processes, reducing the duration by 50%.
- Made re-deployable entities for resource creation on Azure cloud, utilizing Shell and Azure DevOps with YAML file driven pipelines.