

MITCHELL SHARUM

32 Mill Street, Mailbox #143, Winthrop Mail Center,
Cambridge, Massachusetts 02138

432-770-2342 | msharum@college.harvard.edu | <https://github.com/r-mitchell-s>

Cherokee registry number: C0325196

Electrical engineer pursuing FPGA and ASIC design and verification roles, experience with SystemVerilog, C++, python

Education

HARVARD UNIVERSITY

Cambridge, MA | 2021 - 2025

B.S. in electrical engineering with a secondary in computer science. GPA 3.48.

TRINITY SCHOOL OF MIDLAND

Midland, TX | 2017 - 2021

GPA 4.0 (unweighted). SAT 1540 (superscore).

Project Experience

FPGA-BASED AUDIO EFFECTS PROCESSOR (ES 100 - Senior Thesis Project)

In Progress

- Designed and Implemented RTL modules for I2S audio processing with DSP algorithms
- Integrated PMOD I2S2 for signal conversion, handling inter-module communications via AXI-Stream

RTL CRYPTOGRAPHIC ACCELERATOR (CS 2540 - Formal Methods in Computer Security)

In Progress

- Implemented Tiny Encryption Algorithm (TEA) in RTL and functionally verified against C++ behavioral model
- Used SystemVerilog Assertions to ensure that the design computes output in constant time

32-BIT MIPS PROCESSOR (CS 1411 - Computer Architecture)

May 2024

- SystemVerilog implementation for the RTL simulation of a MIPS ISA processor
- The microprocessor features a 5-stage pipeline, interfacing with a separate data and instruction memory

Work Experience

HARVARD UNIVERSITY (Teaching Fellow)

Cambridge, MA | January 2025 - Present

- On ES50 teaching staff (Intro to Electrical Engineering), focusing on digital and analog circuits
- Directed laboratory sections and held office hours, taught students circuit theory and debug

CORRECT DESIGNS INCORPORATED (Design Verification Co-op)

Remote | September 2024 - January 2025

- Worked under mentorship of founder assisting on contract-based projects
- Optimized VHDL testbenches for faster, less resource-intensive simulation

CORVALENT CORPORATION (Electrical Engineering Intern)

Cedar Park, TX | May - August 2023 & 2024

- Two internships supervised by the CTO of an industrial computing hardware company

Skills and Tools: SystemVerilog, C++, Python, Perl, FPGA, MATLAB, LTspice, Xilinx Vivado, Tcl, Git, Xsim

Relevant Coursework: Hardware architectures for deep learning, computer architecture, digital design, computer networks, systems organization, signal processing, multivariate calculus and linear algebra, analog circuits