**Jesus Alfonso Lopez Chin**

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## Skill summary

Pre-Si Verification Engineer with 7+ years of experience on ASIC verification and integration.

- **HDL Expertise** SystemVerilog, UVM/OVM, Verilog.
- **Tools** VCS, Verdi, XCELIUM, Git, Quartus II.
- **Protocols** AMBA (APB, AXI4), PCIE 2.0.
- **Languages** Python, Perl, C/C++, Shell scripting.
- **Methodologies** Coverage-Driven Verification, Agile/Scrum, Test Plan Development.

## Professional Experience

**Intel Corporation, Guadalajara, Mexico**
*CPU Design Verification Engineer* **(March 2022 - April 2024)**

- Developed UVM component for core-level event injection via assembly tests, collaborating cross-functionally to address untestable low-level scenarios.
- Built Python post-process checker to validate core-uncore communication integrity.

**Synopsys, Guadalajara, Mexico**
*Verification Engineer – SOC, Engineer II* **(July 2021 - March 2022)**

- Led a 3-member team to develop a UVM testbench from scratch for a DSP project, ensuring end-to-end validation of FIR filters, complex math operations, and data handling (saturation/rounding).
- Designed PCIE verification components and AXI4 test plans; resolved critical bugs via directed testing and BFM enhancements.

**Intel Corporation, Guadalajara, Mexico**
*Pre-Silicon Validation Engineer* **(March 2017 - July 2021)**

- Validated integration of third-party IP (HEVC, AVC, JPEG codecs) into SoC, owning decompression workflows and vendor collaboration.
- Spearheaded feature verification for Zstandard/LZ77 decompression units, including CSR validation, coverage closure, and reset/error testing.
- Automated GPU validation workflows via scripting, reducing manual effort for test execution and error reporting.

## Education

*Bachelor of Electronic Engineering* at Instituto Tecnológico de Estudios Superiores de Monterrey, campus Guadalajara.