# Bhargava Saketh Nagapattinam

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## EDUCATION

**Master of Science in Computer Engineering, Concentration in Electrical Engineering** **May 2024**
The University of Texas at Dallas, Richardson, TX **GPA 3.6/4.0**
**Courses**: ASIC Design, VLSI Design, Testing & Testability Design, Analog IC Design, Computer Architecture, Machine Learning, Microprocessors & Embedded Systems, Advanced Digital Logic, Hardware Description Languages, Database Design, Design of Algorithms
**Certifications:** Cadence Digital Badge- Static Timing analysis, Design for Test Fundamentals, Verilog Language and Application

**Bachelor of Engineering in Electronics and Communication & Engineering** **Jun 2022**
Osmania University**,** Hyderabad, India
***Leadership Experience:*** *Vice-chairperson, IEEE Circuits and Systems Society* (IEEE CASS)

## SKILLS

**Programming Languages**: Verilog, SystemVerilog, C, C++, Python Scripting, TCL, Perl, MySQL
**Verification Methodologies:** UVM, Object Oriented Programming (OOPs)
**Protocols:** SPI, I2C, UART, AMBA (AXI, AHB, APB), USB, PCIe
**Technical Tools:** Cadence (Allegro, Virtuoso, Genus, Innovus), Calibre (DRC, LVS, PEX), Synopsys (VCS, Design Vision, HSPICE, Design Compiler, WaveView, TetraMAX, PrimeTime), ModelSim, QuestaSim, Xilinx Vivado, Eagle, AutoCAD, MATLAB, MS Office Suite, Linux, Unix
**Concepts:** System Verilog Assertions(SVA), Static Timing Analysis (STA), Clock Domain Crossing (CDC), Low Power Design Techniques, PPA

## ACADEMIC PROJECTS

**Computation Algorithm of MSDAP with PPA Optimization | ASIC Design (C/C++, Verilog, Cadence Genus, Innovus)** **May 2024**

- Developed an optimized computation algorithm for the Mini Stereo Audio DSP using Power of Two (POT) techniques in C/C++, reducing hardware complexity by minimizing the use of traditional multipliers. Implemented the algorithm in Verilog, incorporating memory macros, and synthesized the design using Cadence Genus for efficient logic synthesis.
- Successfully optimized Power, Performance, and Area (PPA) by reducing power consumption, improving efficiency, and minimizing chip area by 15% using Cadence Innovus for Place and Route, ensuring the design met stringent PPA targets.

**Standard Cell Library Design Using Gf 65nm Technology, RTL to GDSII Flow | VLSI Design (HSPICE, Innovus, PrimeTime)** **Jan 2024**

- Developed a standard cell library in GlobalFoundries 65nm Technology using Virtuoso, designing and verifying schematics and layouts for basic gates (Inverter, NAND, NOR, MUX, D flip-flop) with minimal delay and area.
  Performed DRC, LVS, and PEX extraction to ensure accuracy and functionality, and simulated using HSPICE for functional validation.
  Implemented an RTL to GDSII flow for a Verilog-based Parallel ALU, utilizing Cadence Innovus for automatic place and route with the custom standard cell library, and ran PrimeTime on the final layout using the extracted netlist to determine the worst-case delay

**2-Stage Differential Amplifier Design | Analog IC Design (Analog Design, Verilog, Cadence Virtuoso)** **Dec 2023**

- Developed a 2-stage differential-input, single-ended output amplifier in Cadence Virtuoso, creating test benches to validate critical parameters including common-mode rejection ratio (CMRR), output voltage swing ratio (OVSR), gain, and phase margin.
- Calculated and optimized W/L ratios, Miller capacitance, and transistor currents based on design specifications. Verified performance metrics such as gain, phase margin, and CMRR through AC analysis, and confirmed OVSR via DC analysis.

**RISC-V Core Functional Verification | Design Verification (SystemVerilog, UVM, AMBA)** **Aug 2023**

- Developed a UVM-based verification environment for a RISC-V RV32I core, verifying ALU operations, load/store execution, pipeline hazards, and branch misprediction handling. Designed and implemented SystemVerilog scoreboards, monitors, and assertions, achieving functional and code coverage through constrained-random testing and assertion-based verification.
- Utilized Synopsys VCS and ModelSim to simulate and validate instruction execution and memory transactions (AXI, AHB).

**Customizable MCU Implementation on FPGA | Embedded Systems (Xilinx Vivado, Zynq FPGA, Embedded C)** **Jan 2023**

- Implemented a 4-stage pipeline MCU with a basic I/O functionality for synthesizing into RTL simulation utilizing Xilinx Vivado by adding performance branch detection and data hazard blocks to the design. Verified the design by interfacing VGA display and FPGA switches for I/O functions.
- Developed and compared software and hardware versions of the MCU, programming the soft-core processor on the Zynq FPGA and synthesizing the hardware version into configurable FPGA logic, analyzing runtime and resource usage performance.

## WORK EXPERIENCE

**Design Engineer at Bright Mind Enrichment** **Aug 2024–Present**

- Developing and maintaining front-end web applications to support digital system design, integrating interactive dashboards, and automation features to enhance usability, workflow efficiency, and collaboration for engineering teams.

**Design Verification Engineer Intern at Defense Research and Development Laboratory (DRDL), India** **Jan 2021–Jan 2022**

- Verified the digital designs of key components in the QR-SAM (Quick Response Surface-to-Air Missile) project, using SystemVerilog test benches to ensure data integrity, signal timing, and reliable communication between subsystems under various operating conditions. Focused on verifying protocol compliance across multiple operating conditions and resolving issues.
- Applied UVM methodology to develop reusable, scalable verification environments, improving test coverage and reducing verification time, while collaborating with design teams to troubleshoot critical issues and accelerate the design-to-verification cycle.

**Digital Design and Test Intern at Silicon Engineers, India** **Jan 2020–Dec 2020**

- Assisted in the design and implementation of automated test equipment (ATE) for PCB systems, using digital design techniques and Verilog HDL to enhance fault detection in high-reliability applications across various industries like Aerospace and Biomedical.
- Engaged in research focusing on hardware design using Verilog HDL to develop and optimize digital systems, while also providing mentorship for IoT and Arduino-based projects, thereby enhancing performance in embedded applications.