Summary:

Harshith Reddy Surakanti is a Hardware Design Engineer with over 3 years of experience specializing in FPGA/SoC architectures and RTL-to-GDSII ASIC design flow. He has hands-on expertise in RISC-V, MIPS, and ARM-based systems, with practical experience in subsystem design, integration, and custom IP development aimed at optimizing performance, power, and area (PPA). He has worked with Xilinx Zynq-7000 and MIPS, RISC-V, FPGA/SoC architectures and multiple on-chip and inter-chip serial communication protocols.

Name: Harshith Reddy Surakanti

Email: harshith.surakanti@gmail.com

Phone: --

Location: Dublin, CA

Country: USA

Position Category: Design: Logic design

Desired Job Role: Hardware Design Engineer

University: Purdue University Indianapolis

Degree: MS in Electrical and Computer Engineering (VLSI)

Graduation Year: 2024

Years Experience: 3

Notable Companies: Integrated Test Range, DRDO, NTT Data GDS

Top Skills: Verilog, SystemVerilog, TCL, Python, SQL, Cadence tools, OrCAD, Allegro, virtuoso, Innovus, Altium, Xilinx ISE, Modelsim, Simulink, TCAD

Job Intention: full-time

Visa Status: --

Able: no

Subject: Application for Job opportunities at Ahead Computing

Date Sent: 04-08-2025

Resume: Yes