NICTE-HA REYES

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SUMMARY

Accomplished Physical Design Engineer with a master's degree and over 9 years of experience in pioneering technology projects, including 3D XPoint Intel memories, Cryogenic Quantum Computing Control, Meta's micro-LED backplane, and PCIe Gen 5 modules. Expertise in ASIC design, clock tree implementation, and verification methodologies, with a comprehensive understanding of the RTL-to-GDS flow from synthesis to tape-out. Proficient in STA, including developing timing constraints and executing top/blocks level timing ECOs for closure. Skilled in the Synopsys suite and experienced with technology nodes ranging from 180nm to 3nm across various foundries. Proven track of record leading multidisciplinary, multicultural teams, adept at presenting results to clients with exceptional organizational, communication, and presentation skills. Passionate about applied technology and committed to driving innovation.

EXPERIENCE

Sr. Staff SOC Engineer

Synopsys Inc. Mexico • March 2021 -Present

- Physical Design owner for digital top for micro-LED backplane IC for international company in collaboration with analog team.
- Clock tree optimization and custom clock tree strategies to meet high performance spec, audit Reliability, deliver timing ECO implementations and Physical verifications to tape out.
- STA and timing ECO closure for full chip and PCIe gen5 subsystems and partition level blocks.
- Physical design lead for Memory management controller (MMC) subsystem. Coordinate, mentor and supervise Physical Design team with responsibilities of top-level integration.
- Report milestone status, achievement, and audit to customer management team.
- Mentor junior engineers on technical and soft skills.

SoC Desing Engineer

Intel Labs. Mexico • Oct 2019 -March 2021

- Development of Integrated SRAM, memory controllers, clock distribution blocks, integrated voltage regulator and IO cells using Synopsys tool for RTL2GDS flow with 22nm and 7nm Intel Technology.
- Block owner responsible for Synthesis, floorplan, and placement definitions for digital and mix signal blocks with cryogenic temperature specification as low as 4 K for Cryogenic Quantum Computing control chip.
- Timing constraints definitions, including IO budgeting for partitions, synchronous and asynchronous paths, Clocking & Clock domain crossing.
- Reliability and timing ECO implementations, Physical verifications reviews and fixes including IO cells definitions.
- Manage IP libraries to enable physical/design views from RTL2GDSII flow.

EDUCATION

- **M.S Integrated Circuit design.**

(INAOE), Puebla-Mexico.

Research Topic: *Characterization of a selection metric for optimization of digital circuits robust to process variations.*

- **Electronic Engineer**.

ITM Morelia Mexico

HOBBIES

- Trail Running
- Hiking
- Traveling

LANGUAGE:

English: Advanced
Spanish: Native Speaker

Physical Design Engineer

Intel Company. Mexico • Nov 2015 -Oct 2019

- Synthesis and APR flow on mixed signals blocks for silicon product design team. Development of memory controllers (DIMMS) and clock generation unit using 14nm and 10nm intel technology using Synopsys tools.
- Static Timing Analysis (STA), functional ECO implementations and signoff checks like antenna, EMIR, Xtalk and noise.
- Lead for physical design activities for stepping project using ECO metal only fixes and spare devices to implement complex logic ECOs to achieve Production Release Qualification (PRQ) one year ahead of schedule.
- Development plan for new hires and methodologies documentation.

IC Analog Design Engineer

Freescale Semiconductor. Mexico • Jan 2015 -Nov 2015

- Layout analysis, debug and verifications on analog cells using 16nm FinFET TSMC technology, for different types of topologies like decoder, Op-amp and bias cells with targeting area and power.
- Testbench creation, Analysis, and layout fixes of LVS, Design Rules Check, Manufactory Rules Check, Smoke alarm, electromigration, IRdrop and self-heating evaluations.
- Manual Routing power supply optimization for top analog blocks.
- Generation of LEF, CDL and LIB files for Physical Integration level and timing closure.

TOOLS

Synopsys suite

DC - ICC - ICC II - Fusion Compiler

Primer Time - Prime closure - tweaker – StarRC - Redhawk - IC Validator

Cadence suite

Innovus - Calibre

Scripting

TCL – SHELL

PUBLICATIONS

Circuit Performance Optimization for Local Intra-die Process Variations using a Gate Selection Metric. The 23rd IFIP/IEEE International Conference on VLSI-SoC 2015.