JUJHAR SINGH

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OBJECTIVE

Looking for Digital Design Engineer position that utilizes 15+ years of experience in full chip design flow from RTL, Synthesis, Physical Design, STA and Silicon Debug.

EDUCATION

MS-Electrical Engineering(VLSI), University of Southern California, LA,USA — Dec 2009
Advance Diploma in VLSI Design , Semiconductor Laboratory, Dept. Of Space, Chd, India — July 2007
BS- Electronics & Communication Engineering,Punjab University, Chd,India — June 2006

RELATED COURSEWORK

Computer System Organization	CAD of Digital Systems	Asynchronous Design	VLSI Architecture & Algorithm
System Design Using Microprocesso	VLSI System Design-A,B	MOS VLSI Circuit Design	VLSI Testing

TECHNICAL SKILLS

Processor: ARM Cortex M0+, PIC16/18, AVR & 8085
Programming Languages: Verilog, C, C++, Perl, TCL, Assembly Language
Tools: Xilinx ISE, Chip Scope, Questasim, ePD, HSPICE, Virtuoso, Primetime, Design Compiler, ICC, Redhawk, CCK, GIT
Bus Protocols: APB, SPI, UART, I2C

WORK EXPIERIENCE

Microchip Technology, Chandler,AZ –Principal Design Engineer — Oct 2010-March 2025

- Successfuly tapped out 20+ 8 bit PIC & AVR microcontroller by working on complete design cycle from RTL to GDS.
- RTL design of new macros interfaced with APB bus to go on first 32 bit Cortex M0+ chip of my division.
- RTL macro design of multiple macros including nvm, adc, comparator, dac and ram controllers on 8 bit CPUs.
- Chip level rtl connections.
- RTL speed edits to make macro run on faster frequency.
- Interfacing macros with APB, PIC and AVR buses.
- Lead for RTL, Synthesis, STA, APR, Floorlanning & power integrity.
- Schematic design of clock generators, clock switch, oneshots etc.
- Ported hard macros from one process to another.
- Worked on standard cell library development & characterization.
- Developing full chip spice simulation strategy for newly acquired AVR chips.
- Worked on the entire APR flow including floorplanning, placement, CTS and routing using ICC. Also, successfully did various functional and timing ECO's on PIC/AVR families.
- Introduced FPGA for first time in my division for macro development and precise timing control for silicon debug.
- Responsible for closing various checks including RTL lint checker, Formal verification, Power analysis and ATPG simulations
- Writing and maintaining scripts with Makefile, Perl and Tcl to automate workflows for various parts of the design.
- Created functional patterns and debugged them on J750 Tester.
- FIB and Microprobed chips to debug silicon issues.

Quantum Dimension, Huntington Beach- Part Time FPGA Engineer — June 2010-Oct 2010
SoC Microblaze RTL code development & Firmware for software defined radio on Xilinx Spartan 3 FPGA.

Motion Technologies, Burbank- Part Time Firmware Engineer — Aug 2010-Sept 2010
C programming of PIC16F819/ 690, VB GUI development & Circuit Design.

Laboratory of Neural Circuits & Plasticity (LNCP), USC – Student Engineer — April 2010-May 2010
Labview VI for random waveform generator

Topanga Technologies, Canoga Park- Intern Engineer — Aug-Dec 2009, Feb-April 2010
Firmware development, Labview GUI development for life cycle testing.

Department of Electrical Engineering, USC - Course Assistant — Spring 2009

- Providing assignment solutions and grading submitted assignments for EE680 CAD of Digital Systems.

Reliance Infocomm, India - Summer Intern — May-July 2005

- Designed LFSR and implemented on Spartan 3 FPGA. Analyzed GSM, CDMA and WLL systems.

Semiconductor Laboratory, India – Summer Intern June-July 2004

- Studied IC packaging and VLSI assembly operations.

ACADEMIC PROJECTS

DDR2 Controller

- Implemented DDR2 memory controller in Verilog and performed pre and post synthesis simulation**.** Verified using Denali DDR2 model.

SRAM Design

- Schematic and Layout of 1.28KB SRAM using cadence along with dummy decoder for PVT variations.

Direct Digital Synthesizer

- Designed a sine wave generator using SRAM, phase accumulator and DAC.

Viterbi Decoder for Wireless 3G Mobile Phones

- Implementation sequential viterbi decoder using RTL Verilog .Synthesized using design compiler.

Asynchronous Crossbar Interconnect

- PCHB based delay insensitive 4x4 asynchronous crossbar using Verilog CSP. Extended design to 8x8 streaming interconnect.

Advanced Encryption Standard & RSA Cryptographic Algorithm

- Implemented AES algorithm and RSA algorithm based on Montgomery modular multiplication on virtex 4 FPGA. Funded by Dept. of IT, Govt. of India. Graded the top projects in 7^{th} and 8^{th} semester senior year project.

Bitonic Sort Network

- Developed bitonic sort network configurable for various sizes on Virtex 4 FPGA.

Neural Network

- Optimized schematic and layout of neural network w.r.t size and clock period.

Image analysis

- Image acquisition, analysis using labview machine vision toolkit. Stimulus generation using NI PCI 6722 in a closed loop.

Microprocessor 8085 Simulator

- 8085 simulator developed in Visual Basic supports all the instructions including self modifying code. Top project in the Software Lab.

Troy Word Wide Processor

- Designed 4 stage pipeline processor. Multiplier designed using booth's algorithm and synthesized using design compiler.

Data Path and Control unit for single and multi cycle CPU

- Designed and functionally verified data path unit and control unit for single and multi cycle CPU using ePD.

Interfacing Flash memory, SRAM to 80486 Microprocessor

- Interfacing micron 4MB flash memory, SRAM along with I/O chip to 80486 Microprocessor using memory/ IO controller in ePD.

DMA & Bus Arbitration

- Performed DMA & bus arbitration in 8088 & 8086 processor systems.

HONORS/ AWARDS

1. Discretionary bonus for ADC design and debug using fpga based pattern generator.
2. Awarded plaque and discretionary bonus for suggesting innovative architectural improvement.
3. Selected to be part of new initiatives team for new process setup for apr,standard cells
4. Developed new approach for custom scan stitching script that interleaves flip flop and latches while minimizing length.
5. Reduced verification time by developing autobanking script that inserts correct bank in assembly files automatically.
6. Awarded top project in 8^{th} Semester for implementing AES & RSA algorithm on FPGA funded by dept of IT, govt of india.
7. Awarded top project in 6^{th} Semester for developing 8085 instruction simulator GUI in visual basic.