André Alberto Contreras Rivera

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Experience

CPU Design Verification Engineer — **Intel Corporation**, Zapopan, Mexico
January 2024 – Present

- Next generation CPU Core Pre-Silicon Verification:
  - Feature-based verification for Power Management & BIU x86 Architecture.
  - Developed feature checkers, coverage and directed/random stimuli.
  - Ownership of the triaging and debugging of regressions using a third-party triage tool.
  - Enhanced testbench and optimized code using user-defined macros for checkers and coverage.
  - Writing, Implementing and Executing test plans for PM features; including:
    - Frequency scaling external triggers.
    - Intelligently optimized dynamic power gating.
    - Context coherence mechanism for core sleep states.
    - Thermal sensor functionality and core thermal telemetry.

Functional Validation Intern — **Intel Corporation**, Zapopan, Mexico
March 2022 – March 2023

- Xeon Scalable Processor – Accelerator Engines Validation:
  - Functional Validation of Analytics, Storage, Network and Security engines.
  - Planning and design of test cases in Python for each accelerator engine.
  - Debug and triage regressions for each IP in Accelerators.

Education

Instituto Tecnológico y de Estudios Superiores de Monterrey — Zapopan, Mexico
Bachelor of Science Degree in Electric Technologies Engineering — 2018 – 2022

- Fully-developed and tested a single-cycle custom MIPS from scratch using SystemVerilog.
- Using a FPGA, designed and tested a custom-component of an Avalon Memory Map and programmed the embedded software of an Atari Pong.

Centro de Investigación y de Estudios Avanzados del IPN — Zapopan, Mexico
Diploma of Education in ASIC Design and Verification — March – October (2023)

- Convolution Co-processor Design in SystemVerilog applying a standard SoC design methodology.
- Fully-developed a DV plan and verification environment from the ground up using UVM for a SRAM on SkyWater 130nm; additionally functional coverage and SVA were implemented.

Skills

- **Programming Languages:** Python, C/C++, Java, Bash and TCL/Pearl.
- **Hardware Description Languages:** SystemVerilog and Universal Verification Methodology (UVM).
- **EDA Tools:** DVT Eclipse IDE, Cadence Xcelium, Cadence VManager, Synopsys VCS/Verdi.
- **Certifications:** Cadence SystemVerilog, Cadence UVM, Cadence SVA.
- **Operating Systems:** Windows and Linux/UNIX.
- **Languages:** Native Spanish and Fluent English.