Hi,

I'm a hands-on technical physical design lead working on Xeon Server SoC products at Intel. Been at Intel for the last ten years and worked on all phases of implementation from RTL synthesis to tapeout, and currently lead the power convergence for Xeon server SoCs. I drive RTL power estimation and help detect RTL power bugs early in the design cycle,and also own low power implementation methodology. Presently working on chips with the most advanced 18A process node at Intel, 3nm and 2nm process from TSMC. I work on multi-die packaging and design technology co-optimization with both internal and external foundries such as TSMC.

As a technical lead, I collaborate with EDA tool vendors such as Synopsys, Ansys, IP providers, as well as 3

rd

party ASIC design vendors.

I'm interested in the Physical Design positions in AheadComputing. My resume is attached.

Thanks,

Jyotirmoy Ghosh