Summary:

Nilesh Suryavanshi is a final-year MS Computer Engineering student at the University of Texas at Dallas with experience in RTL design and verification, focusing on CPU microarchitecture and performance optimization. He has developed a UVM-based testbench to verify RISC-V pipeline stages, implementing checks for hazards, forwarding, and branch prediction. He has hands-on experience with Verilog/SystemVerilog, Synopsys & Cadence tools, and static timing analysis (STA).

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Location: Austin, Texas, 78736

Country: USA

Position Category: Verification: Design verification

Desired Job Role: Silicon Verification Engineer

University: The University of Texas at Dallas, University Of Mumbai

Degree: Master of Science, Computer Engineering, Bachelor of Engineering, Instrumentation

Graduation Year: 2025

Years Experience: 3

Notable Companies: Bosch, Tata Consultancy Services Limited

Top Skills: Verilog, SystemVerilog, Python, C, C++, UVM, Static Timing Analysis, Synopsys, Cadence

Job Intention: Full-Time

Visa Status: --

Able: No

Subject: Interested to join Ahead Computing.

Date Sent: 03-18-2025

Resume: Yes