A thermomechanical analysis of the single chip hybrid module

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Outline

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- The setup
  - Methodology
  - Software
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  - Software limitations
- Result
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- Next steps
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  - Post-processing
- Conclusions

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Introduction

- Induced thermal stresses (thermal expansion, coupled components)
- Assess **single module's** resistance to the thermal cycle between RT and 213 K
- Compare results for different PCB thickness
- A document that discusses the project in full detail is being prepared

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Methodology

- Finite Element Analysis (FreeCAD+Gmsh+CalculiX)
- Looking for stress and strain plots at module's various layers
- Simulation was validated by comparing results with University of Glasgow's
  - https://indico.cern.ch/event/718423/contributions/3002908/attachments/1651899/2642467/FEA_simulations_of_thermal_induced_stresses_in_RD53.pdf (Liam Cunningham's presentation for a quad module)

Stresses at:	LBNL (measured in the center)	Glasgow (measured at the edges?)
PCB	75-130	85
Glue	28-70	48
Sensor	46-64	220
Bump bonds	39-53	53
RD53	50-66	70

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The Model (Setup)

- Homogeneous materials
  - In case of mixture, interpolation of thermal and mechanical properties (e.g. bump bonds and air)
- All relevant dimensions taken from mechanical design sketches
  - AT2-IP-EP-0009.v3 document (https://edms.cern.ch/ui/#!master/navigator/document?D:100324417:100324417:subDocs)

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The Model

- The Box Model
  - 6 boxes
  - Top to bottom: PCB (multiple layers of Copper, Kapton, or a mixture thereof), glue (Araldite), sensor (Silicon), bump bonds (20% silver-tin, 80% air), RD53 chip (Silicon) and **thermal gel** (SE4445)
  - Material properties were taken from Glasgow's presentation when available or MatWeb database otherwise

PCB layers

- PCB is divided in five layers
  - 3 insulating layers (kapton)
  - 2 conducting layers (copper and kapton)
- We want to observe how stress in the PCB responds to the thickness of the middle insulating layer
- Two models (Single Thin and Single Thick)

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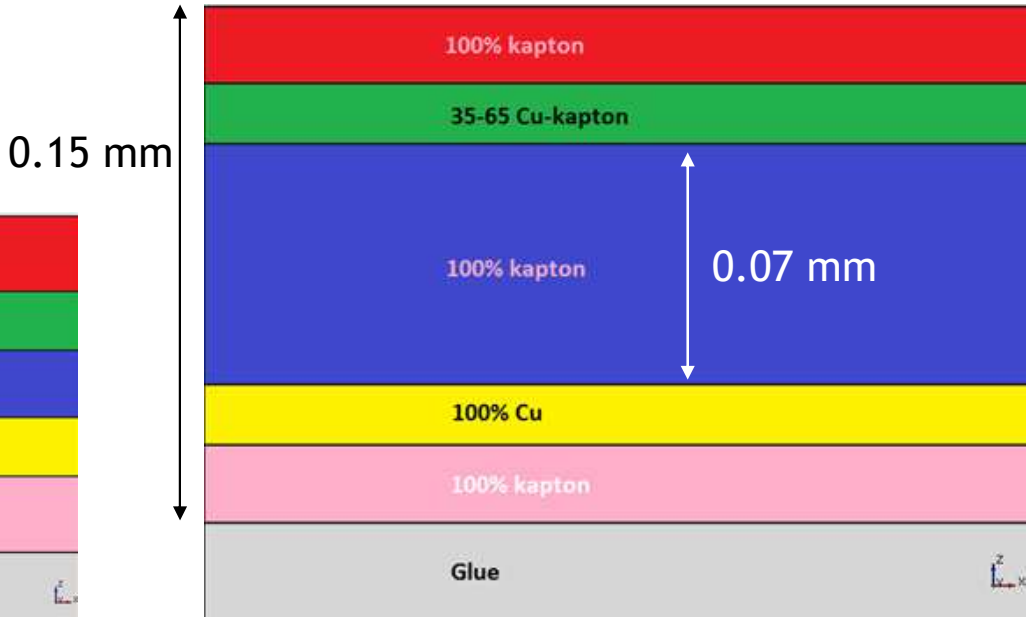
PCB Layers

Single Thin



Single Thick

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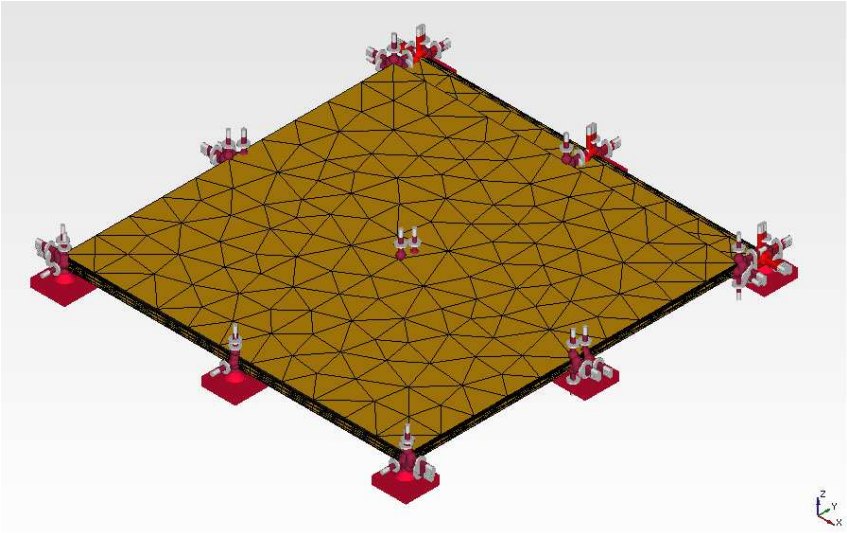
Simulation Constraints

- Ambient temperature going from 300 K to -213 K
- Mechanical constraint at thermal glue's bottom
- Heat flow allowed and taken into account
- 3D Mesh has maximum element size 2 mm



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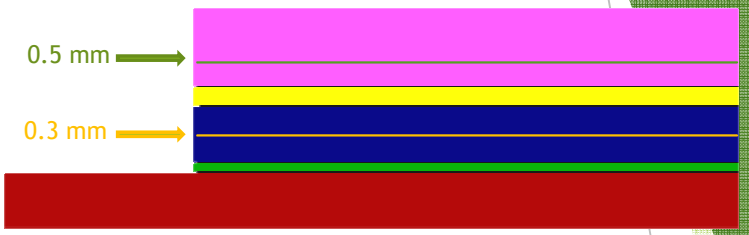
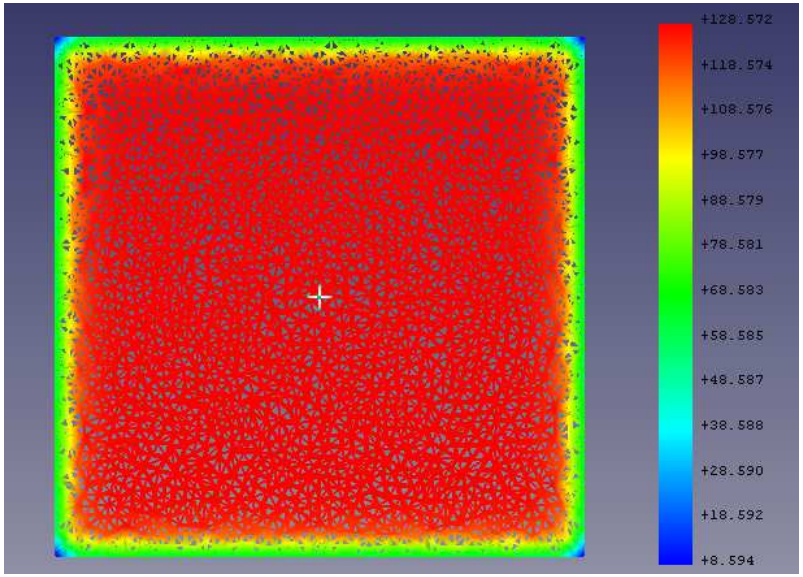
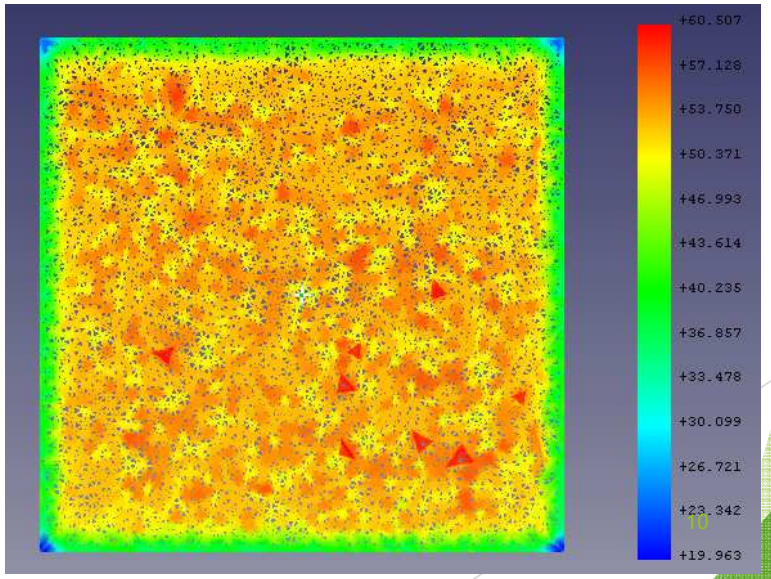
Quantitative challenges



- Limited post-processing options
- Huge fluctuation within each layer, even for high element density
- Cuts at heights of 0.5 mm on the left, 0.3 mm on the right (stress maps)





Quantitative challenges

- Fluctuations change values of maximum stress
- Results not symmetric about origin as expected
- Currently developing post-processing code (Python)
  - Creates a box around reference point (RP)
  - Averages all points around RP (in surrounding box) based on distance
  - Iterates for every point
  - Box is not allowed to cross material boundaries

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Stress and strain plots

- All plots were taken along a line in z going through the middle of the chip (10mm, 10mm, z), where 0 mm < z < 0.6 mm
- Plots were created with Paraview tool *Plot Along Line*
- Stress plots in blue, strain plots in orange
- Stress measured in MPa
- Height (z) on the x-axis
- Plots are to be updated after post-processing algorithm is applied

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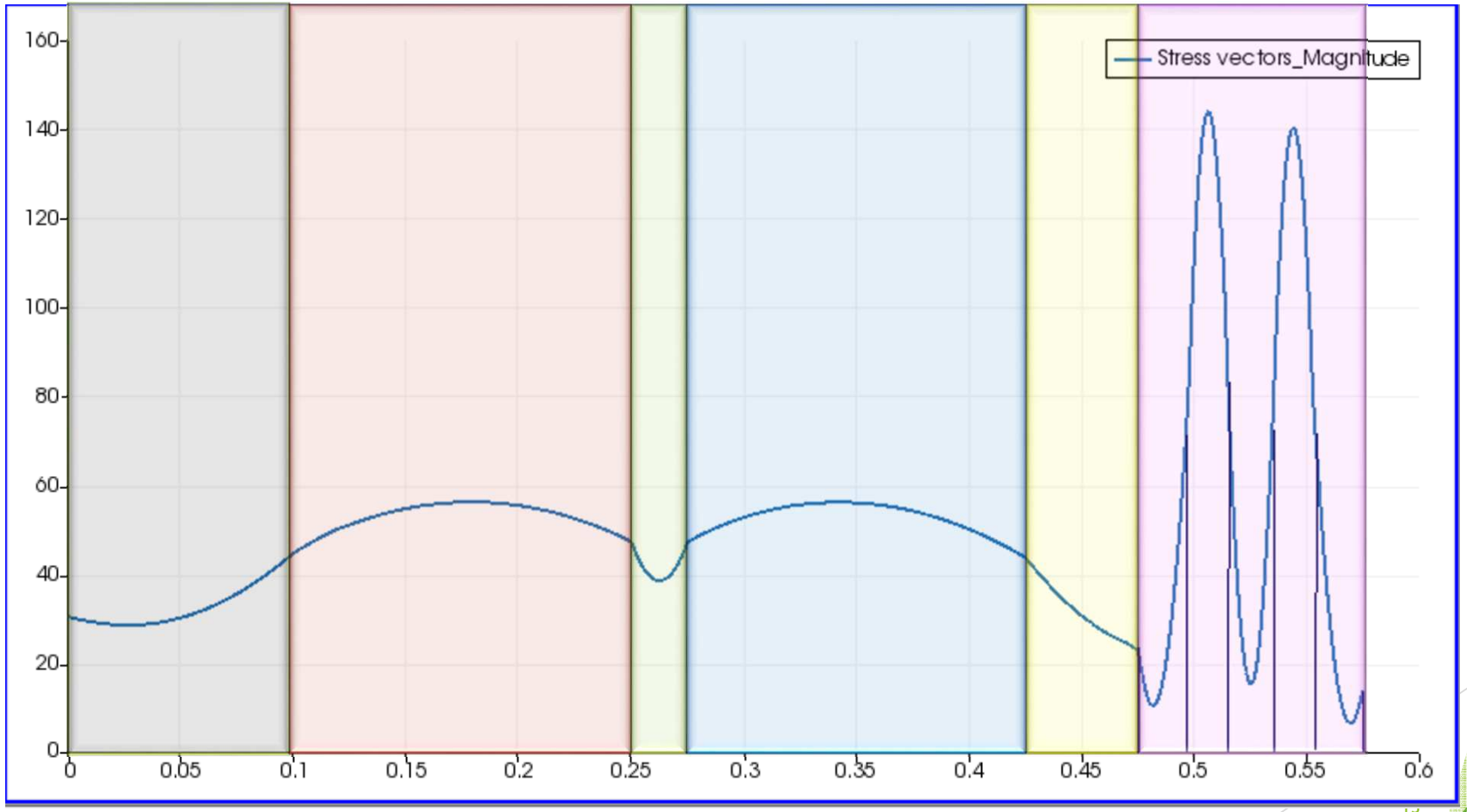
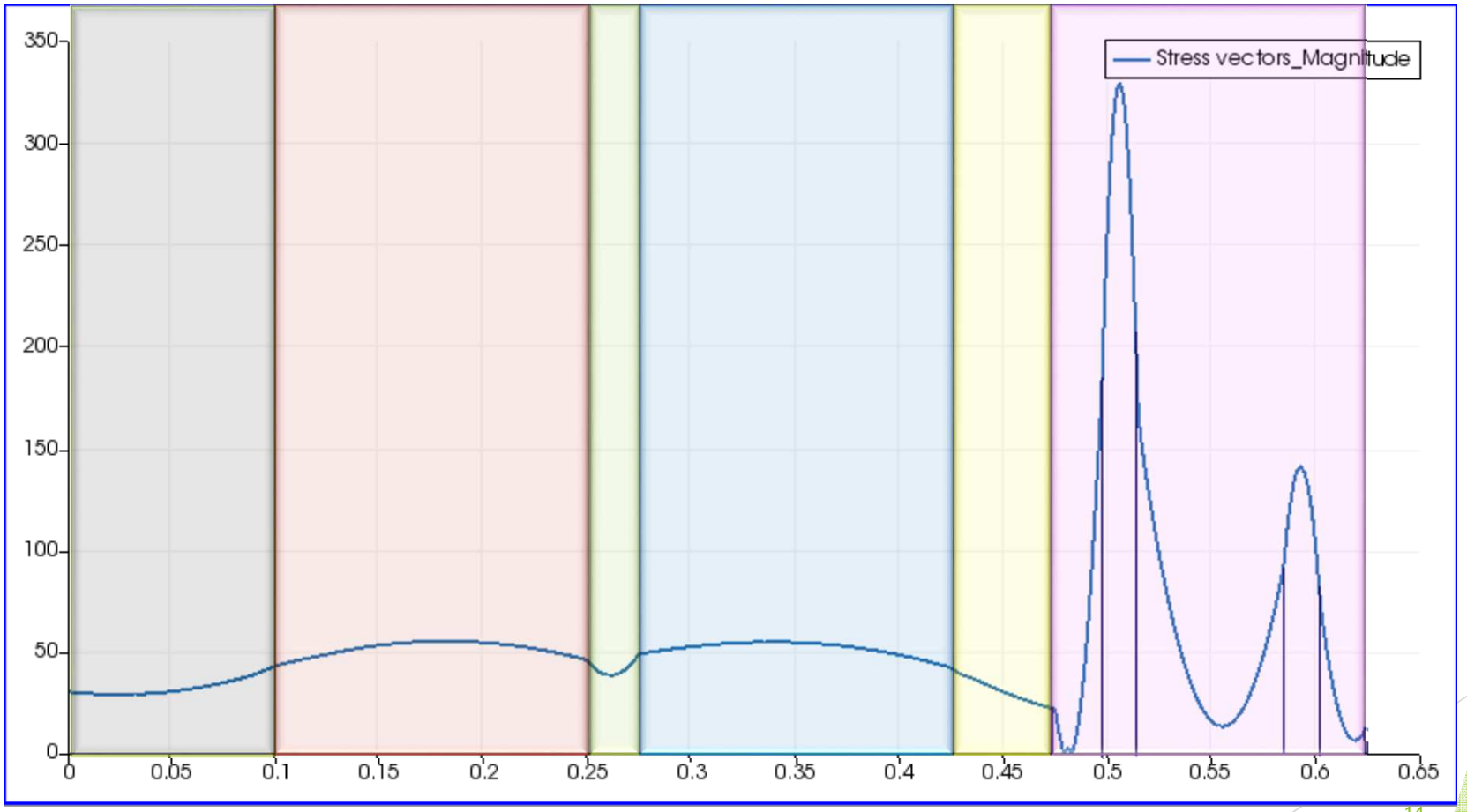
General results



Thermal glue
RD53
Bump bonds
Sensor
Glue
PCB

Single Thin - Stress (MPa) v height (mm)

General results



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PCB

Single Thick – Stress (MPa) v height (mm)

Stress plots (conclusion)

- Single Thin:
  - Maximum stress of ~145 MPa at copper and Cu-kapton layers (PCB)
  - About 69% of copper UTS
- Single Thick
  - Maximum stress of ~330 MPa at pure copper layer (PCB)
  - About 157% of copper UTS
- Stress in the bump bonds does not change with the thickness of the dielectric between copper layers

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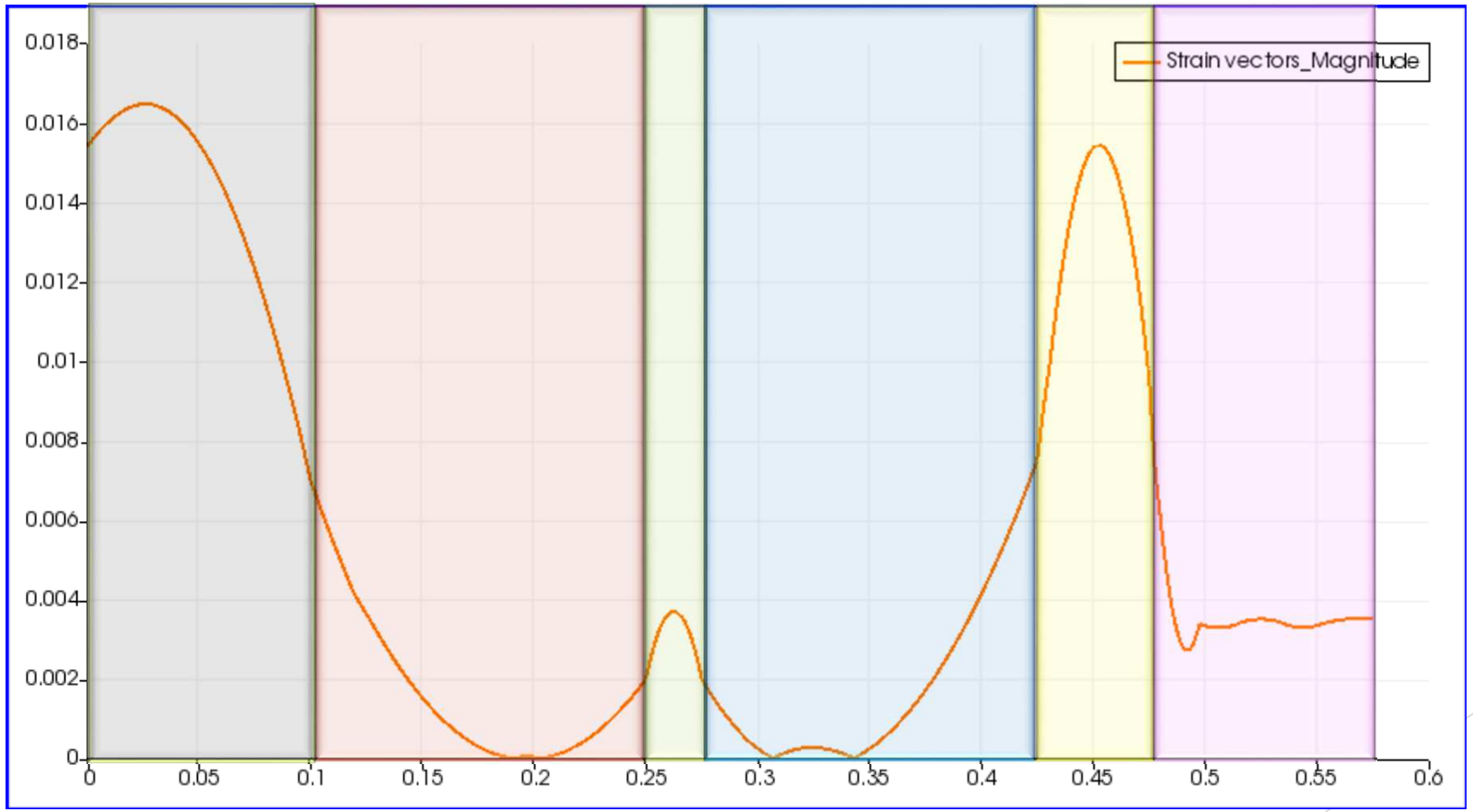
General results



Thermal glue
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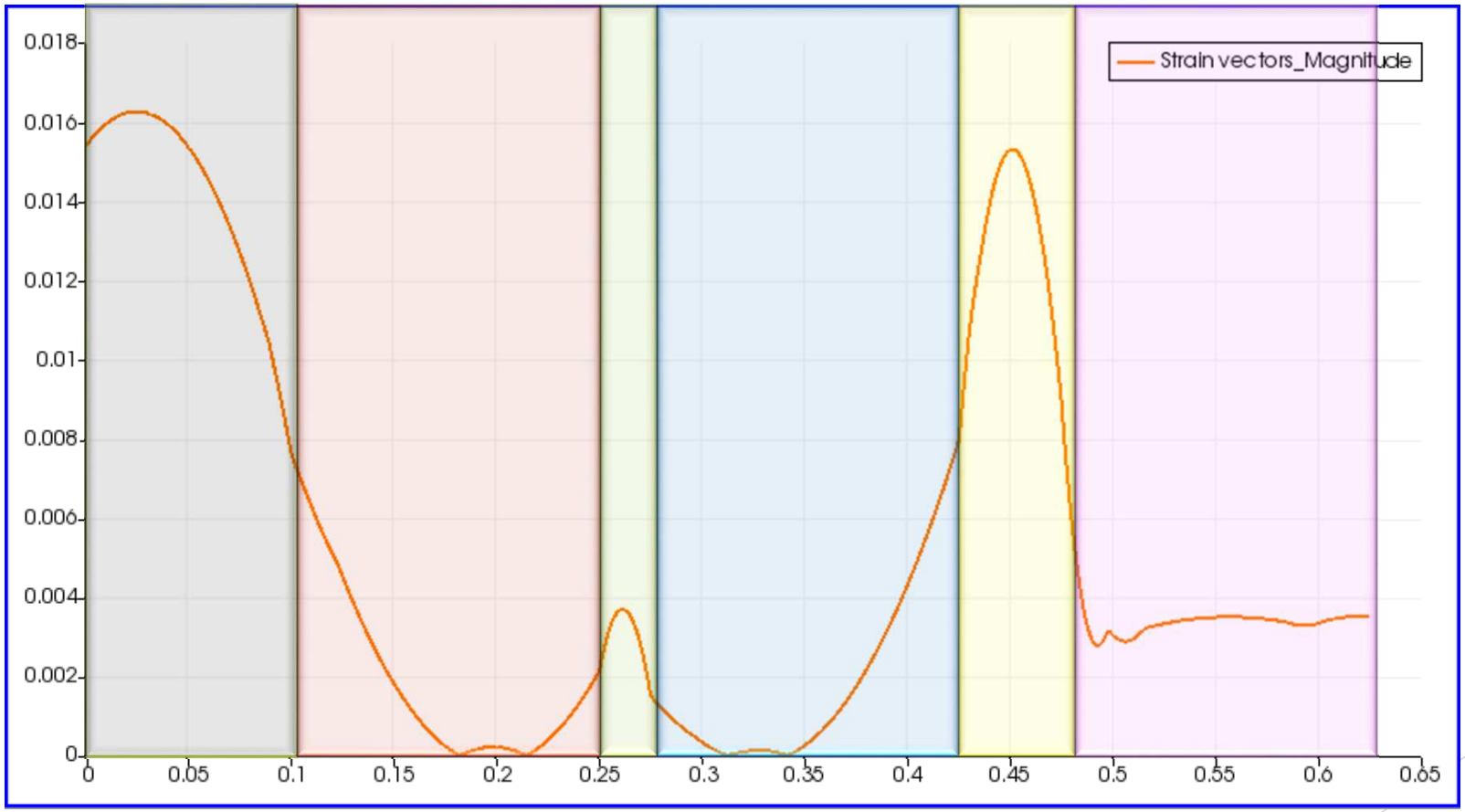
Single Thin - Strain v height (mm)

General results



Thermal glue
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PCB

Single Thick – Strain v height (mm)

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Strain plots (conclusion)

- Strain profiles were nearly identical for the two models
- Maximum strain of around 1.6% at both glue layers

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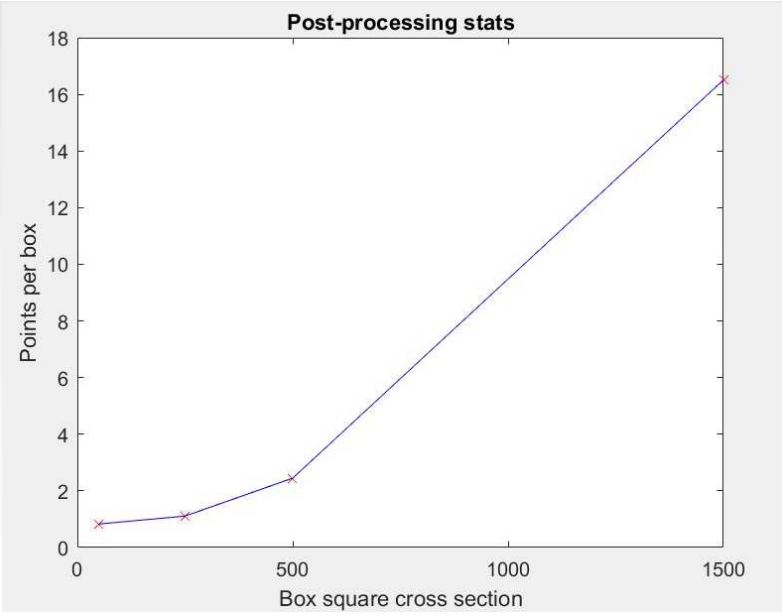
Post-processing

- Algorithm averages several points in order to minimize fluctuations
- We plan to set the box size between 1000 and 1500 microns, so that there are enough points per box and running time is not unnecessarily long



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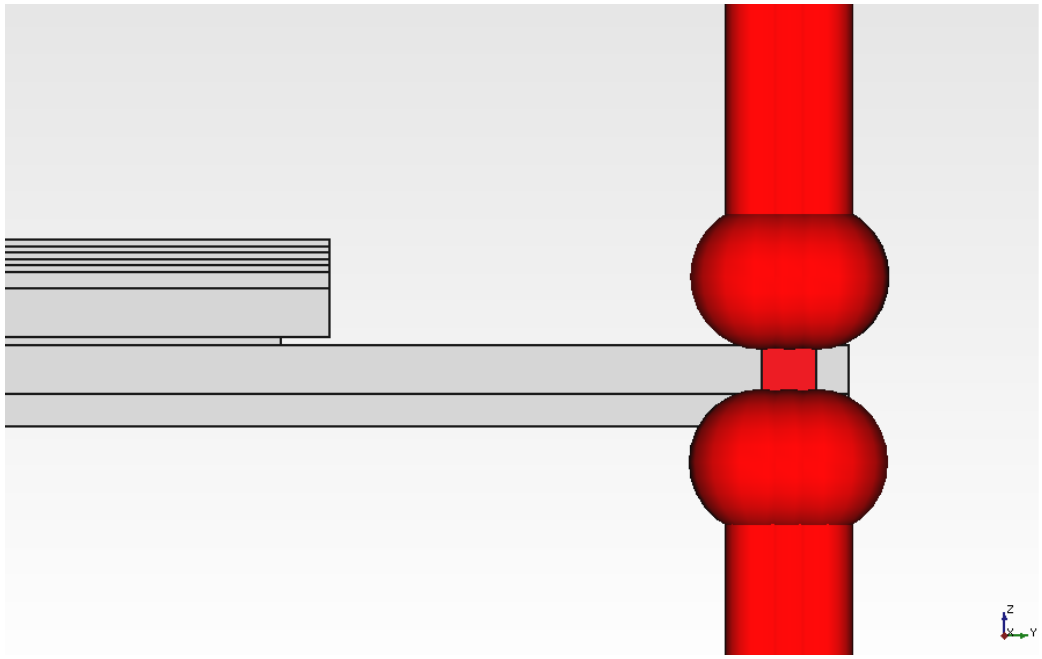
Heat source

- Next step: introduce a heat source in RD53 (Joule heating of 4W on edge)
- Use FreeCAD Heat Flux constraint in FEM Workbench



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Conclusion

- The simulations were produced consistent results when compared with previous quad simulations
- The softwares used are powerful tools, but they have noticeable limitations
- Stress concentrates at copper conducting layers within PCB
- Making the middle dielectric layer wider raises stresses
- Kapton was the only dielectric used, but it is not the only option
- Stress in the bump bonds remained the same regardless of the thickness of kapton between two copper layers in the PCB

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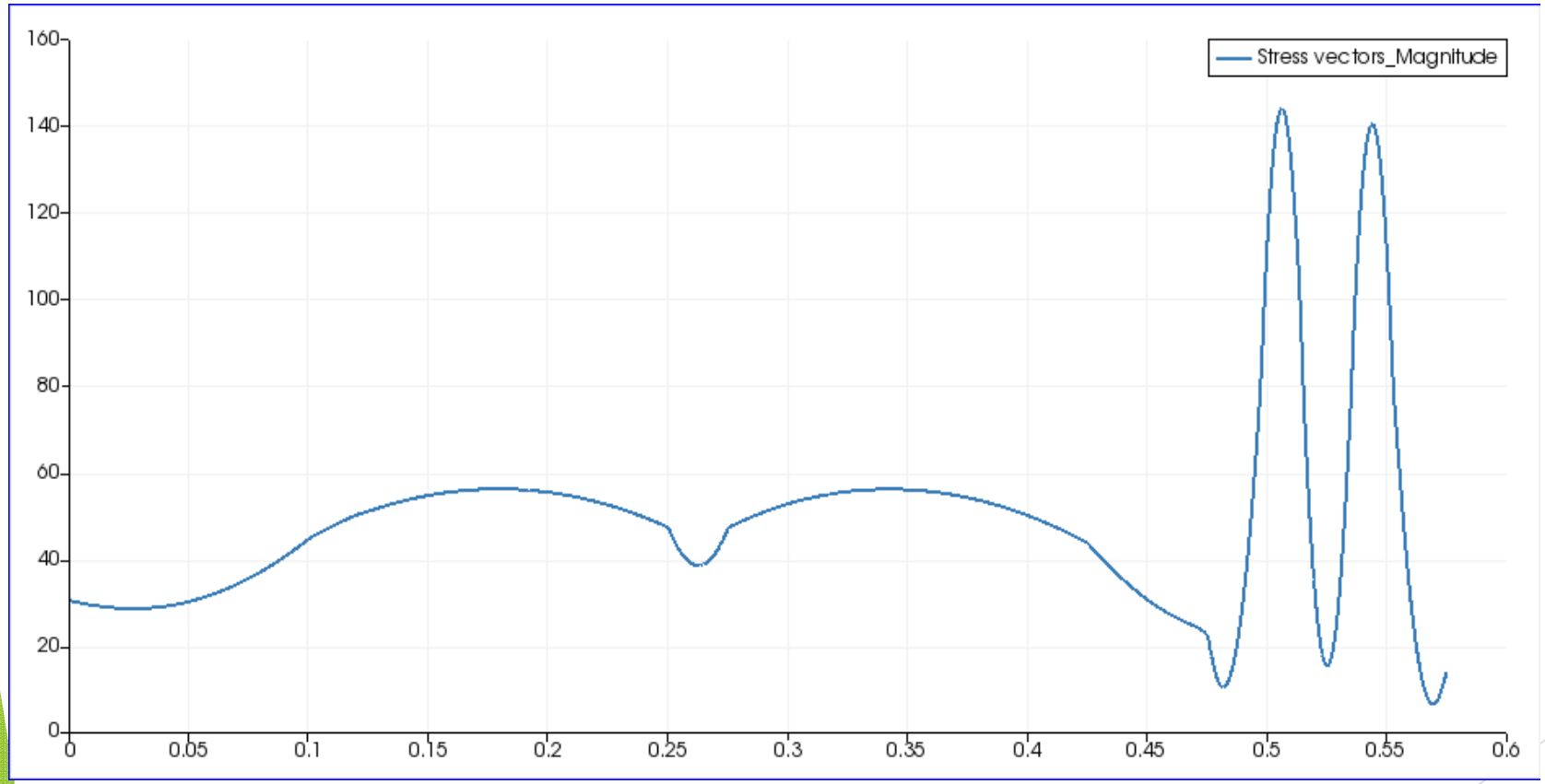
Cross-checking (extra)



Single Cross-Check – Stress (MPa) v height (mm)

Thermal glue
RD53
Bump bonds
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