CprE 381 – Computer Organization and Assembly-Level Programming

Lab-03 Report

Student Name Brandon Cortez

Section / Lab Time 8 / W 9:55-11:45

Submit a typeset pdf version of this on Canvas by the due date (i.e., the start of your next lab section). Refer to the highlighted language in the Lab-03 instructions for the context of the following questions.

a. [Prelab] At the end of Chapter 5, answer question 5. At the end of Chapter 7, answer exercise 2.

i. 5.5

```
1  library IEEE;
2  use IEEE.STD.LOGIC.1164.ALL;
3  entity 8_or is
4    Port (i_A : std_logic;
5          i_B : std_logic;
6          i_C : std_logic;
7          i_D : std_logic;
8          i_E : std_logic;
9          i_F : std_logic;
10         i_G : std_logic;
11         i_H : std_logic;
12         o_F : std_logic);
13 end 8_or;
14 architecture Behavioural of 8_or is
15 begin
16   proc1: process (i_A, i_B, i_C, i_D, i_E, i_F, i_G, i_H)
17     begin
18       o_F <= (i_A or i_B or i_C or i_D or i_E or i_F or i_G or i_H);
19     end process proc1;
20 end Behavioural;
```

ii. 7.2

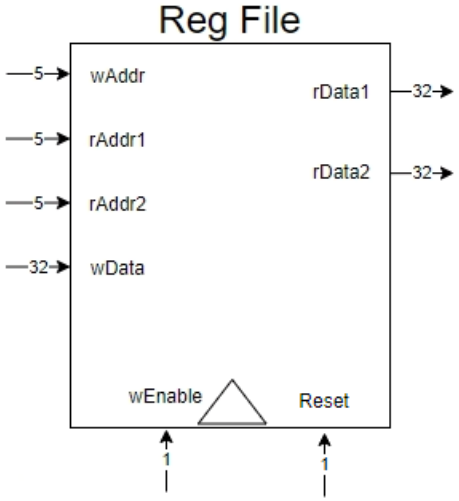
```
1  library IEEE;
2  use IEEE.STD.LOGIC.1164.ALL;
3  entity flip_flop is
4    Port (D : in std_logic;
5          S : in std_logic;
6          R : in std_logic;
7          CLK : in std_logic;
8          Q : out std_logic;
9          QB : out std_logic);
10 end flip_flop;
11 architecture Behavioural of flip_flop is
12 begin
13   proc2: process (CLIK, S, R)
14     begin
15       if S = '0' then
16         Q <= '1';
17       elseif R = '0' then
18         Q <= '0';
19       elseif CLK'event and CLK = '1' then
20         Q <= D;
21         QB <= not Q;
22       end if;
23     end process proc2;
24 end Behavioural;
```

b. [Prelab, contract due at Lab-03 deadline] Project team assignment and completed contract.

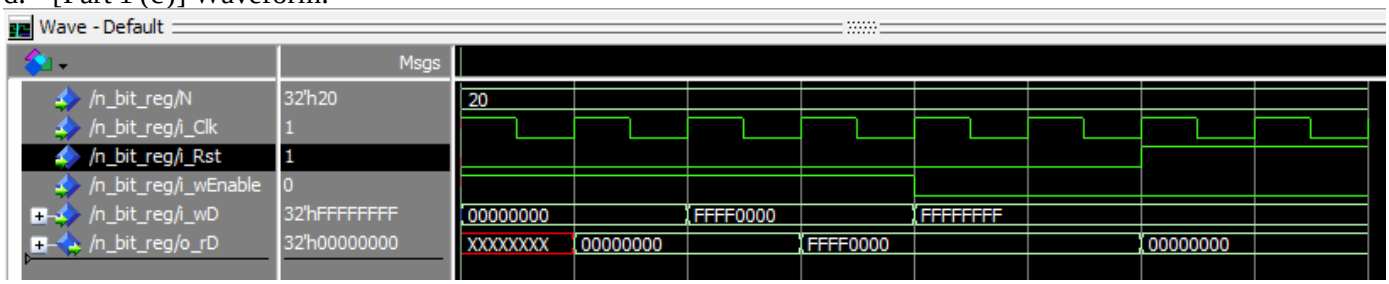
   i. Included in submission

c. [Part 1 (a)] Draw the interface description for the MIPS register file. Which ports do you think are necessary, and how wide (in bits) do they need to be?

   i.



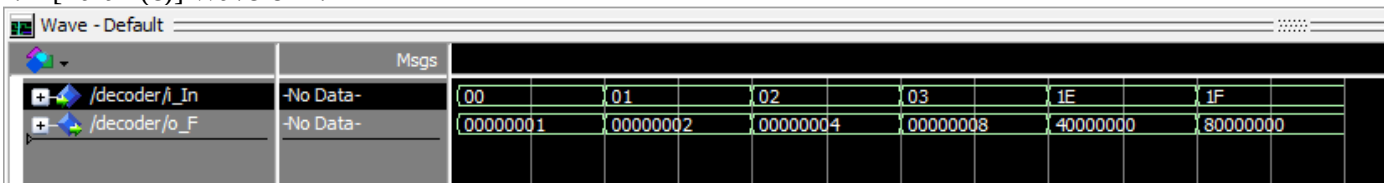
d. [Part 1 (c)] Waveform.



e. [Part 1 (d)] What type of decoder would be required by the MIPS register file and why?

   i. The decoder would require a 5:32 decoder to go from the 5 bit inputs to the 32 bit outputs in the register file.

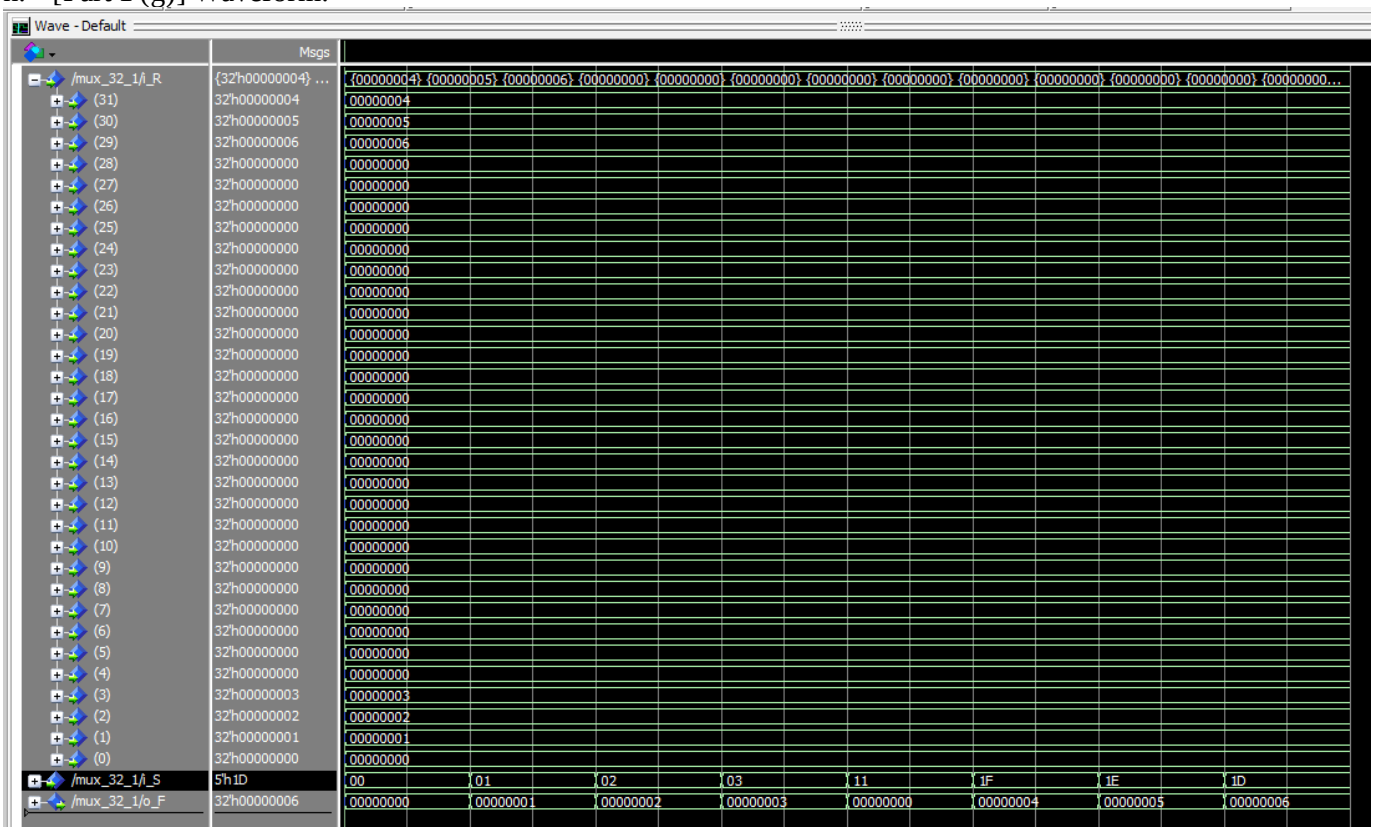
f. [Part 1 (e)] Waveform.



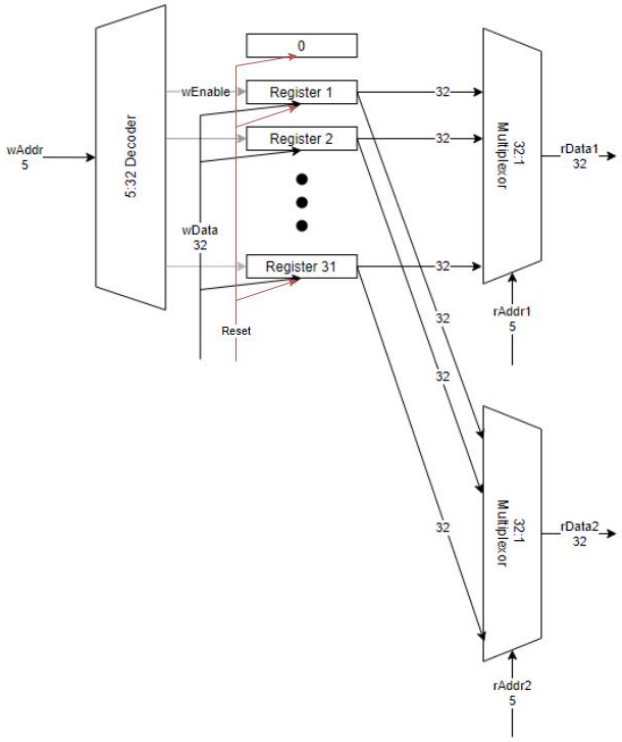
g. [Part 1 (f)] In your write-up, describe and defend the design you intend on implementing for the next part.

   i. I believe I can efficiently create the 32 bit 32 to 1 Mux by modifying the decoder code that I just created in conjunction with the Mux examples from the Free Range text to build a 32:1 Mux using the same when / else statements as before.

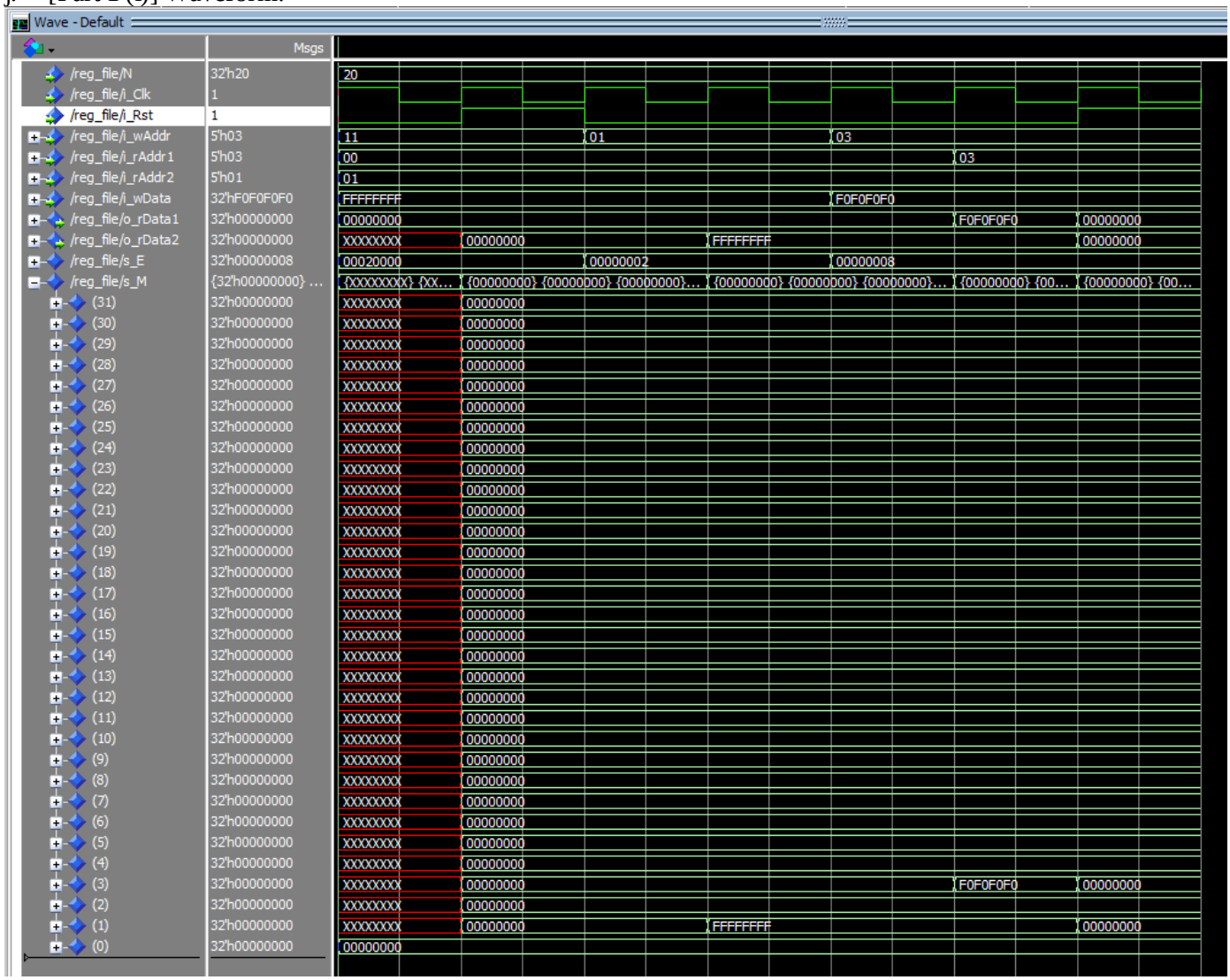
h. [Part 1 (g)] Waveform.



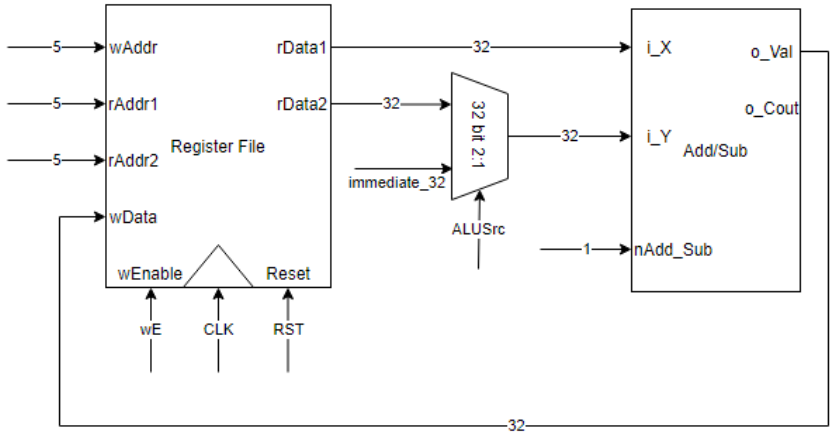
i. [Part 1 (h)] Draw a (simplified) schematic for the MIPS register file, using the same top-level interface ports as in your solution for part a), and using only the VHDL components you have created in parts (b), (e), and (g).



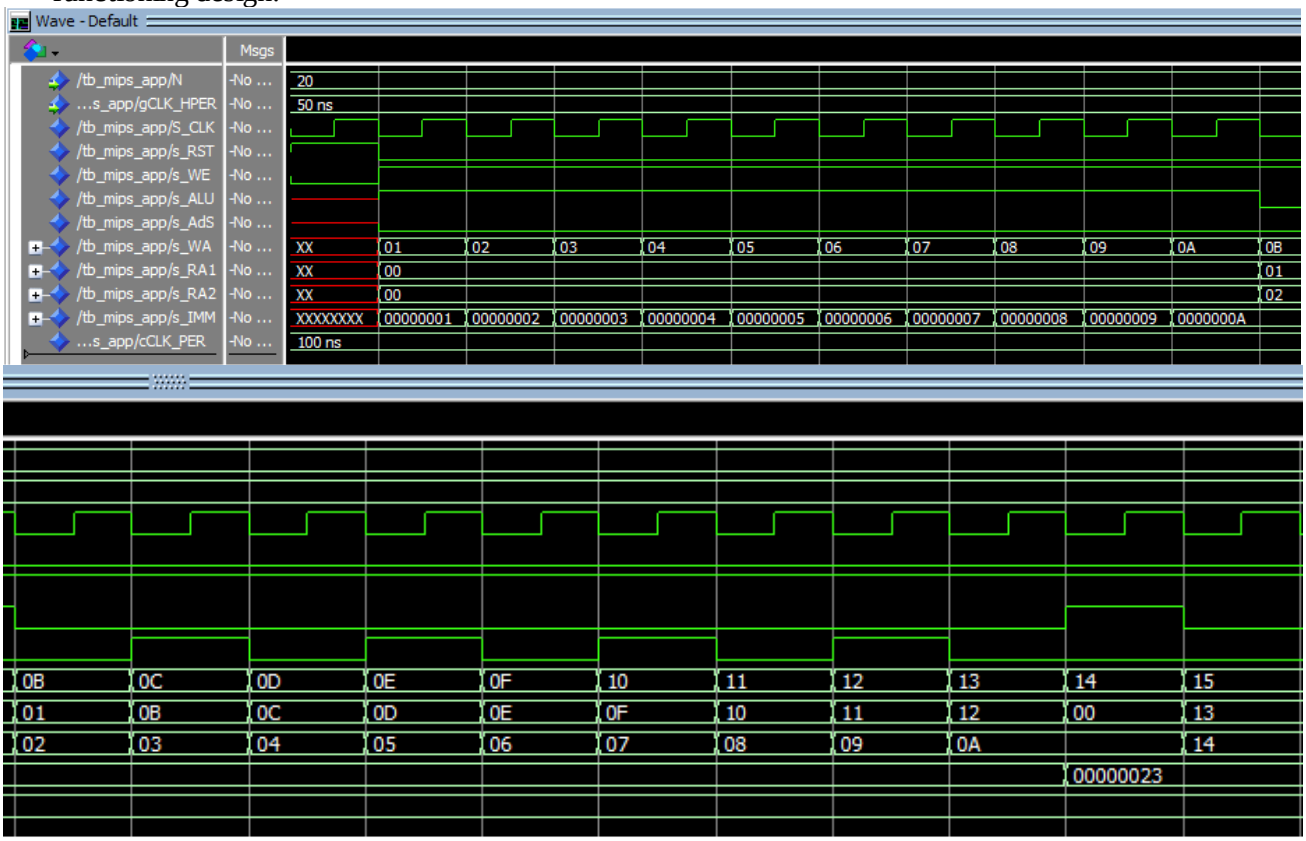
j. [Part 1 (i)] Waveform.



k. [Part 2 (b)] Draw a schematic of the simplified MIPS processor datapath consisting only of the component described in part (a) and the register file from problem (1).



l. [Part 2 (c)] Include in your report waveform screenshots that demonstrate your properly functioning design.



m. [Feedback] You must complete this section for your lab to be graded. Write down the first response you think of; I expect it to take roughly 5 minutes (do not take more than 10 minutes).

i. How many hours did you spend on this lab?

Task	During lab time	Outside of lab time
Reading lab	.5	1
Pencil/paper design	0	0
VHDL design	1	4
Assembly coding	0	
Simulation	.25	1
Debugging	.25	2
Report writing	0	1
Other:	0	0
Total	2	9

ii. If you could change one thing about the lab experience, what would it be? Why?

i. If I could change one thing I would give a little more guidance when it comes to why we are doing what we are doing when putting together components into a complex structure. I spent an hour on part 2 before realizing I was doing it backwards.

iii. What was the most interesting part of the lab?
    i. The most interesting part of the lab for me was seeing how we could make components that were seemingly unrelated and combine them to make something useful.