CprE 381 – Computer Organization and Assembly-Level Programming

Lab-02 Report

Student Name Brandon Cortez

Section / Lab Time 8 / W:9:55-11:45

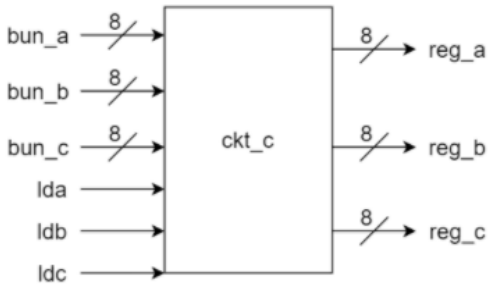
Submit a typeset pdf version of this on Canvas by the due date (i.e., the start of your next lab section). Refer to the highlighted language in the Lab-02 instructions for the context of the following questions.

a. [Prelab] At the end of Chapter 3, answer questions 4b), 5a), and 6.

4.b)

```
entity sys2 is
port (
        input.w         : in    std_logic;
        clk             : in    std_logic;
        a_data          : in    std_logic_vector(0 to 7);
        b_data          : in    std_logic_vector(0 to 7);
        dat_4           : out   std_logic_vector(7 downto 0);
        dat_5           : out   std_logic_vector(7 downto 0));
end sys2;
```

5.a)



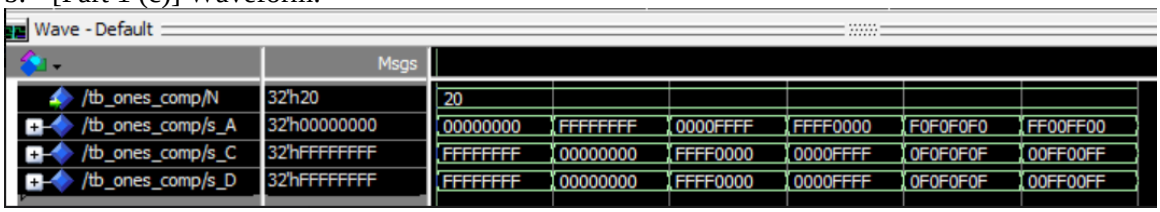
6.a)

The CLK : in std_logic statement is missing the semi colon at the end

6.b)

The closing parenthesis of the port section is missing. The end of byte_out should look like "...down to 0));"

b. [Part 1 (c)] Waveform.



This this the wave form of the one's complimenter taking the one's compliment of the input.

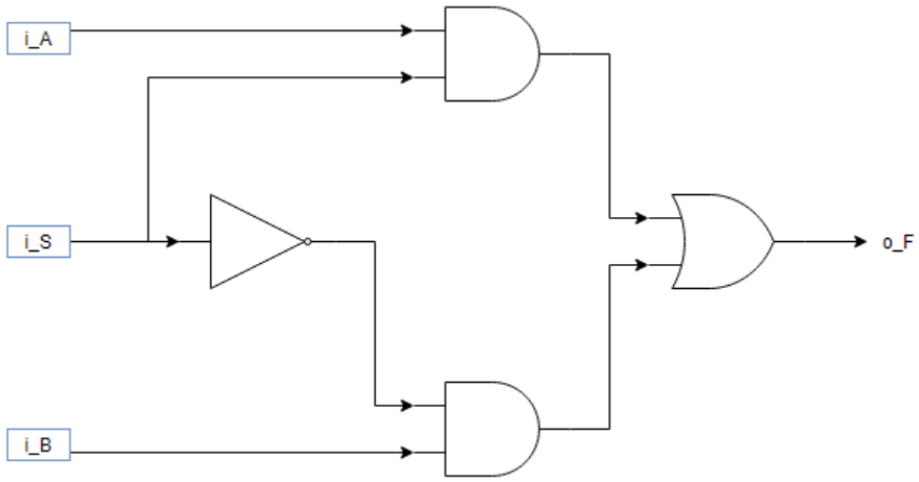
c. [Part 2 (a)] Draw the truth table, Boolean equation, and Boolean circuit equivalent (using only two-input gates) that implements a 2:1 mux.

Truth Table:

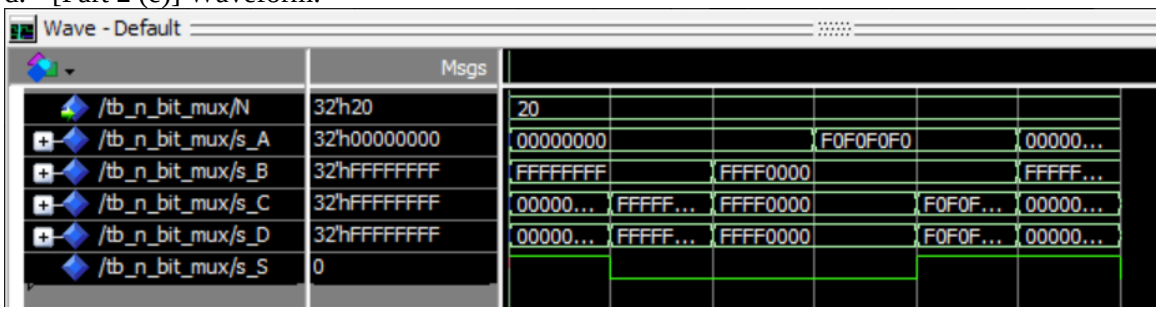
i_S	i_A	i_B	o_F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Boolean Expression:

o_F = (i_A * i_S) + (i_B * ~i_S)



d. [Part 2 (e)] Waveform.



This is the wave form showing that both the structural and dataflow multiplexers have the same behavior.

e. [Part 3 (a)] Draw the truth table, Boolean equation, and Boolean circuit equivalent (using only two-input gates) that implements a full adder.

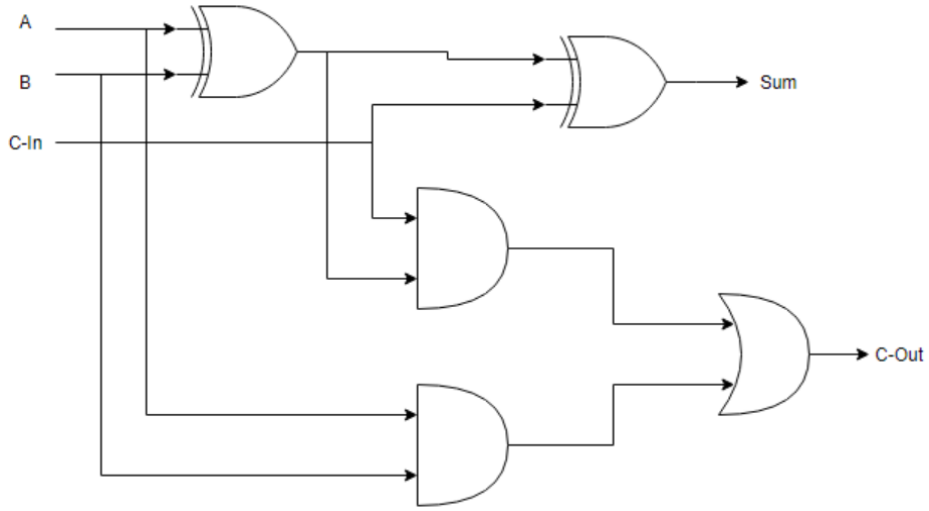
Truth Table:

Inputs			Outputs	
A	**B**	**C-In**	**Sum**	**C-Out**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

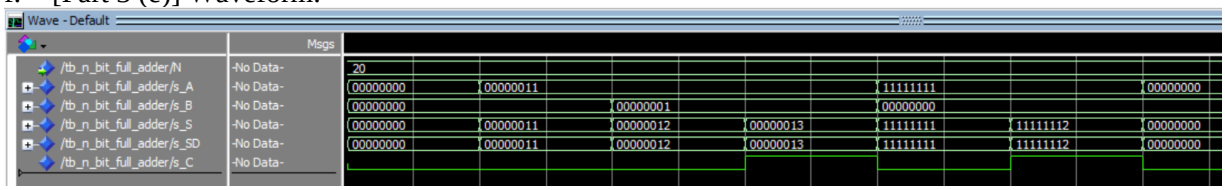
Boolean Expression:

Sum = A XOR B XOR C-In

C-Out = (A AND B) Or (A XOR B)

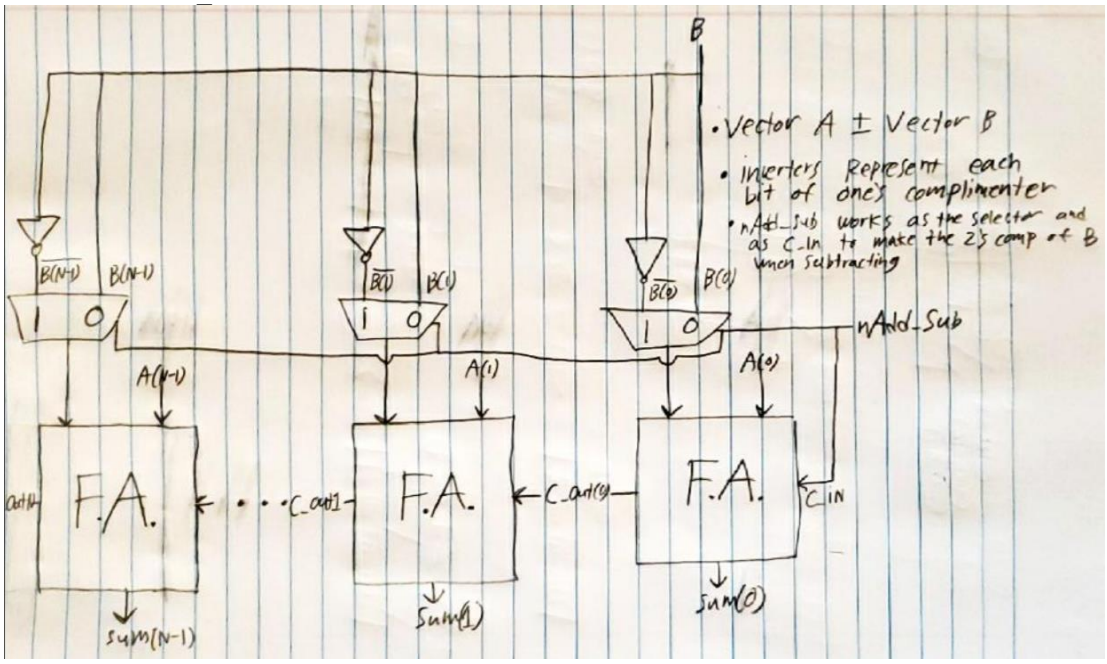


f. [Part 3 (e)] Waveform.



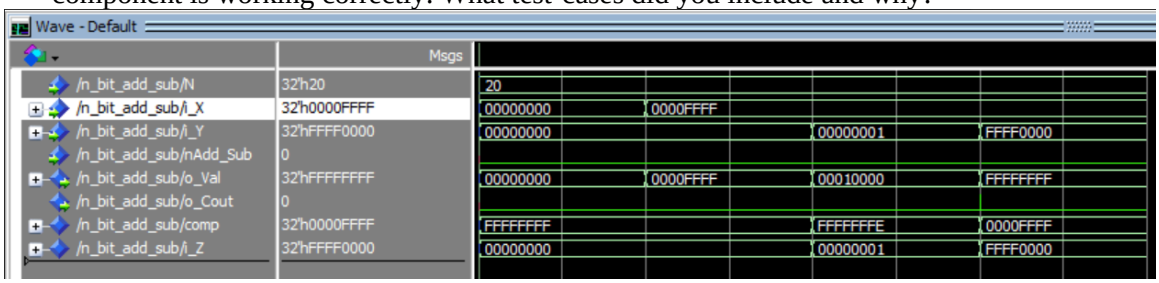
This is the wave form showing the behavior of the full adder with different input values.

g. [Part 4 (a)] Draw a schematic (don't use a schematic capture tool) showing how an N-bit adder/subtractor with control can be implemented using only the three main components designed in problems 1), 2), and 3) (the N-bit inverter, N-bit 2:1 mux, and N-bit adder). How is the 'nAdd_Sub' bit used?

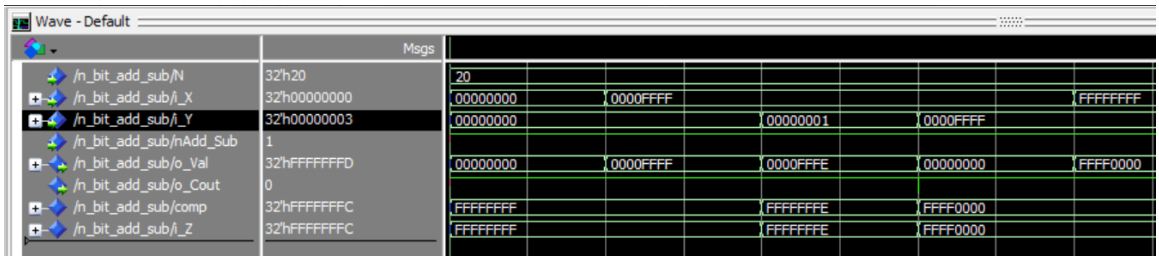


nAdd_Sub is used as both the first carry in bit and the selector bit for the multiplexers. When nAdd_Sub = 0 the multiplexors forward the standard form of the vector to be added and the carry in bit is 0 allowing for addition. When nAdd_Sub = 1 the one's compliment of the vector is forwarded by the multiplexers and the carry in bit = 1 which turns the vector to be added into the two's compliment form to allow subtraction.

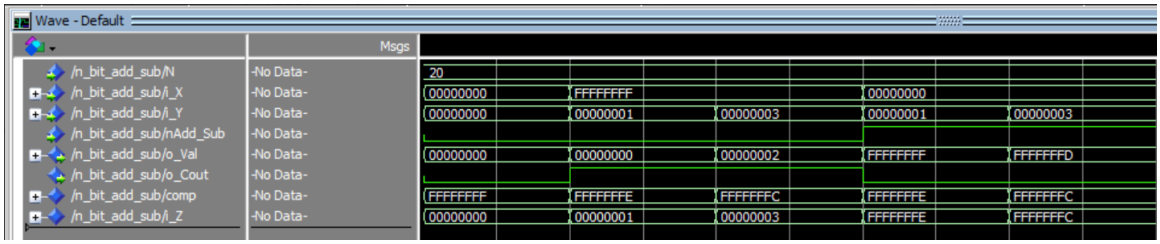
h. [Part 4 (c)] Provide multiple waveform screenshots in your write-up to confirm that this component is working correctly. What test-cases did you include and why?



This is the wave form showing the addition behavior of the Add/Sub with various values.



This is the wave form showing the subtraction behavior of the Add/Sub with various values.



This is the wave form showing the behavior of the Add/Sub in cases with unusual behavior. We can see that if subtraction takes the value below zero, the value wraps around to the max and begins to count down. We can also see that if addition take the value past the max the value wraps around to zero and counts up returning one less than expected.

i. [Feedback] You must complete this section for your lab to be graded. Write down the first response you think of; I expect it to take roughly 5 minutes (do not take more than 10 minutes).

   i. How many hours did you spend on this lab?

Task	During lab time	Outside of lab time
Reading lab	1	1
Pencil/paper design	0	0
VHDL design	.5	3
Assembly coding	0	0
Simulation	.5	1
Debugging	0	1
Report writing	0	1
Other:	0	0
Total	2	7

   ii. If you could change one thing about the lab experience, what would it be? Why?

   I would include a bit more direction when it comes to using new tools rather than having more vague directions to find how to use them on my own.

   iii. What was the most interesting part of the lab?

   The part of the lab that I found most interesting was putting together three smaller components that I had created to make a functional unit that completes a complex task.