LISPM Bus Interface CADR1:BUSINT UML 25-MAR-81 0822
******* DIP MAP *******

26S10 XD x F30	26S10 XD x E30	74LS244 XBD x D30	93S48 BUSPAR x C30	8304 LMDATA x B30	SIP180/3 LMDATA x A30
26S10 XD x F29	26S10 XD x E29	74LS244 XBD x D29	93S48 BUSPAR x C29	8304 LMDATA x B29	SIP180/3 LMDATA x A29
26S10 XD x F28	26S10 XD x E28	74LS244 XBD x D28	93S48 BUSPAR x C28	8304 LMDATA x B28	SIP180/3 LMDATA x A28
26S10 XD x F27	26S10 XD x E27	74LS244 XBD x D27	29701 WBUF x C27	8304 LMDATA x B27	74LS240 LMADR x A27
26S10 XA x F26	26S10 XA x E26	29701 RBUF x D26	29701 WBUF x C26	74LS244 BUSSEL x B26	74LS240 LMADR x A26
26S10 XA x F25	26S10 XA x E25	29701 RBUF x D25	29701 WBUF x C25	74LS244 BUSSEL x B25	74LS240 LMADR x A25
26S10 XA x F24	93S48 XAPAR x E24	29701 RBUF x D24	29701 WBUF x C24	74LS244 BUSSEL x B24	74LS240 LMADR x A24
26S10 XA x F23	93S48 XAPAR x E23	29701 RBUF x D23	74LS244 RBUF x C23	74LS244 BUSSEL x B23	74LS240 LMADR x A23
26S10 XA x F22	74LS244 UBXA x E22	74LS244 RBUF x D22	74LS244 RBUF x C22	8304 DBGOUT x B22	SIP180/3 DBGIN x A22
26S10 XA x F21	74LS244 UBXA x E21	74LS244 RBUF x D21	74LS244 BUSSEL x C21	8304 DBGOUT x B21	8304 DIAG x A21
26S10 XD x F20	74LS244 UBXA x E20	74S86 REQERR xxxx D20	74LS244 BUSSEL x C20	74S00 DATCTL xxxx B20	8304 DIAG x A20

LISPM Bus Interface CADR1;BUSINT UML 25-MAR-81 0823
******* DIP MAP *******

DM8838 UBD x F19	74LS244 UBD x E19	74LS244 BUSSEL x D19	74LS244 BUSSEL x C19	74S04 DATCTL xxxxxx B19	74LS374 DBGIN x A19
DM8838 UBD x F18	74LS244 UBD x E18	74LS240 UBINTC x D18	74S51 DATCTL xx C18	74S32 DATCTL xxxx B18	74LS374 DBGIN x A18
DM8838 UBD x F17	74LS244 UBMAP x E17	74LS374 UBINTC x D17	74S51 DATCTL xx C17	74S02 DATCTL xxxx B17	74S241 DBGOUT x A17
DM8838 UBD x F16	74LS244 UBMAP x E16	25LS2519 UBINTC x D16	74LS244 REQERR x C16	74S08 REQTIM xxxx B16	25LS2519 DBGIN x A16
DM8838 UPRIOR x F15	29701 UBMAP x E15	74LS74 UBINTC xx D15	74S64 DATCTL x C15	8304 REQERR x B15	74S139 DBGIN xo A15
74S38 UPRIOR xxoo F14	29701 UBMAP x E14	74LS74 UBINTC xx D14	74S51 DATCTL xx C14	74S74 RQSYNC xx B14	74S10 DBGIN xxx A14
74S38 UPRIOR xxxx F13	29701 UBMAP x E13	74LS74 UBINTC xx D13	74S10 RQSYNC xxx C13	74S04 XA xxxxxx B13	74S04 DBGIN xxxxxx A13
DM8838 UBA x F12	29701 UBMAP x E12	74S133 REQU x D12	74S260 RQSYNC xx C12	74S02 DBGOUT xxxx B12	74S08 DBGOUT xxxx A12
DM8838 UBA x F11	74S258 UBMAP x E11	74S04 UBA xxxxxx D11	74S64 REQLM x C11	74S51 REQLM xx B11	74S00 DIAG xxxx A11
DM8838 UBA x F10	74S258 UBMAP x E10	74S174 UPRIOR x D10	74S64 REQLM x C10	74S74 REQUB xx B10	MTD100 DBGOUT xoo A10
DM8838 UBA x F09	74S08 REQLM xxoo E09	74S472 UPRIOR x D09	TD100 REQLM x C09	TD250 REQUB x B09	74S32 DBGIN xxxx A09

LISPM Bus Interface CADR1:BUSINT UML 25-MAR-81 0823
******* DIP MAP *******

DM8838 UBA x	74S133 UBCYC x	25LS2519 UPRIOR x	74S04 REQLM xxxxxx	74S74 UBCYC xx	74S175 RQSYNC x
F08	E08	D08	C08	B08	A08
DM8838 UBMAST x	74S139 UBCYC xx	25LS2519 UPRIOR x	MTD100 REQU xxx	74S04 CLM xxxxxx	74S260 RQSYNC xx
F07	E07	D07	C07	B07	A07
DM8838 UPRIOR x	74S260 UBCYC xx	74S10 UBMAST xxx	74S51 REQUB xx	TD100 RQSYNC x	74S175 RQSYNC x
F06	E06	D06	C06	B06	A06
74S133 UBCYC x	74S04 UBINTC xxxxxx	74S00 UBINTC xxxx	74S20 REQU xo	74S11 RQSYNC xxx	74S02 RQSYNC xxxx
F05	E05	D05	C05	B05	A05
TD250 UBCYC x	74S32 UBINTC xxxx	74S74 UBMAST xx	74S11 DBGIN xxx	74S241 DBGOUT x	74S00 REQU xxxx
F04	E04	D04	C04	B04	A04
74S00 REQU xxxx	74S138 UBCYC x	74LS74 REQU xx	74LS27 UPRIOR xxx	74S04 REQTIM xxxxxx	74LS112 REQERR ox
F03	E03	D03	C03	B03	A03
74S02 REQU xxxx	74S08 UBINTC xxxx	74LS74 UBMAST xx	74LS74 UBMAST xx	74 276 REQERR x	74S288 REQTIM x
F02	E02	D02	C02	B02	A02
TD100 REQU x	74S00 UBMAST xxxx	MTD100 UBMAST xxx	74LS163 UPRIOR x	74LS273 REQTIM x	74LS124 REQTIM xo
F01	E01	D01	C01	B01	A01

LISPM Bus Interface CADR1;BUSINT UML 25-MAR-81 0823
******* EDGE CONNECTIONS Flags: (# Output, @ Terminator, ---- Dedicated ground, ++++ Dedicated power) *******

-A-	-B-	-C-	-D-
A1 -XBUS35 A2 +5.0V++++++++++++++++++	A1 -XBUS5 A2 +5.0V++++++++++++++++++	#A1 UB NPG IN #A2 +5.0V++++++++++++++++++	#A1 #A2 +5.0V++++++++++++++++++
B1 -XBUS34 B2 -5.0V	B1 -XBUS4 B2 -5.0V	#B1 UB NPG OUT #B2 -5.0V	#B1 #B2 -5.0V
C1 -XBUS33 C2 GND----------	C1 -XBUS3 C2 GND----------	#C1 -XBUS RQ #C2 GND----------	#C1 #C2 GND----------
D1 -XBUS32 D2 -XBUS31	D1 -XBUS2 #D2 -XBUS1	#D1 -XBUS ACK #D2 -UBD16 H	#D1 #D2 -UB BR7 H #
E1 -XBUS30 E2 -XBUS29	#E1 -XBUS0 #E2 -XBUS PAR	#E1 -XBUS WR #E2 -UBD14 H	#E1 #E2 -UB BR6 H #
F1 GND F2 -XBUS28	F1 GND #F2 -XADDR PAR	F1 GND #F2 -UBD13 H	F1 GND #F2 -UB BR5 H #
H1 -XBUS27 H2 -XBUS26	#H1 -XADDR21 #H2 -XADDR20	#H1 -UBD11 H #H2 -UBD12 H	#H1 #H2 -UB BR4 H #
J1 -XBUS25 J2 -XBUS24	#J1 -XADDR19 #J2 -XADDR18	#J1 -XBUS IGNPAR #J2 -UBD10 H	#J1 #J2
K1 -XBUS23 K2 -XBUS22	#K1 -XADDR17 #K2 -XADDR16	#K1 -XBUS INIT #K2 -UBD9 H	#K1 #K2 UB BG7 IN #
L1 -XBUS21 L2 -XBUS20	#L1 -XADDR15 #L2 -XADDR14	#L1 -XBUS EXTRQ #L2 -UBD8 H	#L1 -UB INIT H # #L2 UB BG7 IN #
M1 -XBUS19 M2 -XBUS18	#M1 -XADDR13 #M2 -XADDR12	#M1 -XBUS BUSY #M2 -UBD7 H	#M1 #M2 UB BG6 IN #
N1 GND N2 -XBUS17	N1 GND #N2 -XADDR11	N1 GND #N2 -UBD4 H	N1 GND #N2 UB BG6 IN #
P1 -XBUS16 P2 -XBUS15	#P1 -XADDR10 #P2 -XADDR9	#P1 -XBUS SYNC #P2 -UBD5 H	#P1 +12.0V #P2 UB BG5 IN #
R1 -XBUS14 R2 -XBUS13	#R1 -XADDR8 #R2 -XADDR7	#R1 -LM BOOT H #R2 -UBD1 H	R1 +12.0V #R2 UB BG5 IN #
S1 -XBUS12 S2 -XBUS11	#S1 -XADDR6 #S2 -XADDR5	#S1 -XBUS INTR #S2 -UBD0 H	#S1 +12.0V #S2 UB BG4 IN #
T1 GND----------	T1 GND----------	T1 GND----------	T1 GND----------
T2 -XBUS10	#T2 -XADDR4	#T2 -UBD3 H	#T2 UB BG4 IN #
U1 -XBUS9 U2 -XBUS8	#U1 -XADDR3 #U2 -XADDR2	#U1 -XBUS POWER RESET H #U2 -UBD2 H	#U1 #U2
V1 -XBUS7 V2 -XBUS6	#V1 -XADDR1 #V2 -XADDR0	#V1 -XBUS EXTGRANT OUT #V2 -UBD6 H	#V1 #V2

LISPM Bus Interface CADR1;BUSINT UML 25-MAR-81 0823
******* EDGE CONNECTIONS Flags: (# Output, @ Terminator, ---- Dedicated ground, ++++ Dedicated power) *******

-E-		-F-		-J01-		-J02-	
A1		A1		01 CLK0	#	01	
A2 +5.0V++++++++++++++++++		A2 +5.0V++++++++++++++++++		02 -MEMRQ H	@	02	
B1		B1		03 -LM ACK H	#	03	
B2 -5.0V		B2 -5.0V		04 LMX GRANT	#	04	
C1 -UB ADR12 H	#	C1		05 LMUB GRANT	#	05	
C2 GND----------		C2 GND----------		06 XBUS REQUEST	#	06	
D1 -UB ADR17 H	#	D1 -UB BBSY H	#	07 LMUB MASTER	#	07	
D2 -UB ADR15 H	#	D2		08 C1 OUT	#	08	
E1 -UB MSYN H	#	E1		09 XWR	#	09	
E2 -UB ADR16 H	#	E2		10 -FREE H	#	10	
F1 -UB ADR2 H	#	F1 GND		11 NXM TIMEOUT	#	11	
F2 -UB C1 H	#	F2		12 -ANY PAR ERROR H	#	12	
H1 -UB ADR1 H	#	H1		13 ANY GRANT DLYD	#	13	
H2 -UB ADR0 H	#	H2		14 MSYN IN	#	14	
J1 -UB SSYN H	#	J1 -UB NPR H	#	15 MSYN OUT	#	15	
J2 -UB C0 H		J2		16 SSYN IN	#	16	
K1 -UB ADR14 H	#	K1		17 SSYN OUT	#	17	
K2 -UB ADR13 H	#	K2		18 UB REG CYC TO	#	18	
L1 -UB ADR11 H	#	L1		19 UBXRQ	#	19	
L2		L2		20 UBX GRANT	#	20	
M1		M1 -UB INTR H	#	21 -DEBUG IN REQ H	@	21	
M2		M2		22 DEBUG ACK	#	22	
N1 GND		N1 GND		23 DBUB MASTER	#	23	
N2 -UB ADR8 H	#	N2		24 NC	#	24	
P1 -UB ADR10 H	#	P1		25 NC	#	25	
P2 -UB ADR7 H	#	P2		26 ----------		26 ----------	
R1 -UB ADR9 H	#	R1		27 ----------		27 ----------	
R2		R2		28 ----------		28 ----------	
S1		S1		29 ----------		29 ----------	
S2		S2		30 ----------		30 ----------	
T1 GND----------		T1 GND----------		31 ----------		31 ----------	
T2		T2 -UB SACK H	#	32 ----------		32 ----------	
U1 -UB ADR6 H	#	U1		33 ----------		33 ----------	
U2 -UB ADR4 H	#	U2		34 ----------		34 ----------	
V1 -UB ADR5 H	#	V1		35 ----------		35 ----------	
V2 -UB ADR3 H	#	V2 LOCAL ENABLE	@	36 ----------		36 ----------	
				37 ----------		37 ----------	
				38 ----------		38 ----------	
				39 ----------		39 ----------	
				40 ----------		40 ----------	
				41 ----------		41 ----------	
				42 ----------		42 ----------	
				43 ----------		43 ----------	
				44 ----------		44 ----------	
				45 ----------		45 ----------	
				46 ----------		46 ----------	
				47 ----------		47 ----------	
				48 ----------		48 ----------	
				49 ----------		49 ----------	
				50 ----------		50 ----------	

LISPM Bus Interface CADR1;BUSINT UML 25-MAR-81 0823
******* EDGE CONNECTIONS Flags: (# Output, @ Terminator, ---- Dedicated ground, ++++ Dedicated power) *******

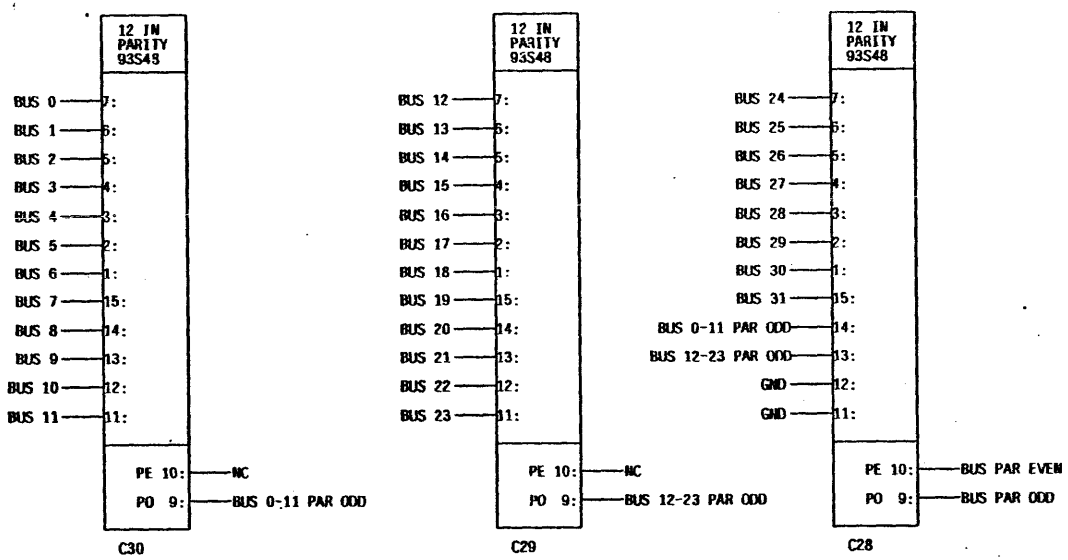
-J03-	-J04-	-J05-	-J06-
01	01	01 DBD0 #	01 DBD0 #
02	02	02 DBD1 #	02 DBD1 #
03	03	03 DBD2 #	03 DBD2 #
04	04	04 DBD3 #	04 DBD3 #
05	05	05 DBD4 #	05 DBD4 #
06	06	06 DBD5 #	06 DBD5 #
07	07	07 DBD6 #	07 DBD6 #
08	08	08 DBD7 #	08 DBD7 #
09	09	09 DBD8 #	09 DBD8 #
10	10	10 DBD9 #	10 DBD9 #
11	11	11 DBD10 #	11 DBD10 #
12	12	12 DBD11 #	12 DBD11 #
13	13	13 DBD12 #	13 DBD12 #
14	14	14 DBD13 #	14 DBD13 #
15	15	15 DBD14 #	15 DBD14 #
16	16	16 DBD15 #	16 DBD15 #
17	17	17 DEBUG IN A0 @	17 DEBUG OUT A0 #
18	18	18 DEBUG IN A1 @	18 DEBUG OUT A1 #
19	19	19 DEBUG IN WR @	19 DEBUG OUT WR #
20	20	20 -DEBUG IN REQ H @	20 -DEBUG OUT REQ H #
21 ----------	21 ----------	21 DEBUG IN ACK #	21 DEBUG OUT ACK @
22 ----------	22 ----------	22 NC #	22 NC #
23 ----------	23 ----------	23 NC #	23 NC #
24 ----------	24 ----------	24 NC #	24 NC #
25 ----------	25 ----------	25 NC #	25 NC #
26 ----------	26 ----------	26 ----------	26 ----------
27 ----------	27 ----------	27 ----------	27 ----------
28 ----------	28 ----------	28 ----------	28 ----------
29 ----------	29 ----------	29 ----------	29 ----------
30 ----------	30 ----------	30 ----------	30 ----------
31 ----------	31 ----------	31 ----------	31 ----------
32 ----------	32 ----------	32 ----------	32 ----------
33 ----------	33 ----------	33 ----------	33 ----------
34 ----------	34 ----------	34 ----------	34 ----------
35 ----------	35 ----------	35 ----------	35 ----------
36 ----------	36 ----------	36 ----------	36 ----------
37 ----------	37 ----------	37 ----------	37 ----------
38 ----------	38 ----------	38 ----------	38 ----------
39 ----------	39 ----------	39 ----------	39 ----------
40 ----------	40 ----------	40 ----------	40 ----------
		41 ----------	41 ----------
		42 ----------	42 ----------
		43 ----------	43 ----------
		44 ----------	44 ----------
		45 ----------	45 ----------
		46 ----------	46 ----------
		47 ----------	47 ----------
		48 ----------	48 ----------
		49 ----------	49 ----------
		50 ----------	50 ----------

LISPM Bus Interface CADR1;BUSINT UML 25-MAR-81 0823
******* EDGE CONNECTIONS Flags: (# Output, @ Terminator, ---- Dedicated ground, ++++ Dedicated power) *******

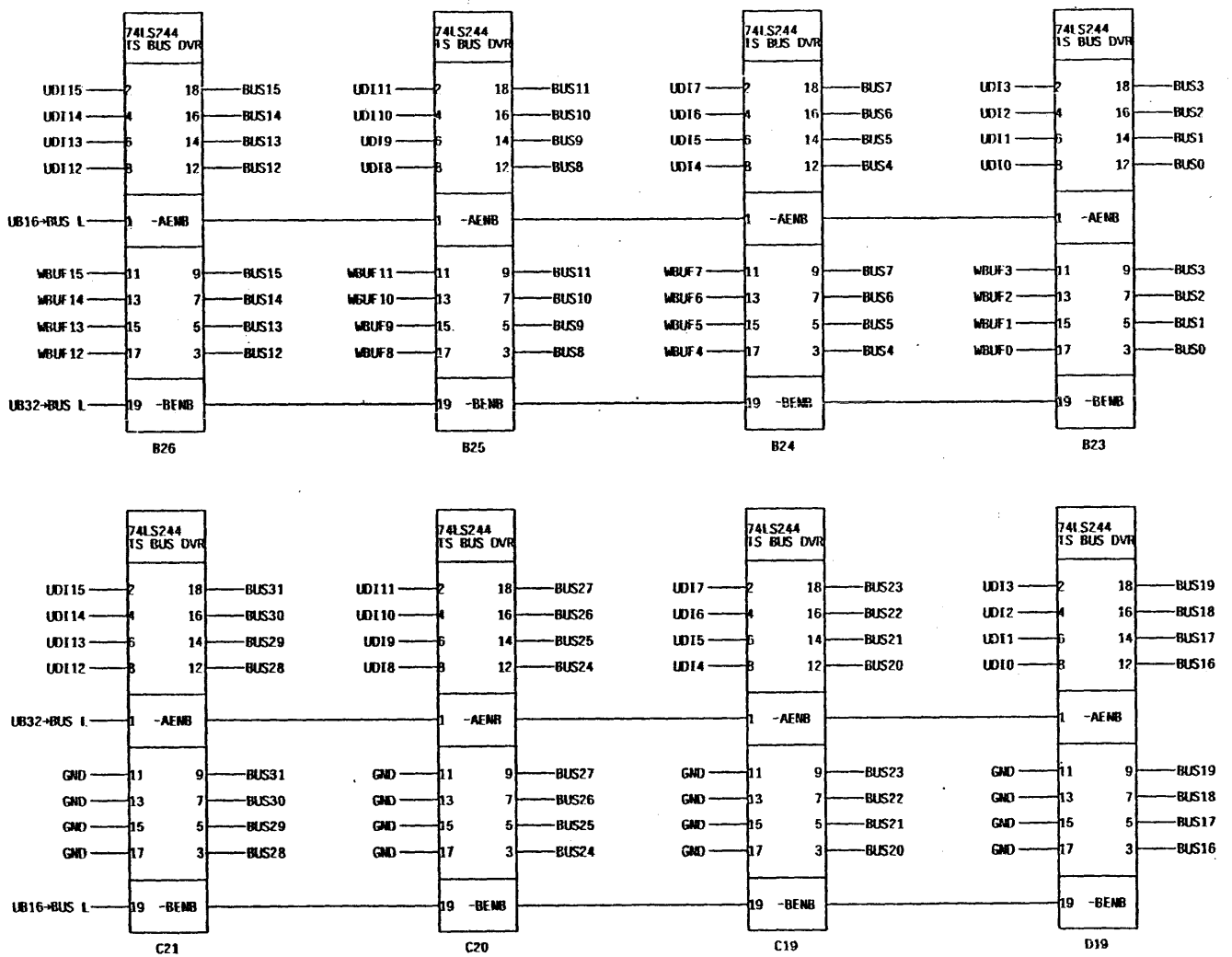
-J07-	-J08-	-J09-	-J10-
01 SPY0	# 01 GND	01 -ADR15. H	01
02 SPY1	# 02 -MCLK7 H	@ 02 -ADR14 H	02
03 SPY2	# 03 GND	03 -ADR13 H	03
04 SPY3	# 04 GND	04 -ADR12 H	04
05 SPY4	# 05 SPY ADR 1	# 05 -ADR11 H	05
06 SPY5	# 06 SPY ADR 2	# 06 -ADR10 H	06
07 SPY6	# 07 SPY ADR 3	# 07 -ADR9 H	07
08 SPY7	# 08 SPY ADR 4	# 08 -ADR8 H	08
09 SPY8	# 09 -SPY READ H	# 09 -ADR7 H	09
10 SPY9	# 10 -SPY WRITE H	# 10 -ADR6 H	10
11 SPY10	# 11 -BUSINT LM RESET H	# 11 -ADR5 H	11
12 SPY11	# 12 -LM BOOT H	12 -ADR4 H	12
13 SPY12	# 13 -LM UNIBUS RESET H	13 -ADR3 H	13
14 SPY13	# 14 LM MEMDRIVE ENB	# 14 -ADR2 H	14
15 SPY14	# 15 -LM POWER RESET H	15 -ADR1 H	15
16 SPY15	# 16 NC	# 16 -ADR0 H	16
17 -LM GRANT H	# 17 NC	# 17 -MEMRQ H	@ 17
18 WRCYC	@ 18 NC	# 18 -LM ACK H	# 18
19 LM INT	# 19 NC	# 19 -LOADMD H	# 19
20 MEMPAR FROM LM	@ 20 NC	# 20 -LM IGNPAR H	# 20
21 ----------	21 ----------	21	21
22 ----------	22 ----------	22	22
23 ----------	23 ----------	23	23
24 ----------	24 ----------	24	24
25 ----------	25 ----------	25	25
26 ----------	26 ----------	26 ----------	26 ----------
27 ----------	27 ----------	27 ----------	27 ----------
28 ----------	28 ----------	28 ----------	28 ----------
29 ----------	29 ----------	29 ----------	29 ----------
30 ----------	30 ----------	30 ----------	30 ----------
31 ----------	31 ----------	31 ----------	31 ----------
32 ----------	32 ----------	32 ----------	32 ----------
33 ----------	33 ----------	33 ----------	33 ----------
34 ----------	34 ----------	34 ----------	34 ----------
35 ----------	35 ----------	35 ----------	35 ----------
36 ----------	36 ----------	36 ----------	36 ----------
37 ----------	37 ----------	37 ----------	37 ----------
38 ----------	38 ----------	38 ----------	38 ----------
39 ----------	39 ----------	39 ----------	39 ----------
40 ----------	40 ----------	40 ----------	40 ----------
		41 ----------	41 ----------
		42 ----------	42 ----------
		43 ----------	43 ----------
		44 ----------	44 ----------
		45 ----------	45 ----------
		46 ----------	46 ----------
		47 ----------	47 ----------
		48 ----------	48 ----------
		49 ----------	49 ----------
		50 ----------	50 ----------

LISPM Bus Interface CADR1;BUSINT UML 25-MAR-81 0823
******* EDGE CONNECTIONS Flags: (# Output, @ Terminator, ---- Dedicated ground, ++++ Dedicated power) *******

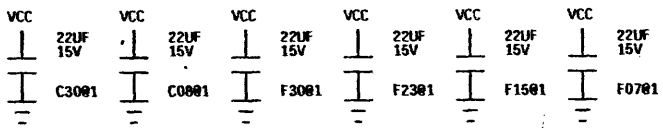
-J11-		-J12-	
01 MEM31	#	01 MEM11	#
02 MEM30	#	02 MEM10	#
03 MEM29	#	03 MEM9	#
04 MEM28	#	04 MEM8	#
05 MEM27	#	05 MEM7	#
06 MEM26	#	06 MEM6	#
07 MEM25	#	07 MEM5	#
08 MEM24	#	08 MEM4	#
09 MEM23	#	09 MEM3	#
10 MEM22	#	10 MEM2	#
11 MEM21	#	11 MEM1	#
12 MEM20	#	12 MEM0	#
13 MEM19	#	13 MEMPAR TO LM	#
14 MEM18	#	14 -ADRPAR H	
15 MEM17	#	15 -ADR21 H	
16 MEM16	#	16 -ADR20 H	
17 MEM15	#	17 -ADR19 H	
18 MEM14	#	18 -ADR18 H	
19 MEM13	#	19 -ADR17 H	
20 MEM12	#	20 -ADR16 H	
21 ----------		21 ----------	
22 ----------		22 ----------	
23 ----------		23 ----------	
24 ----------		24 ----------	
25 ----------		25 ----------	
26 ----------		26 ----------	
27 ----------		27 ----------	
28 ----------		28 ----------	
29 ----------		29 ----------	
30 ----------		30 ----------	
31 ----------		31 ----------	
32 ----------		32 ----------	
33 ----------		33 ----------	
34 ----------		34 ----------	
35 ----------		35 ----------	
36 ----------		36 ----------	
37 ----------		37 ----------	
38 ----------		38 ----------	
39 ----------		39 ----------	
40 ----------		40 ----------	



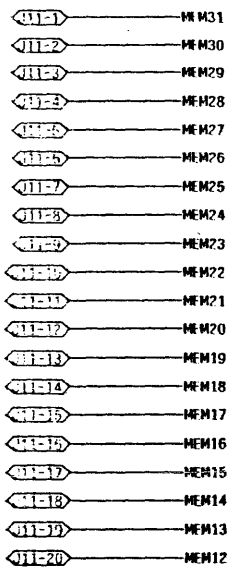
CBUS	BUS PARITY	10-DEC-1980 10:04	AI: CADR1; BUSPAR



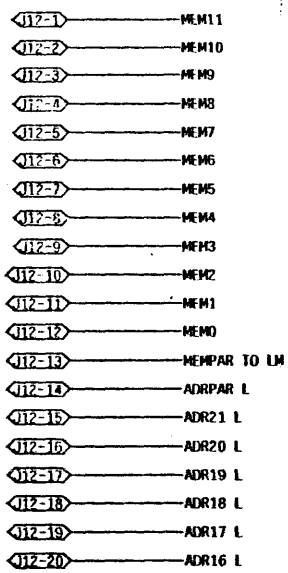
CBUS	BUS FROM UNIBUS	10-DEC-1980 10:05	AI: CADR1; BUSSEL



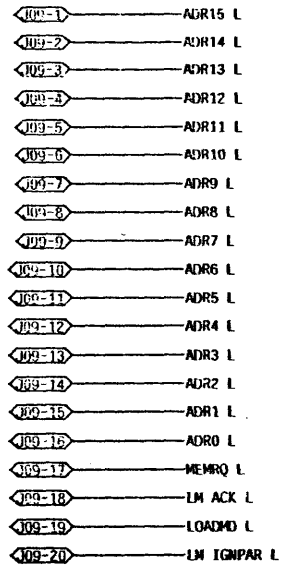
CBUS	BYPASS CAPACITORS	10-DEC-1980 10:06	AI: CADR1; CAPS



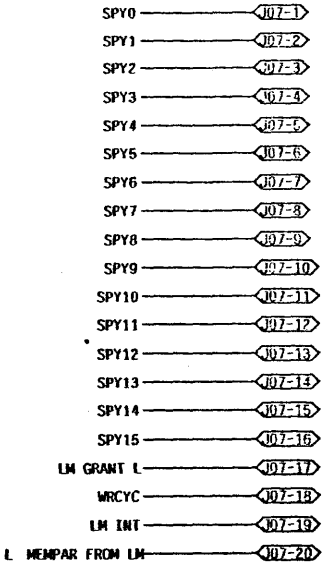
CADR; BCPINS
to 1AJ1



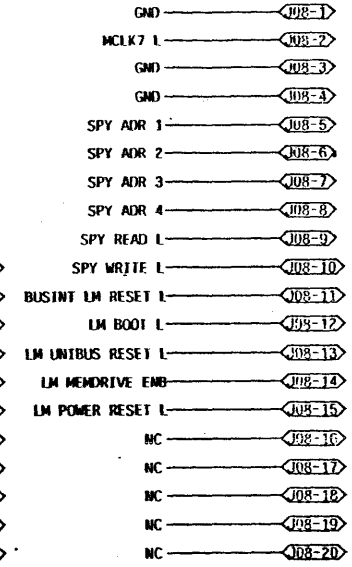
CADR; BCPINS
to 1BJ1



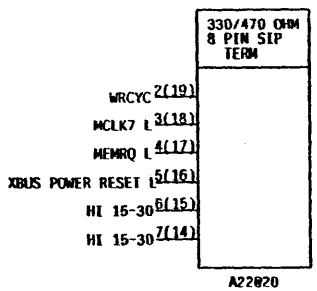
CADR; BCPINS
to 1CJ1

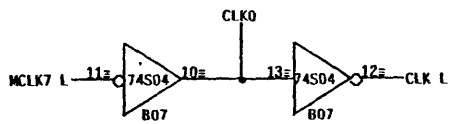


TO 3AJ1
CADR; BCPINS

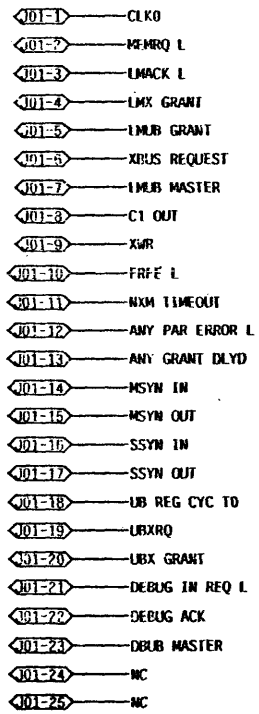


TO 5AJ1
CADR; MBCPIN

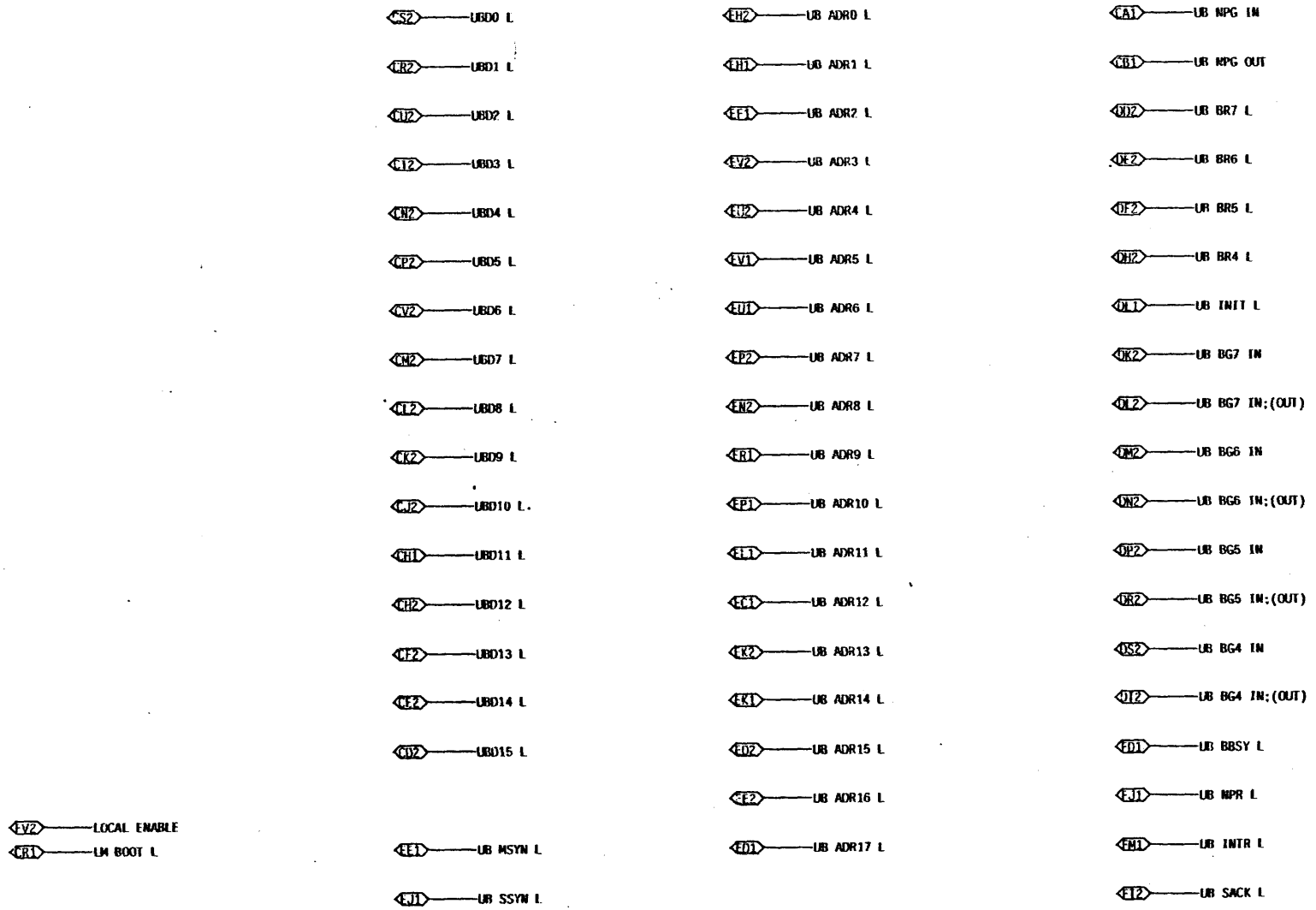




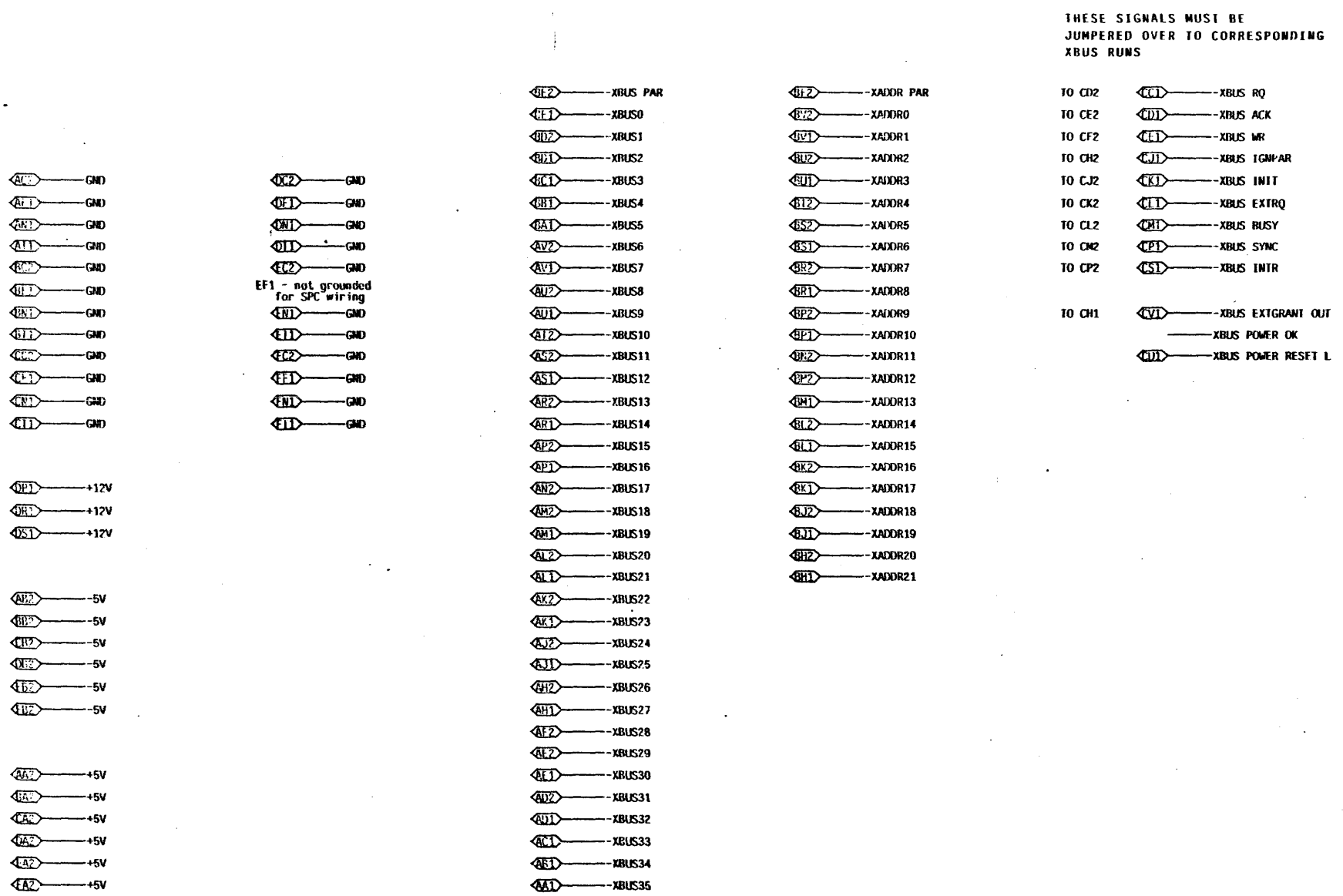
CBUS	CABLES TO PROCESSOR	10-DEC-1980 10:04	AI: CADR1; CLM



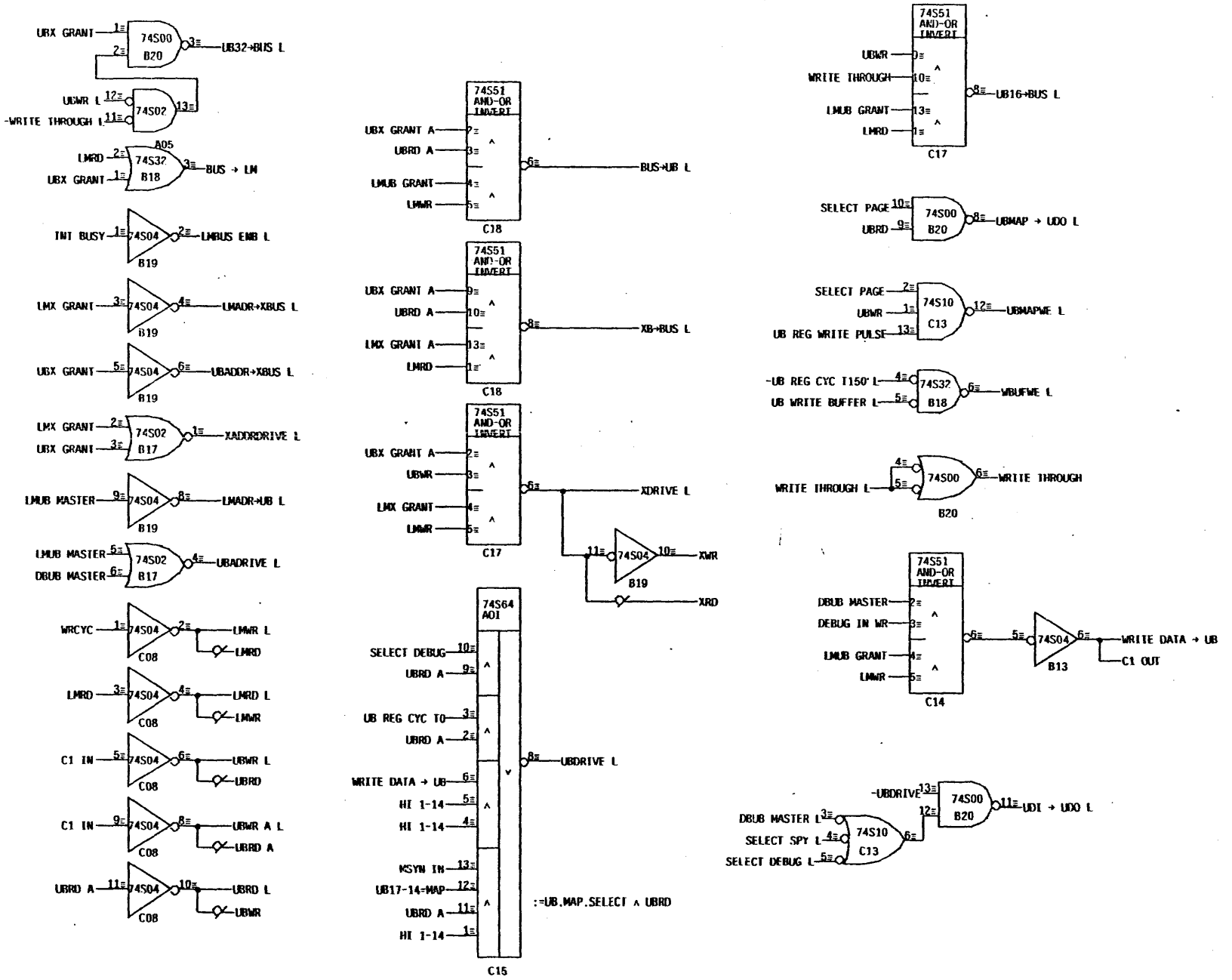
CBUS	TEST POINTS	8-SEP-1978 13:11	AI: CADR1; CTP



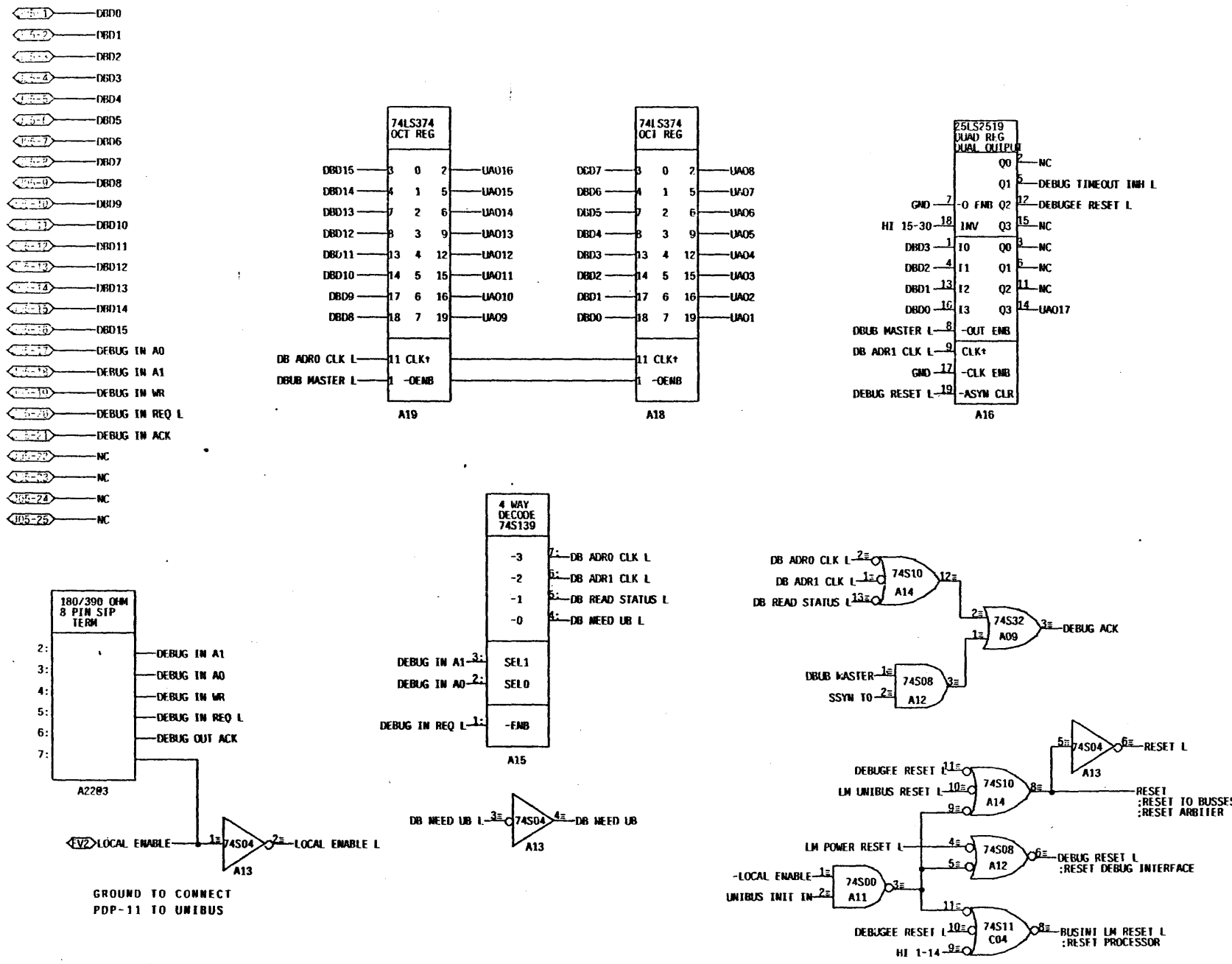
CBUS	UNIBUS SPC CONNS	3-OCT-1978 07:16	AI: CADR1; CUBUS



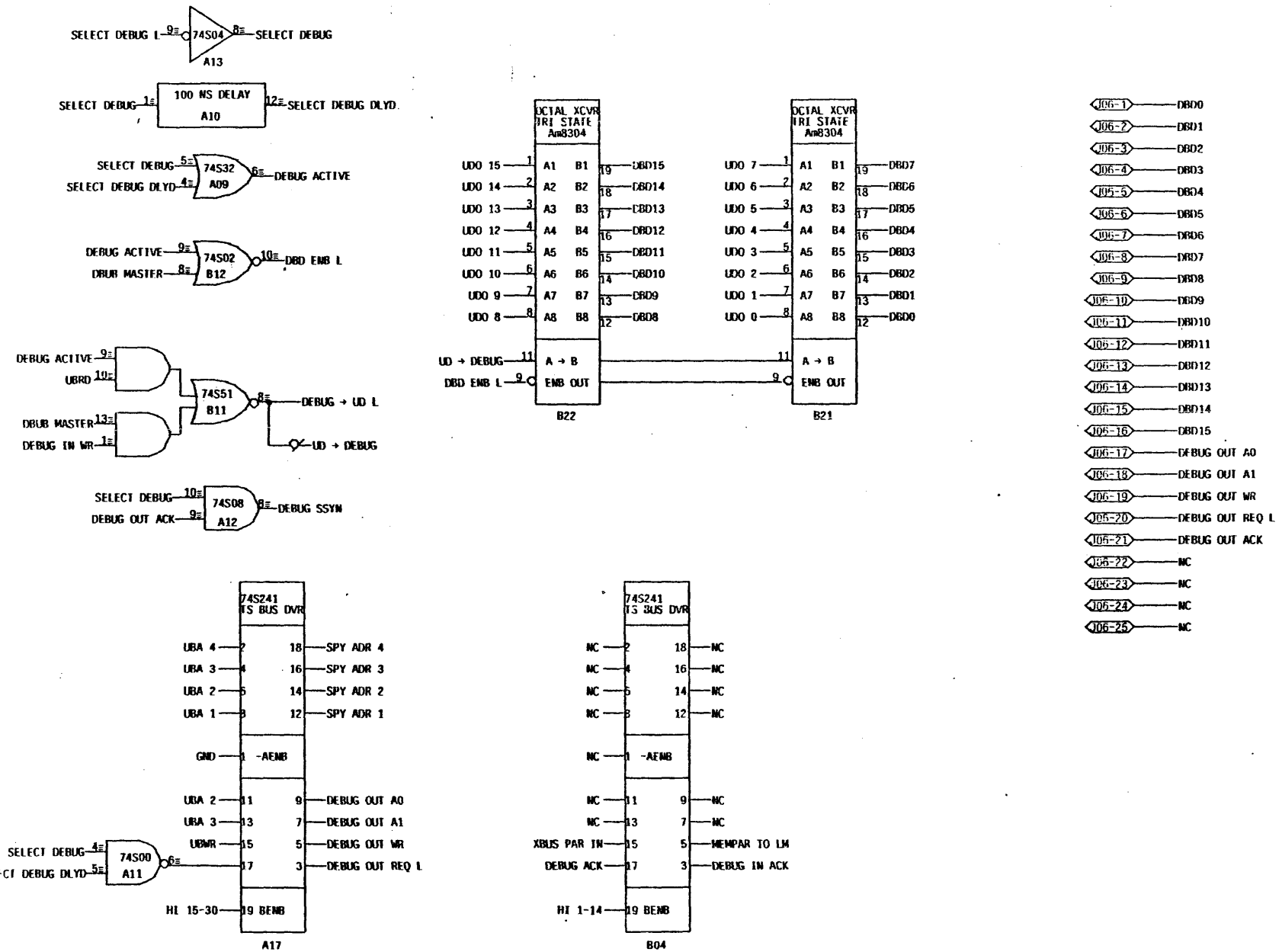
CBUS	XBUS BACKPLANE CONNS	10-DEC-1980 10:09	AI: CADR1; CXBUS



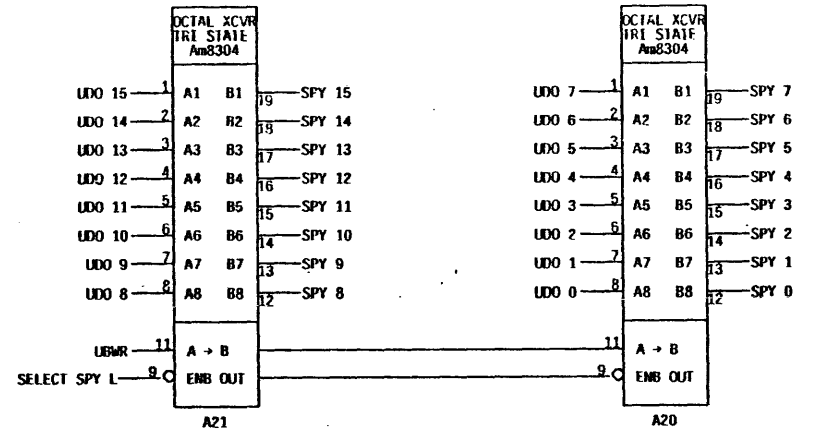
CBUS	DATA PATH CONTROL	10-DEC-1980 17:33	AI: CADR1; DATCTL

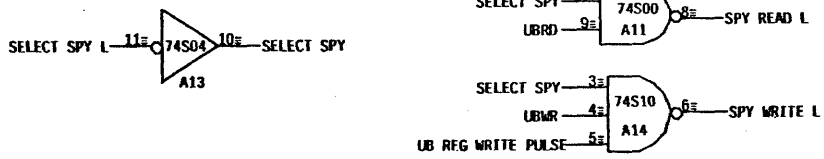


CBUS	DEBUGEE DATA PATH	10-DEC-1980 10:25	AI: CADR1; DBGIN

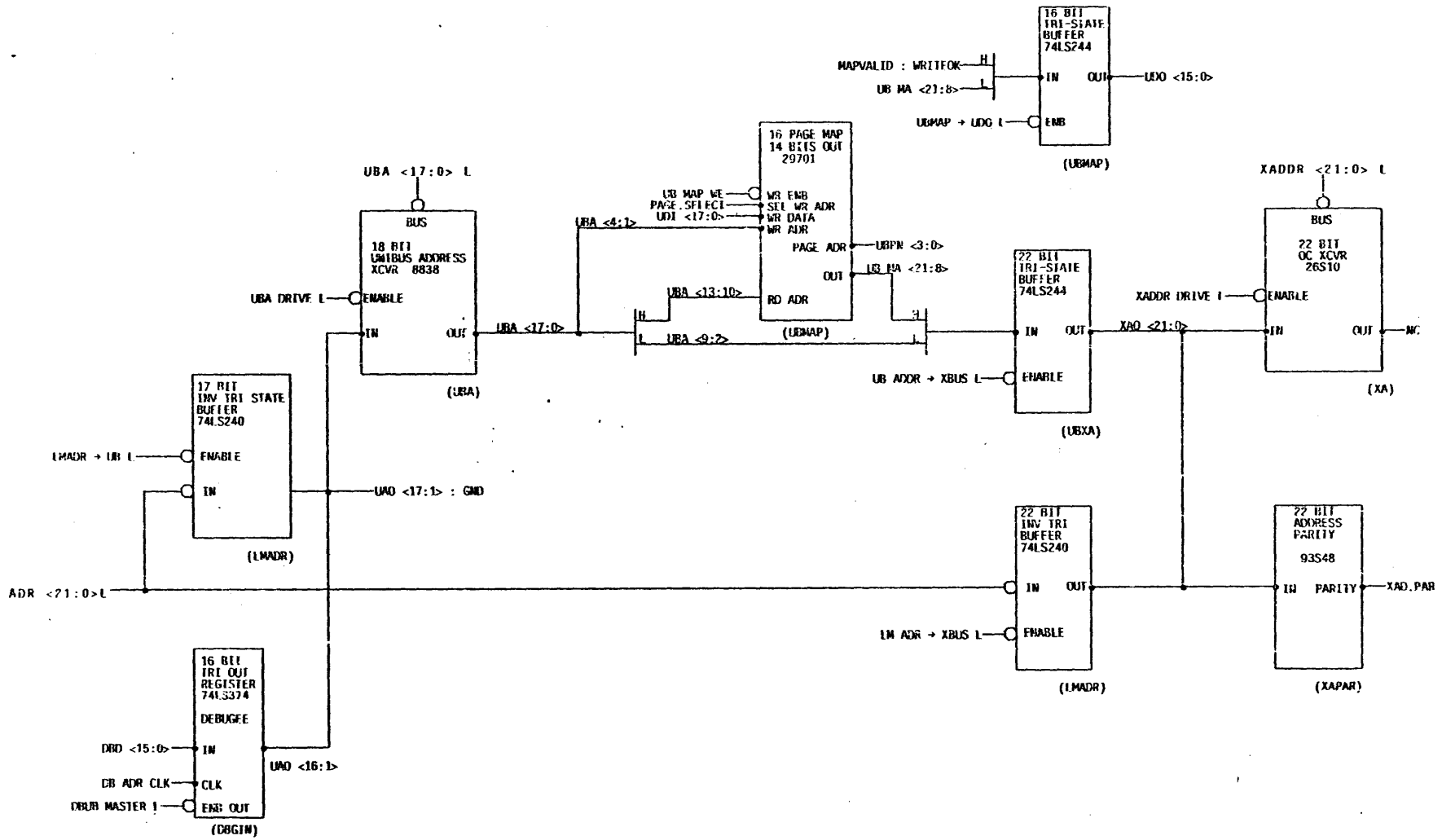


CBUS	DEBUGER DATA PATH	10-DEC-1980 10:26	AI: CADR1; DBGOUT

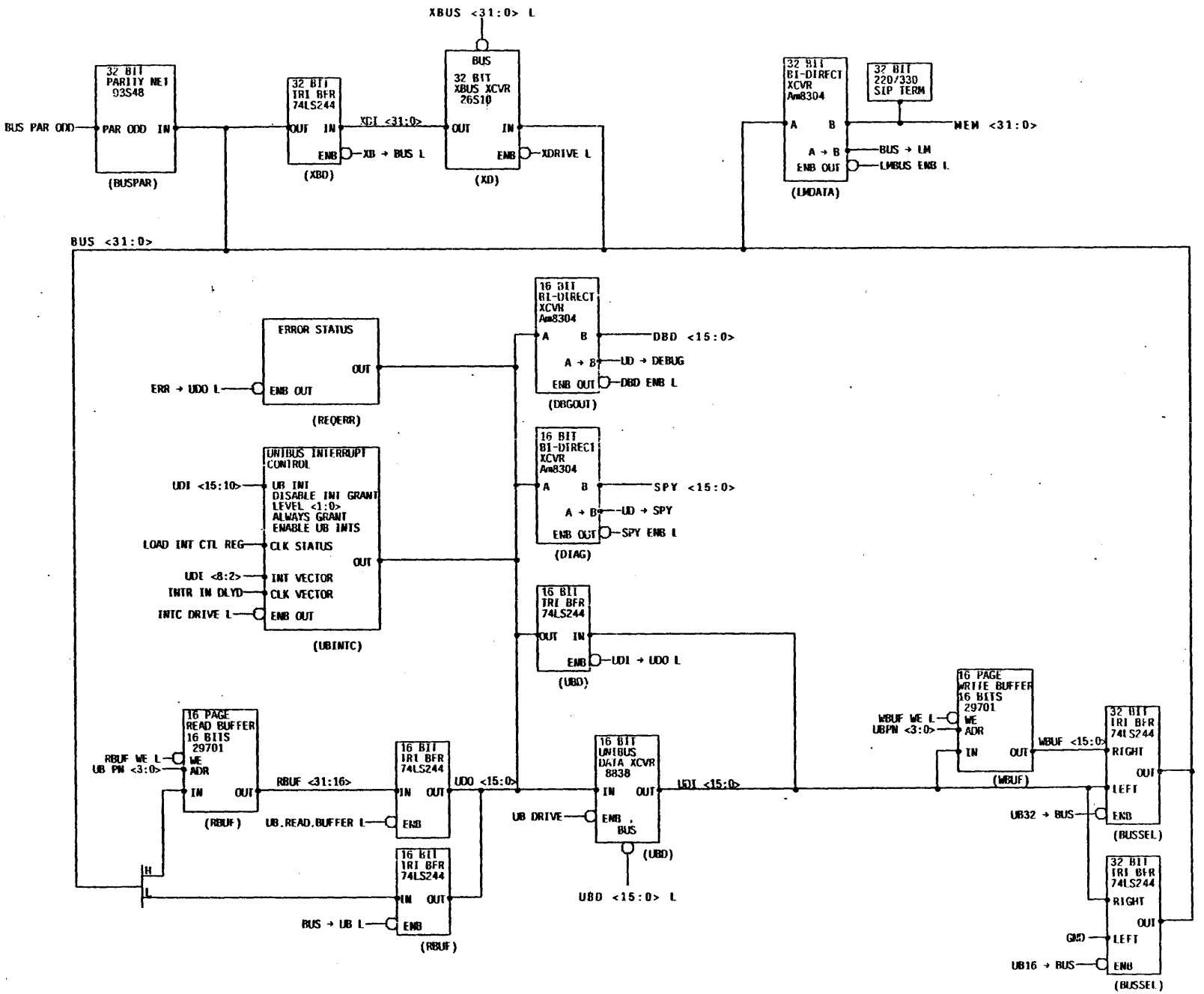




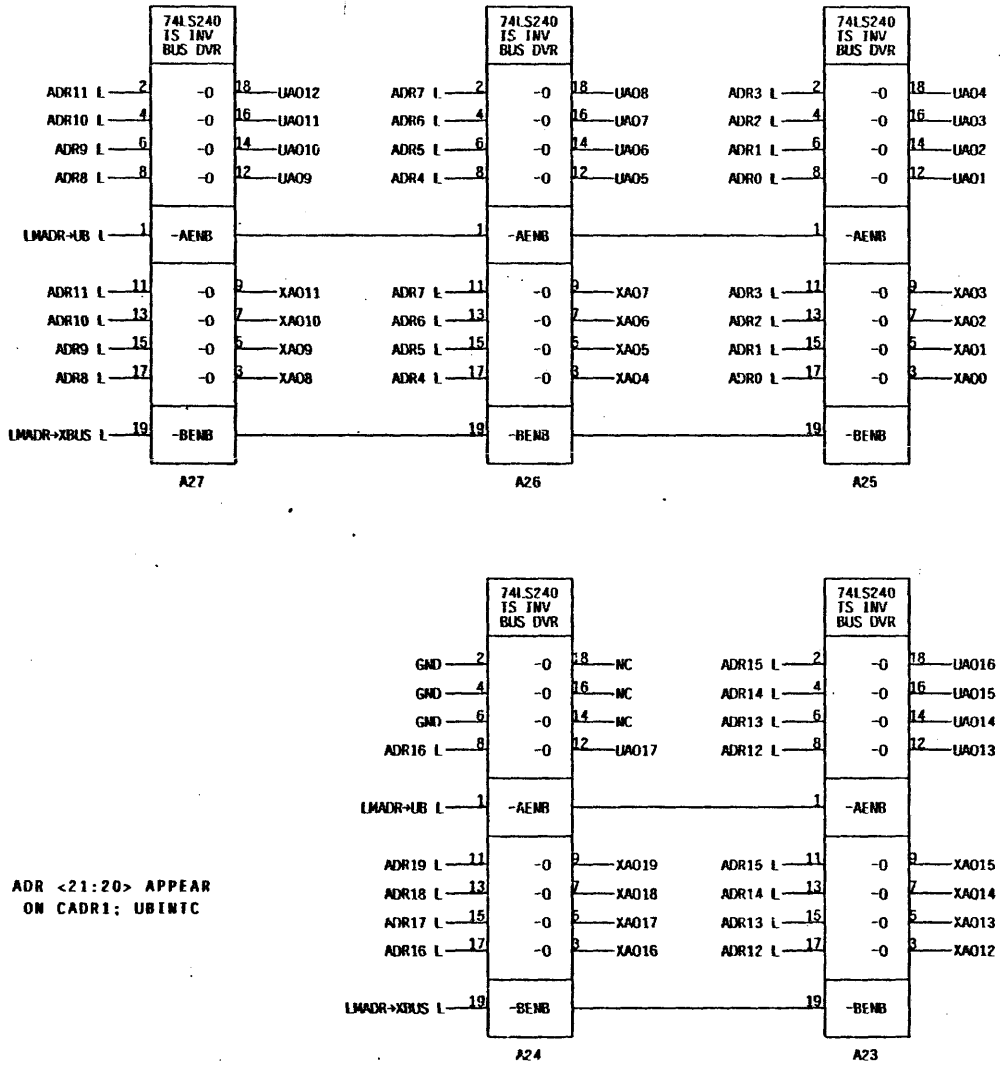
CBUS	DIAGNOSTIC BUS	10-DEC-1980 10:26	AI: CADR1; DIAG

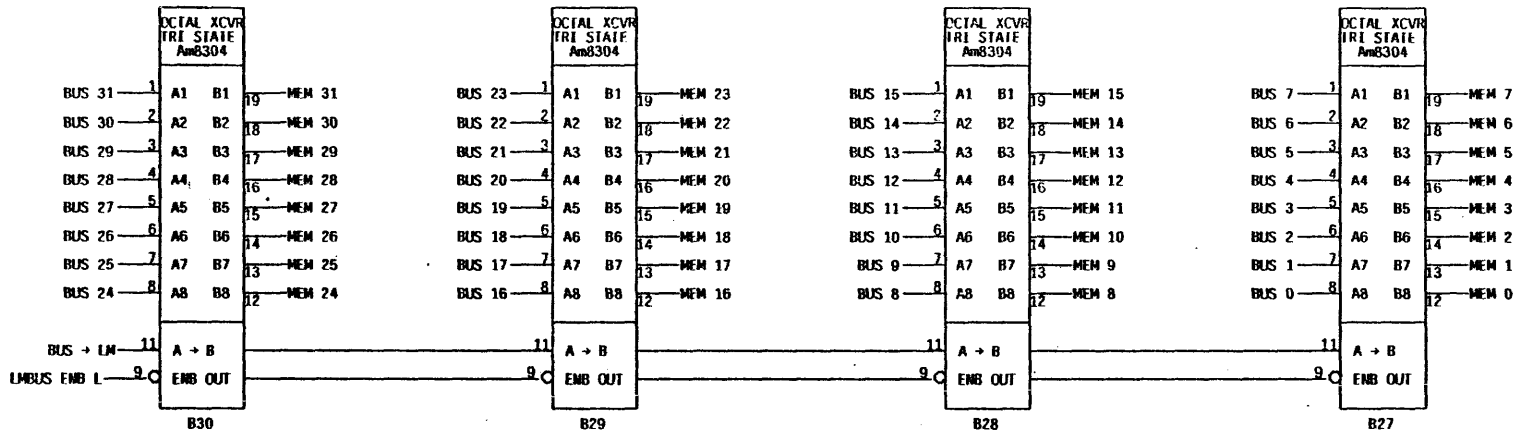


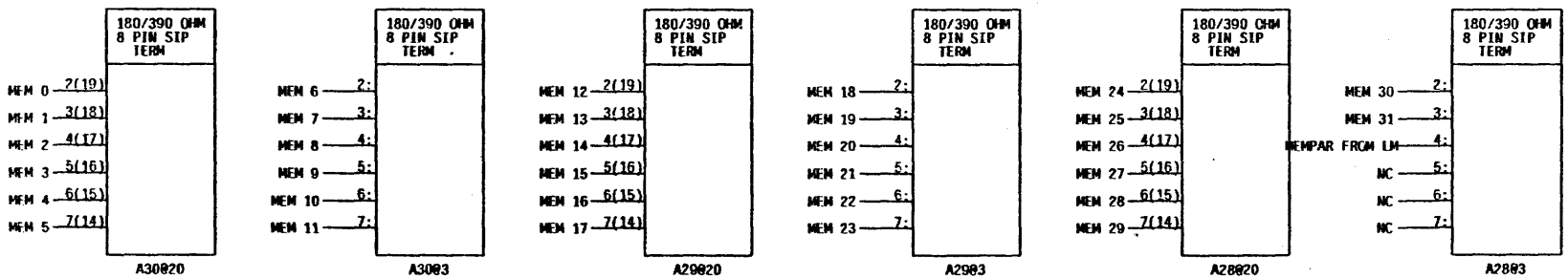
C5US	DATA PATH - ADDRESS	25-MAY-1978 16:41	AI: CADR1; DPADR



CBUS	DATA PATH - XBUS DATA	25-MAY-1978 16:47	AI: CADR1; DPDATA

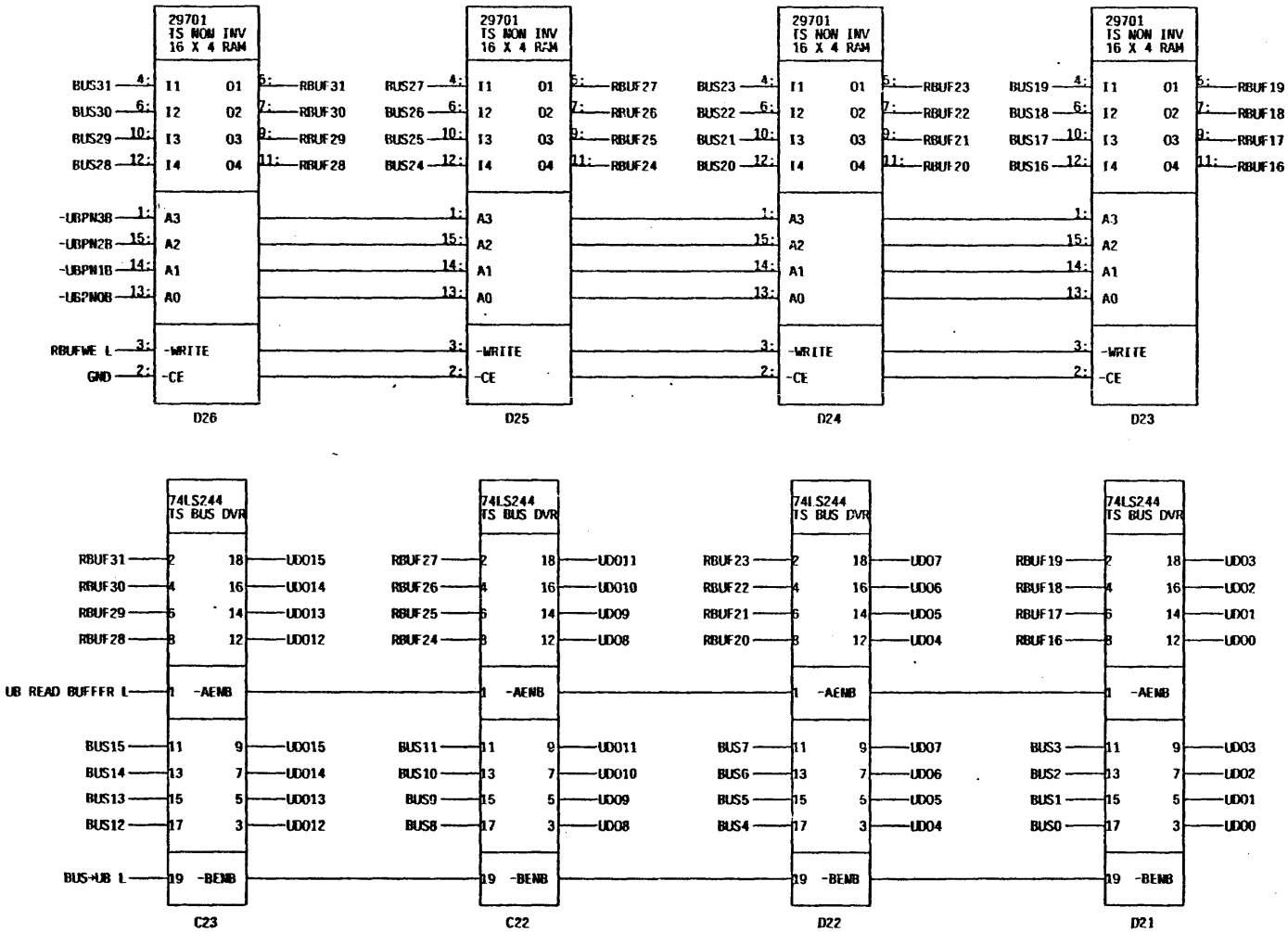

74LS240
TS INV
BUS DVR
ADR11 L
ADR10 L
ADR9 L
ADR8 L
-0
UA012
UA011
UA010
UA09
LMADR→UB L
-AENB
ADR11 L
ADR10 L
ADR9 L
ADR8 L
XA011
XA010
XA09
XA08
LMADR→XBUS L
-BENB
A27
ADR7 L
ADR6 L
ADR5 L
ADR4 L
UA08
UA07
UA06
UA05
XA07
XA06
XA05
XA04
A26
ADR3 L
ADR2 L
ADR1 L
ADR0 L
UA04
UA03
UA02
UA01
XA03
XA02
XA01
XA00
A25
GND
GND
GND
ADR16 L
NC
NC
NC
UA017
ADR19 L
ADR18 L
ADR17 L
ADR16 L
XA019
XA018
XA017
XA016
A24
ADR15 L
ADR14 L
ADR13 L
ADR12 L
UA016
UA015
UA014
UA013
XA015
XA014
XA013
XA012
A23
ADR <21:20> APPEAR
ON CADR1; UBINTC



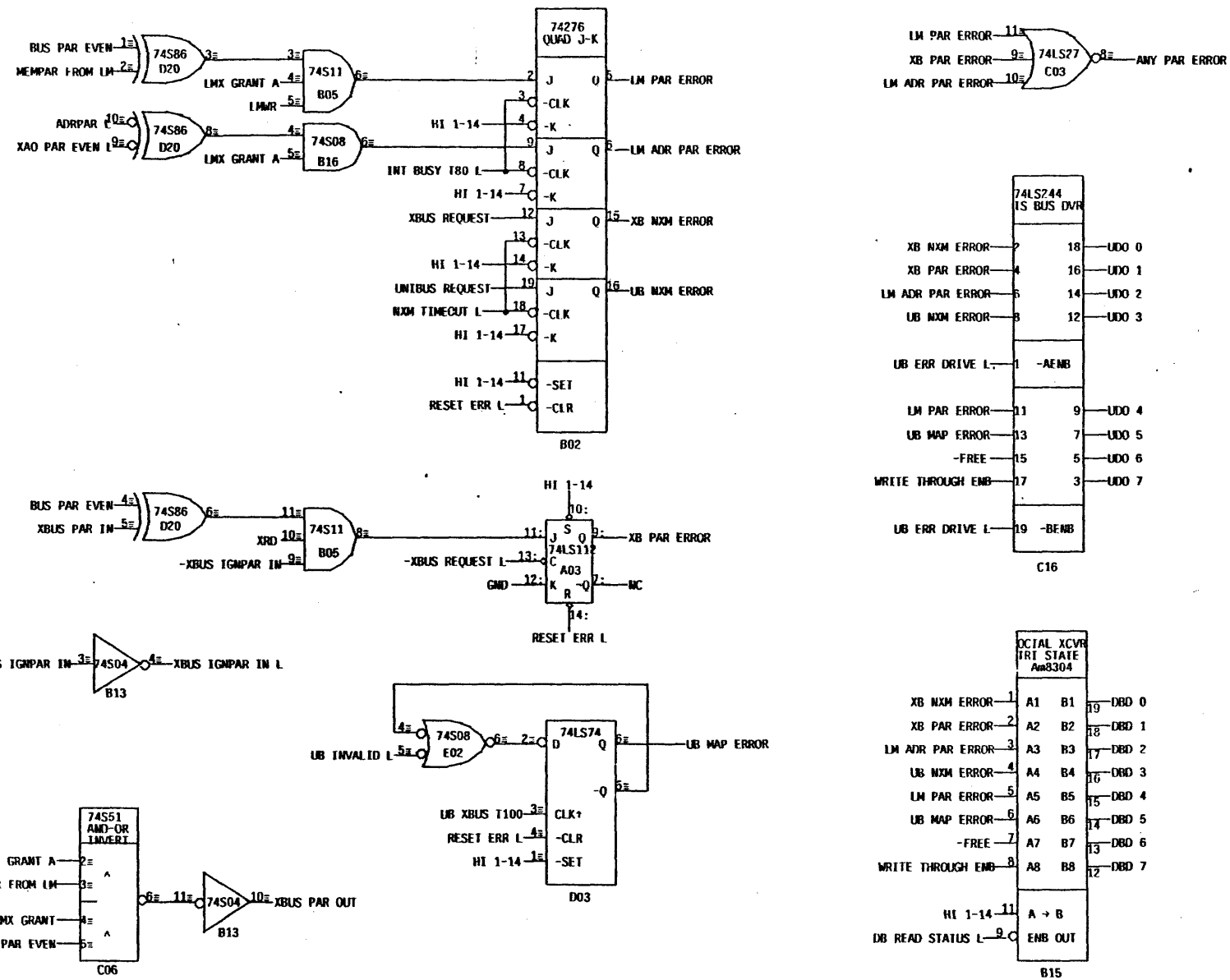


NOTE: MEMPAR TO LM is on DBGOUT

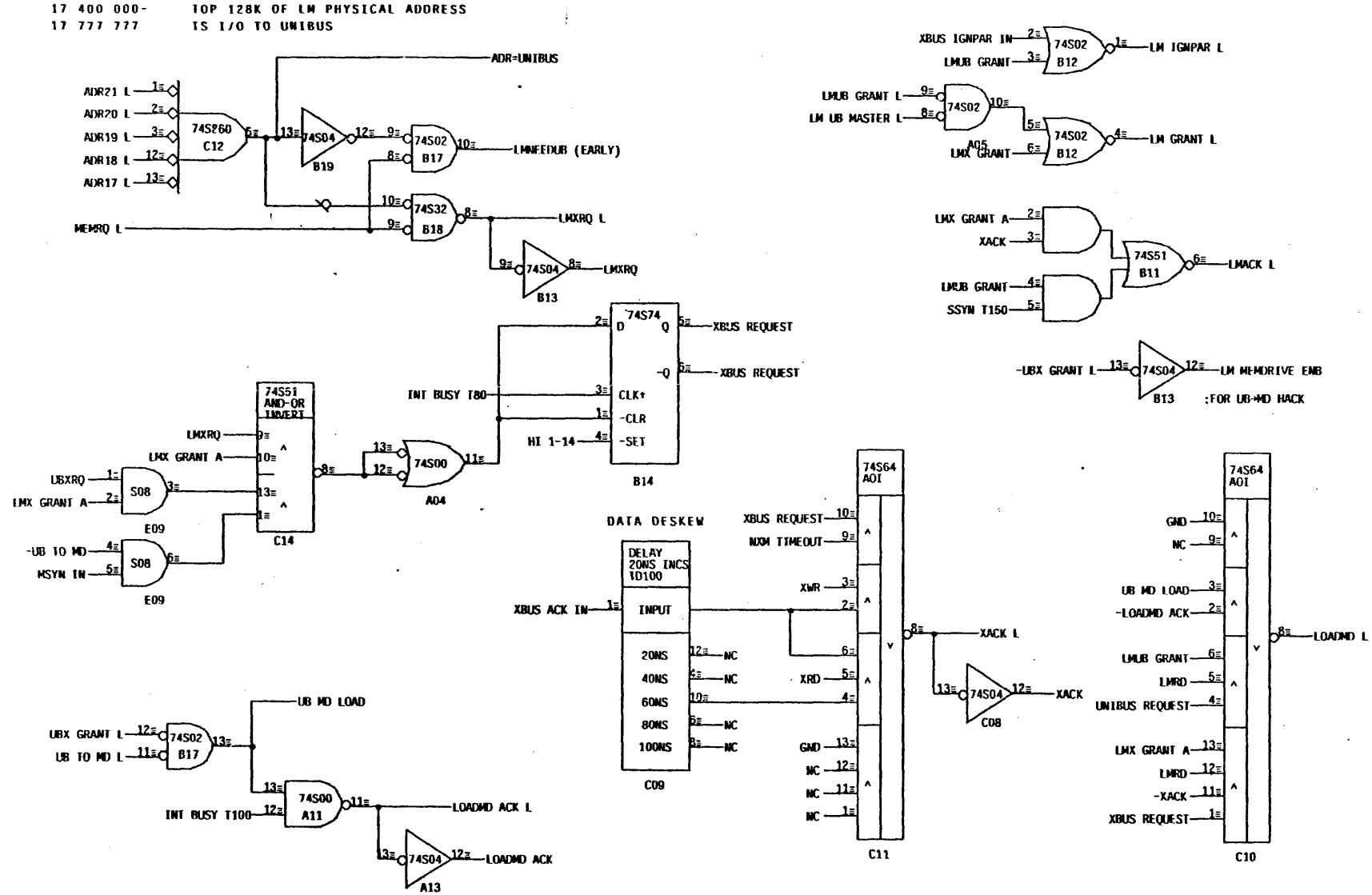
CBUS	PROCESSOR DATA XCVR	10-DEC-1980 10:27	AI: CADR1; LMDATA



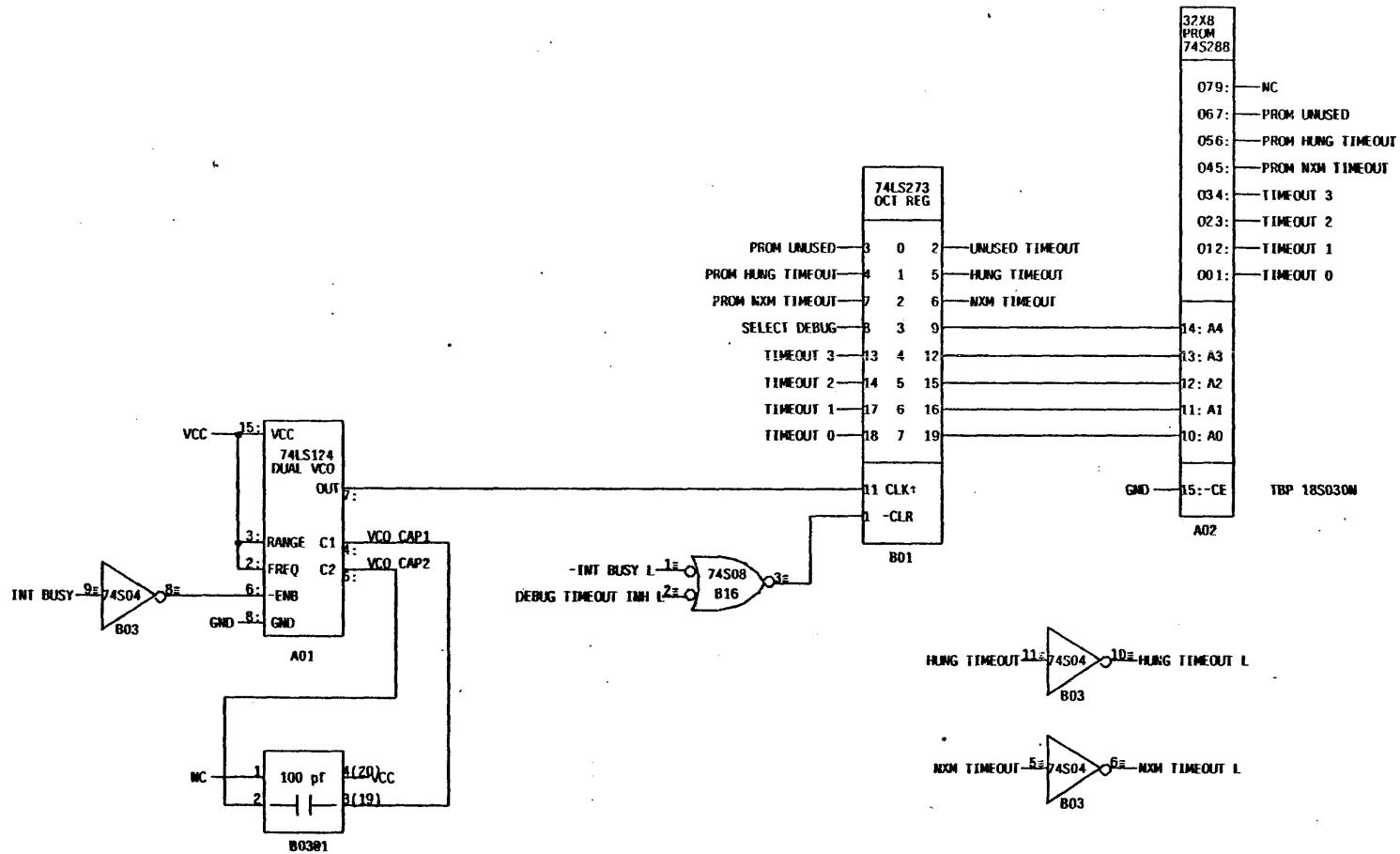
CBUS	READ BUFFER	10-DEC-1980 10:28	AI: CADR1; RBUF



CBUS	ERROR LOGIC	10-DEC-1980 10:40	AI: CADR1; REQERR



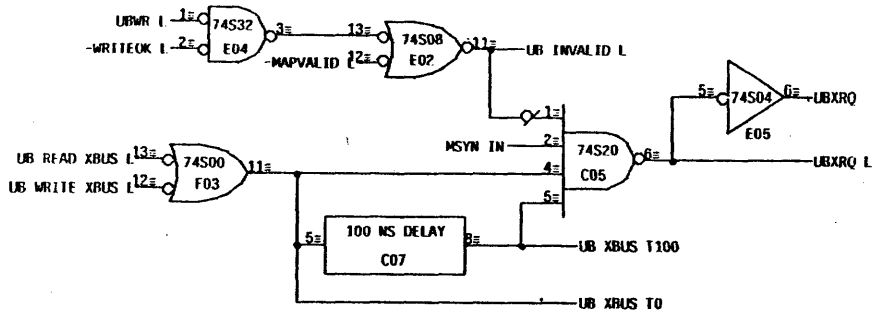
CBUS	XBUS REQ & ACK	10-DEC-1980 17:18	AI: CADR1; REQLM



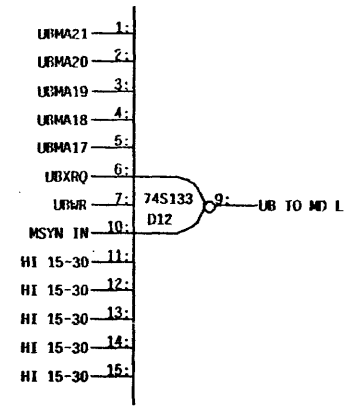
CBUS	XBUS & UNIBUS TIMEOUT	10-DEC-1980 15:26	AI: CADR1; REQTIM

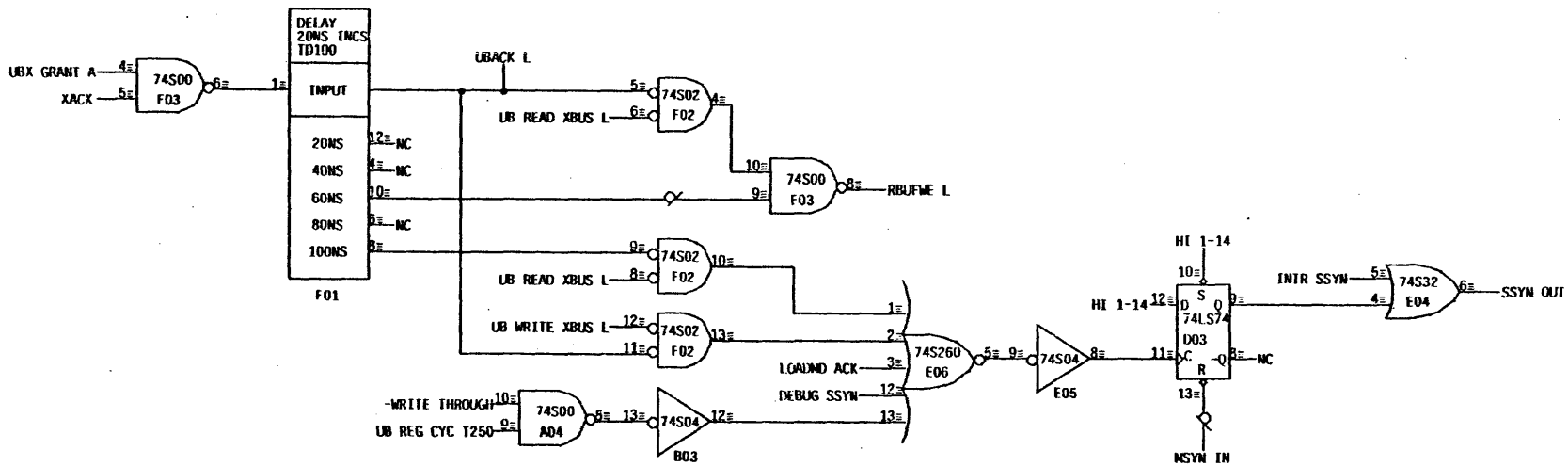
17 400 000 to
17 777 777

THESE ARE LM ADDRESSES THAT ARE MAPPED ONTO UNIBUS
THEY DON'T EXIST ON XBUS
THEREFORE THEY'LL MEAN UNIBUS TO MEMORY DATA REGISTER

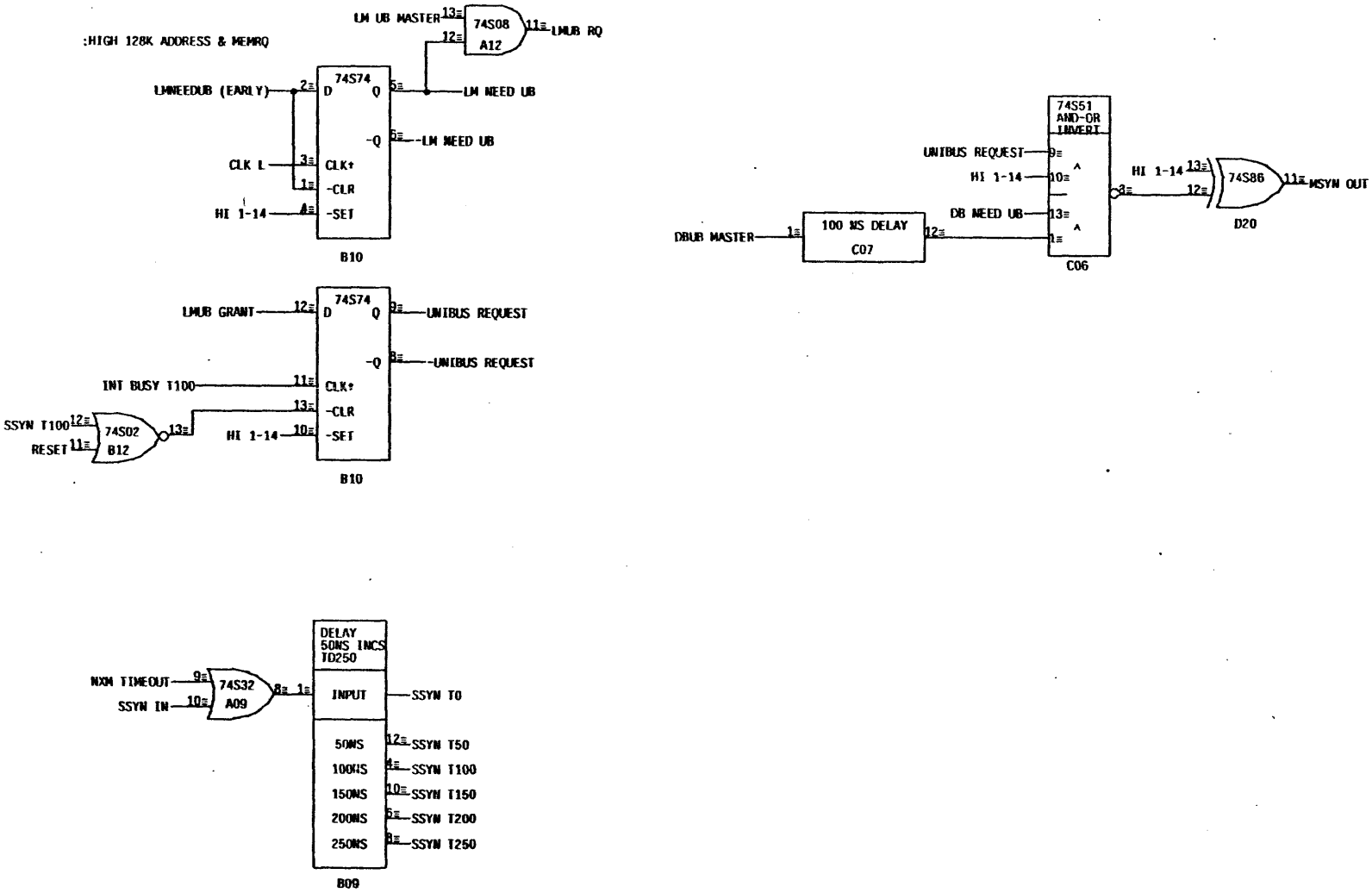


DELAY FOR MAPVALID

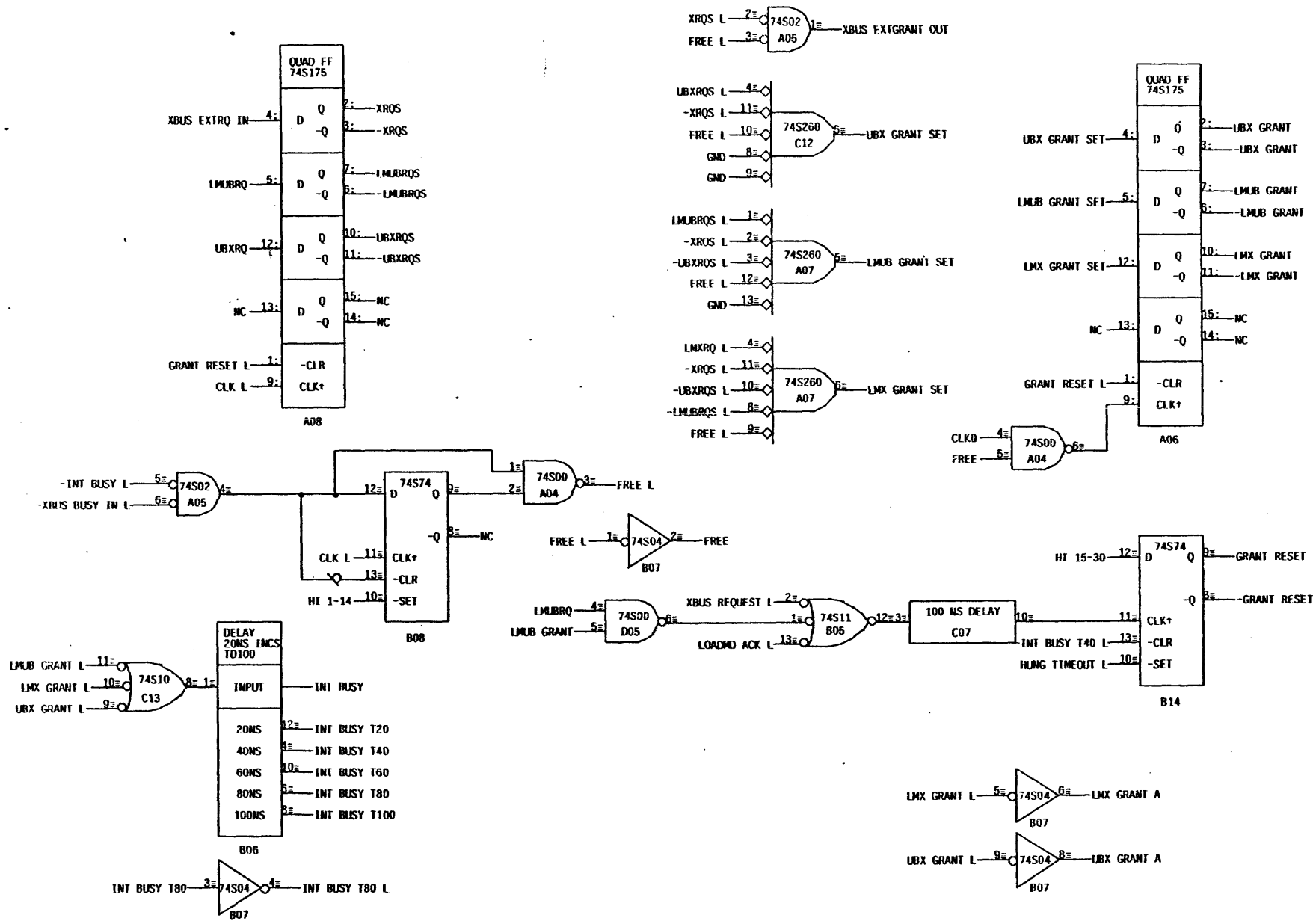




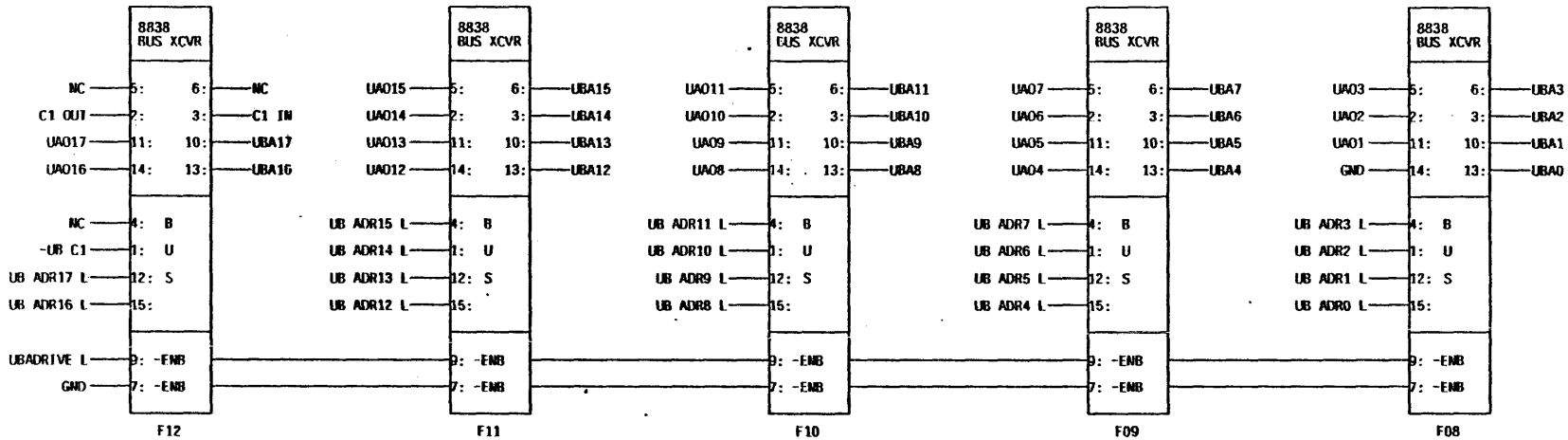
CBUS	XBUS REQUEST FROM UNIBUS	10-DEC-1980 15:36	AI: CADR1; REQU

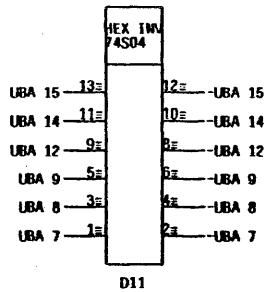


CBUS	LM & DEBUG TO UNIBUS	10-DEC-1980 15:23	AI: CADR1; REQUB

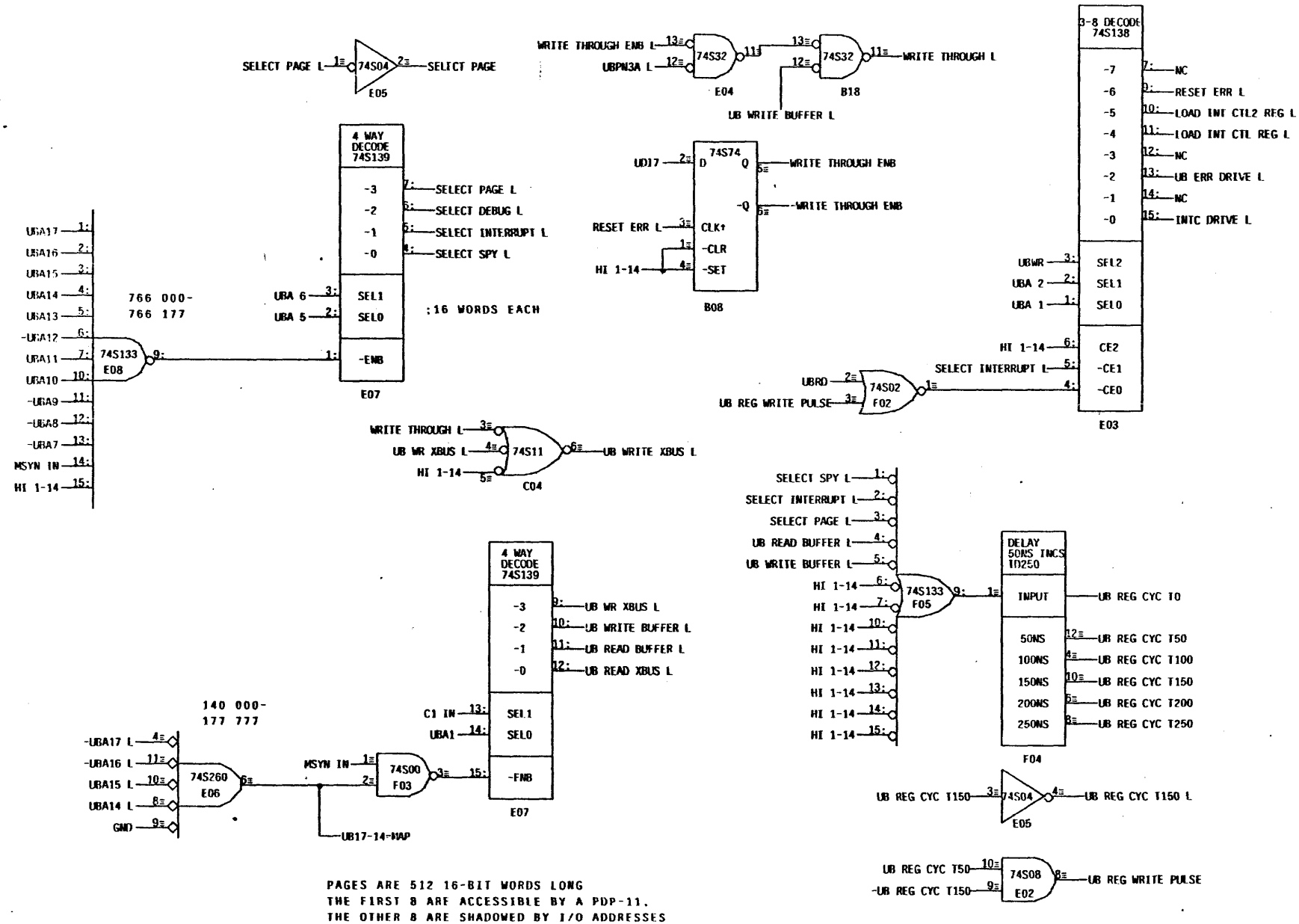


CBUS	REQUEST SYNCHRONIZER	10-DEC-1980 11:32	AI: CADR1; RQSYNC



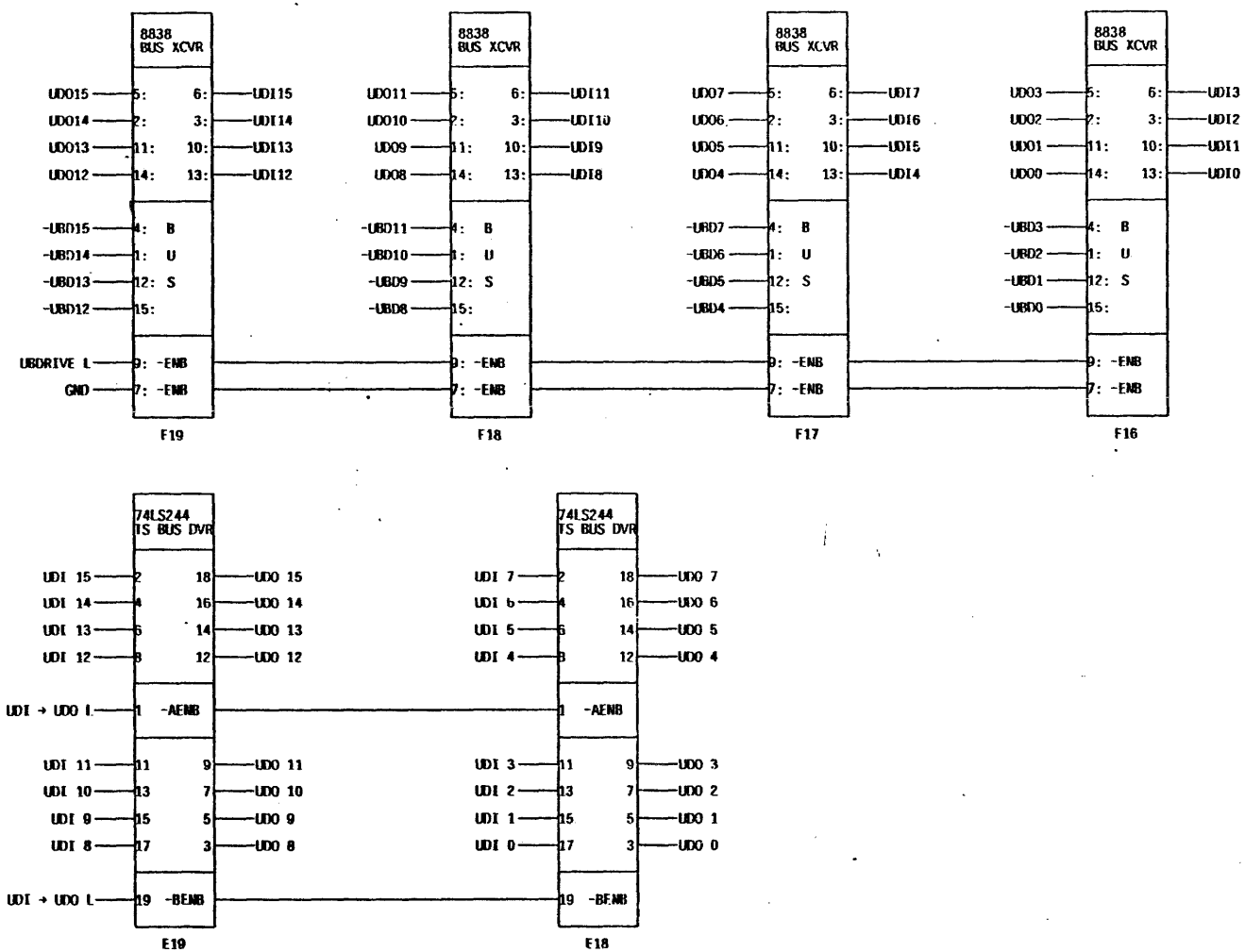


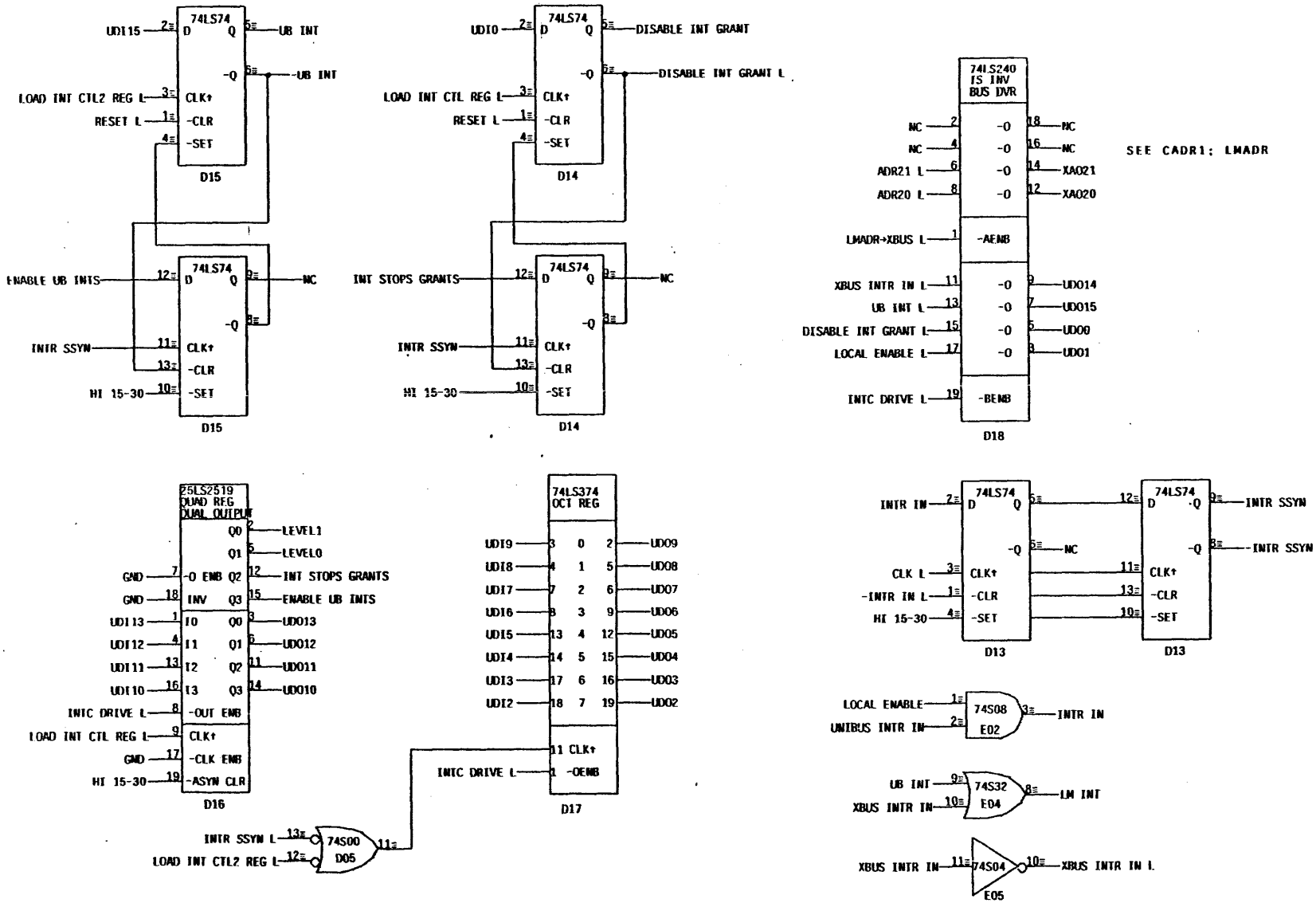
CBUS	UNIBUS ADDRESS TRANSCEIVERS	10-DEC-1980 11:32	AI: CADR1; UBA



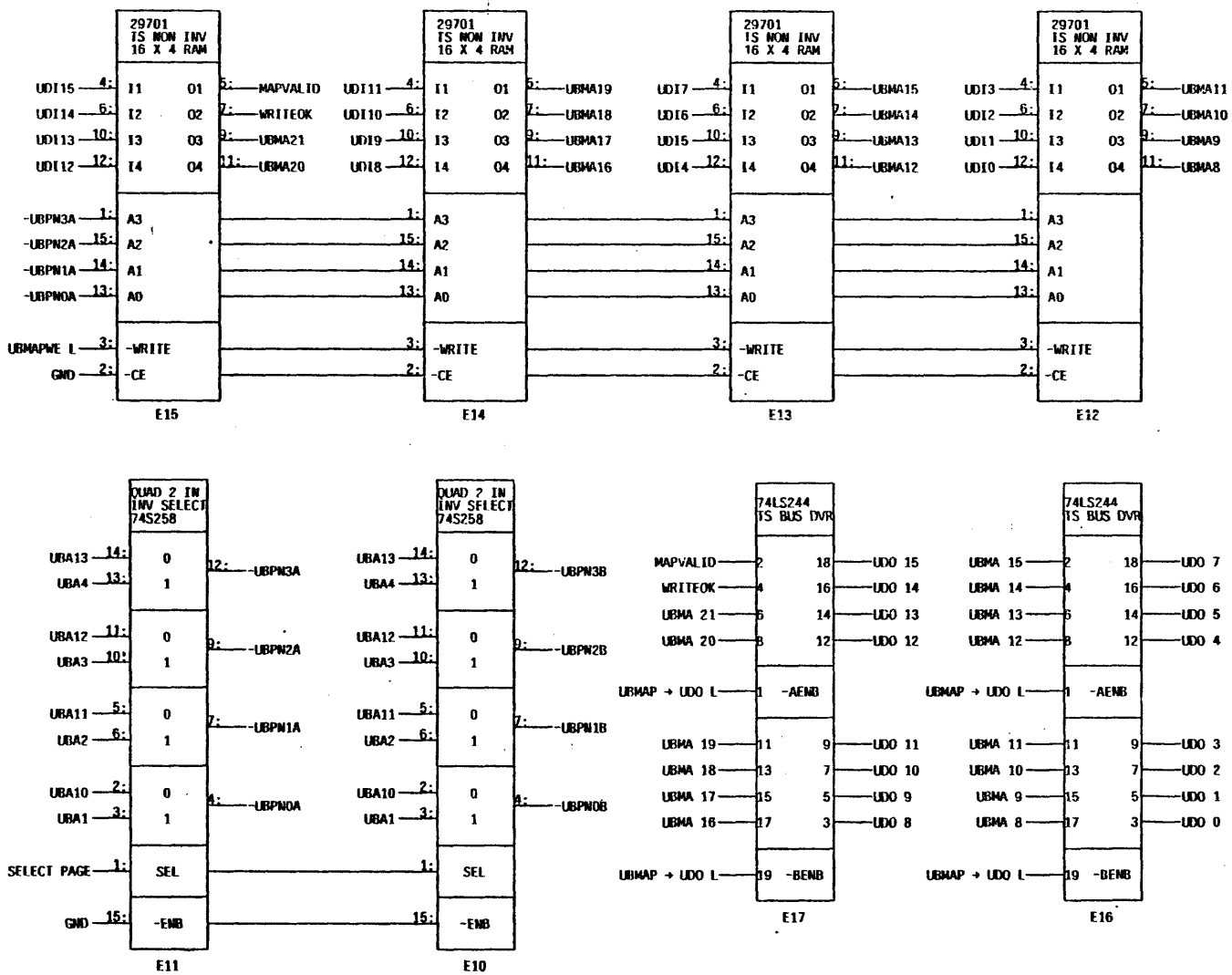
PAGES ARE 512 16-BIT WORDS LONG
THE FIRST 8 ARE ACCESSIBLE BY A PDP-11.
THE OTHER 8 ARE SHADOWED BY I/O ADDRESSES

CBUS	UNIBUS SLAVE RESPONSE	11-DEC-1980 14:57	AI: CADR1; UBCYC

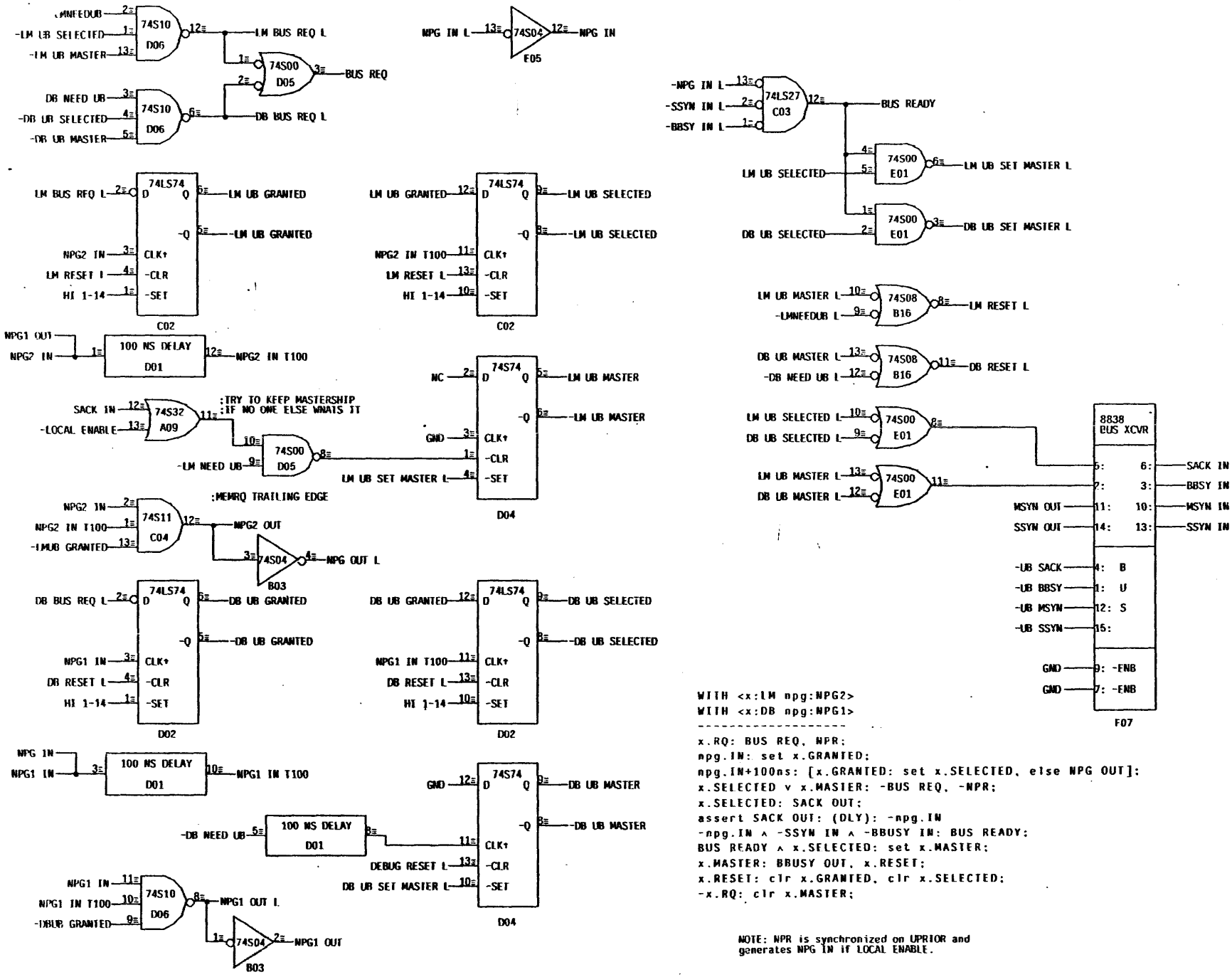

8838
BUS XCVR
UDO15
UDO14
UDO13
UDO12
UDI15
UDI14
UDI13
UDI12
-UBD15
-UBD14
-UBD13
-UBD12
UBDRIVE L
GND
F19
UDO11
UDO10
UDO9
UDO8
UDI11
UDI10
UDI9
UDI8
-UBD11
-UBD10
-UBD9
-UBD8
F18
UDO7
UDO6
UDO5
UDO4
UDI7
UDI6
UDI5
UDI4
-UBD7
-UBD6
-UBD5
-UBD4
F17
UDO3
UDO2
UDO1
UDO0
UDI3
UDI2
UDI1
UDI0
-UBD3
-UBD2
-UBD1
-UBD0
F16
74LS244
TS BUS DVR
UDI 15
UDI 14
UDI 13
UDI 12
UDO 15
UDO 14
UDO 13
UDO 12
UDI → UDO L
-AENB
UDI 11
UDI 10
UDI 9
UDI 8
UDO 11
UDO 10
UDO 9
UDO 8
-BENB
E19
UDI 7
UDI 6
UDI 5
UDI 4
UDO 7
UDO 6
UDO 5
UDO 4
UDI 3
UDI 2
UDI 1
UDI 0
UDO 3
UDO 2
UDO 1
UDO 0
E18



CBUS	UNIBUS INTERRUPT CONTROL	10-DEC-1980 11:34	AI: CADR1; UBINTC



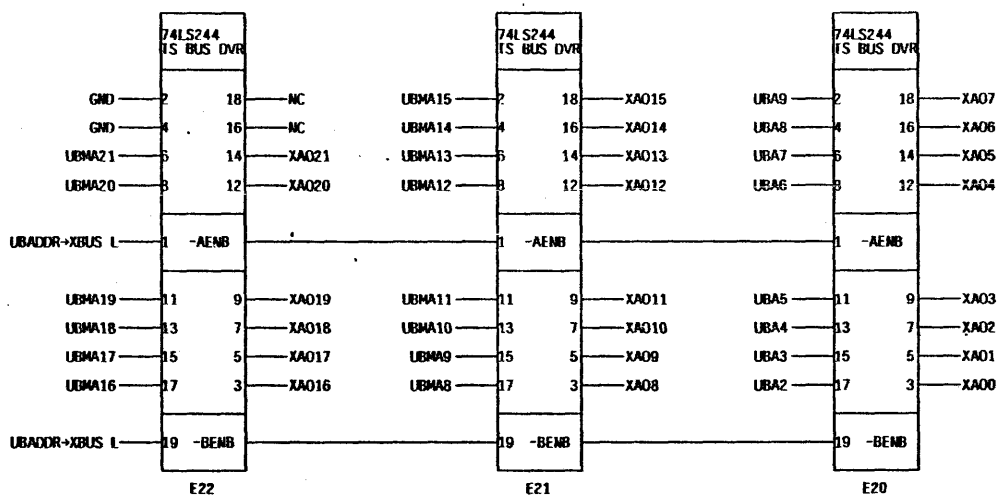
CBUS	UNIBUS MAP	10-DEC-1980 11:35	AI: CADR1; UBMAP



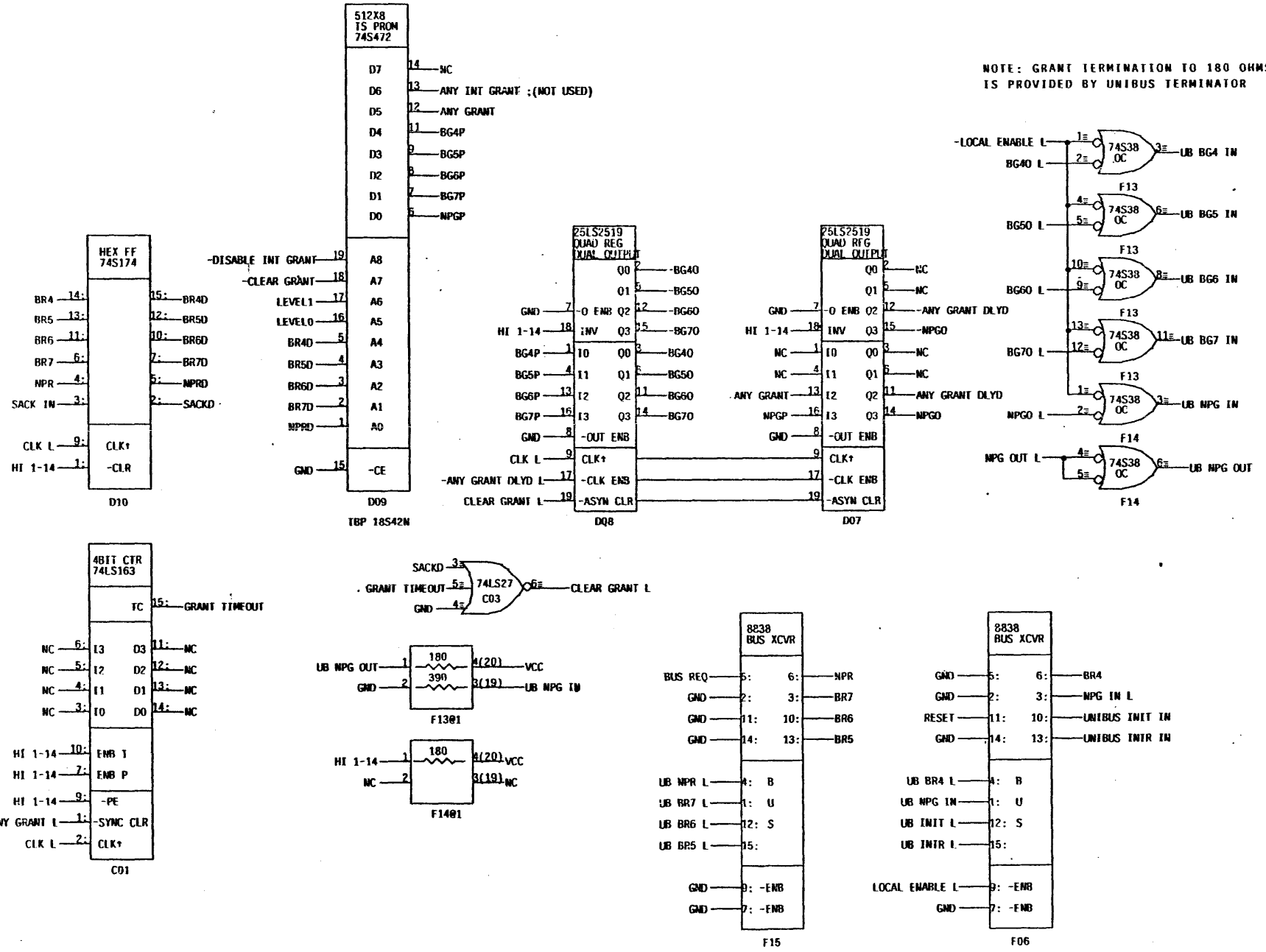

```
WITH <x:LM npg:NPG2>
WITH <x:DB npg:NPG1>
--------------------
x.RQ: BUS REQ, NPR;
npg.IN: set x.GRANTED;
npg.IN+100ns: [x.GRANTED: set x.SELECTED, else NPG OUT];
x.SELECTED v x.MASTER: -BUS REQ, -NPR;
x.SELECTED: SACK OUT;
assert SACK OUT: (DLY): -npg.IN
-npg.IN ∧ -SSYN IN ∧ -BBUSY IN: BUS READY;
BUS READY ∧ x.SELECTED: set x.MASTER;
x.MASTER: BBUSY OUT, x.RESET;
x.RESET: clr x.GRANTED, clr x.SELECTED;
-x.RQ: clr x.MASTER;
```

NOTE: NPR is synchronized on UPRIOR and generates NPG IN if LOCAL ENABLE.

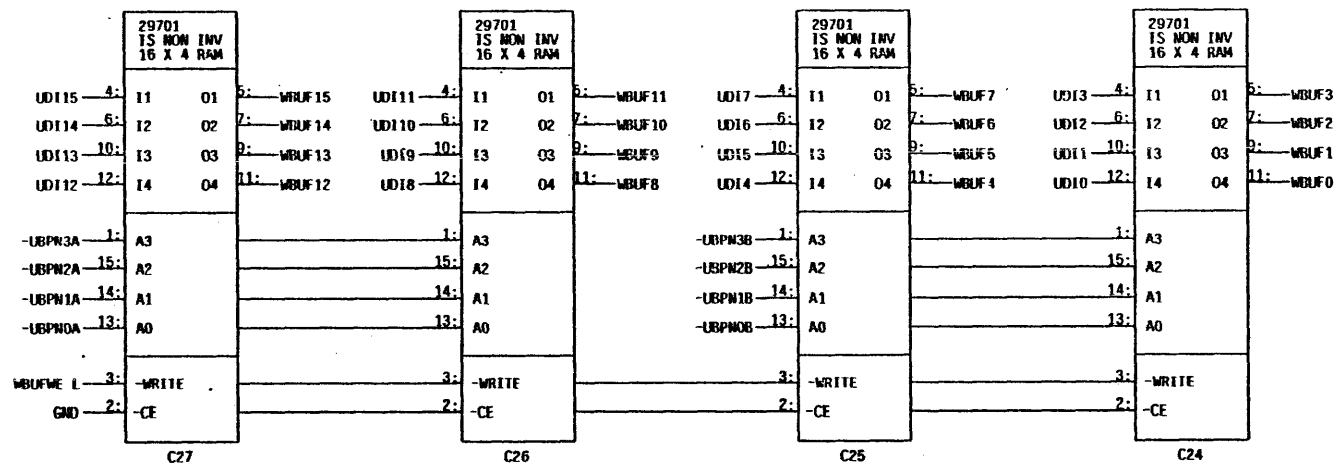
CBUS	UNIBUS MASTERSHIP	10-DEC-1980 13:21	AI: CADR1; UBMAST



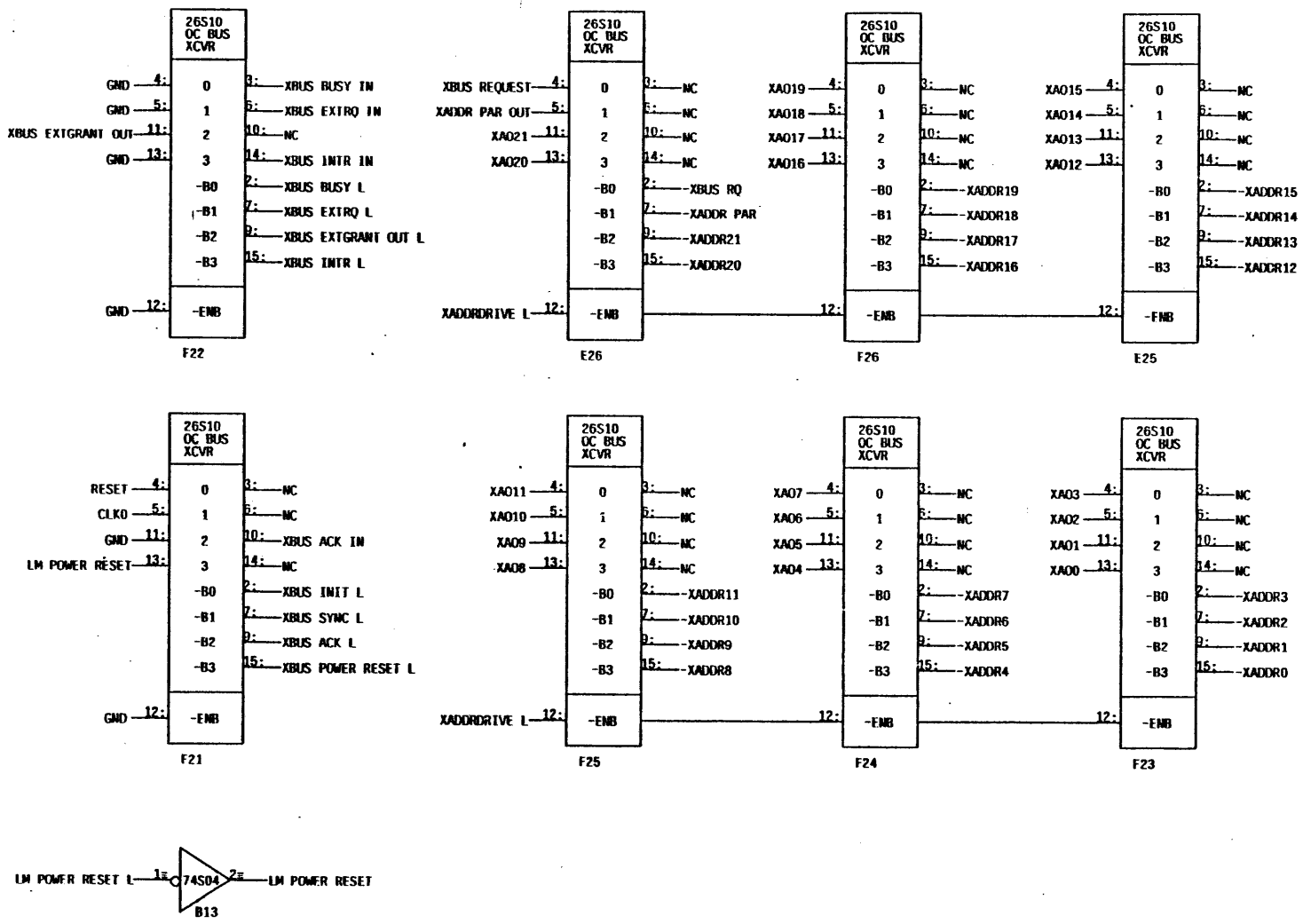
CBUS	UNIBUS ADDRESS TO XBUS	10-DEC-1980 11:36	AI: CADR1; UBXA

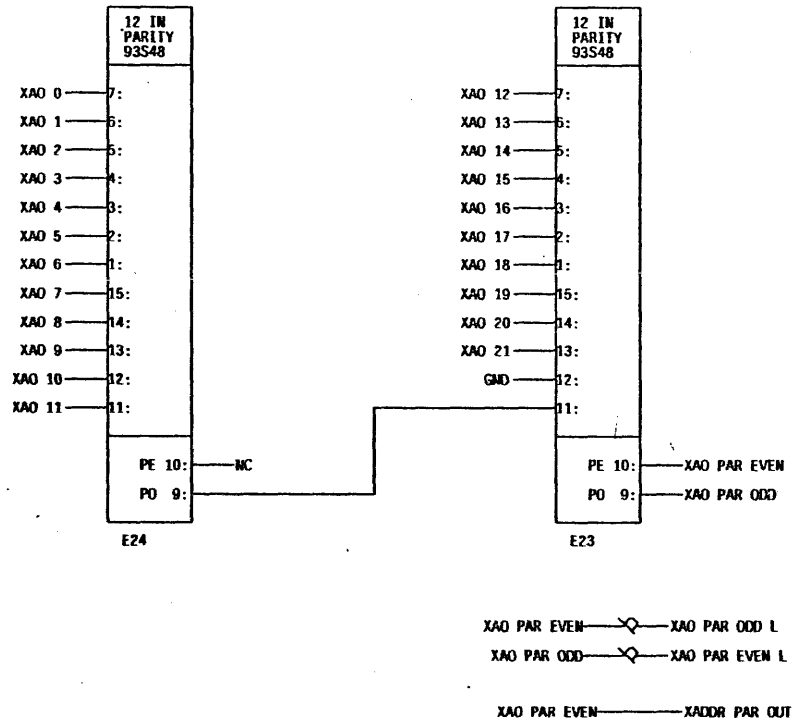


CBUS	UNIBUS BUS GRANT	10-DEC-1980 13:15	AI: CADR1; UPRIOR

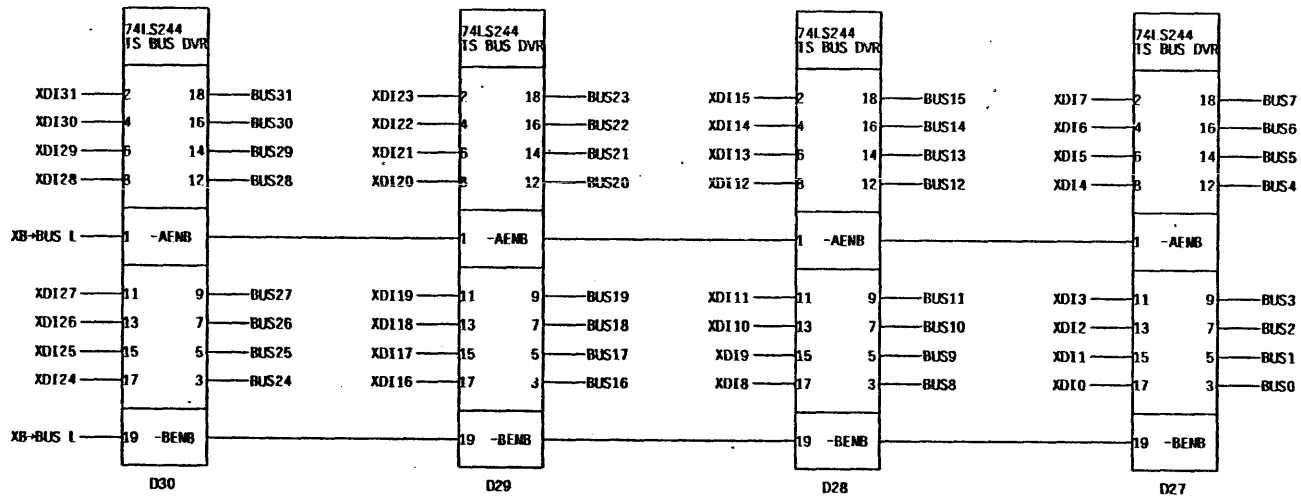


CBUS	WRITE BUFFER	10-DEC-1980 11:37	AI: CADR1; WBUF

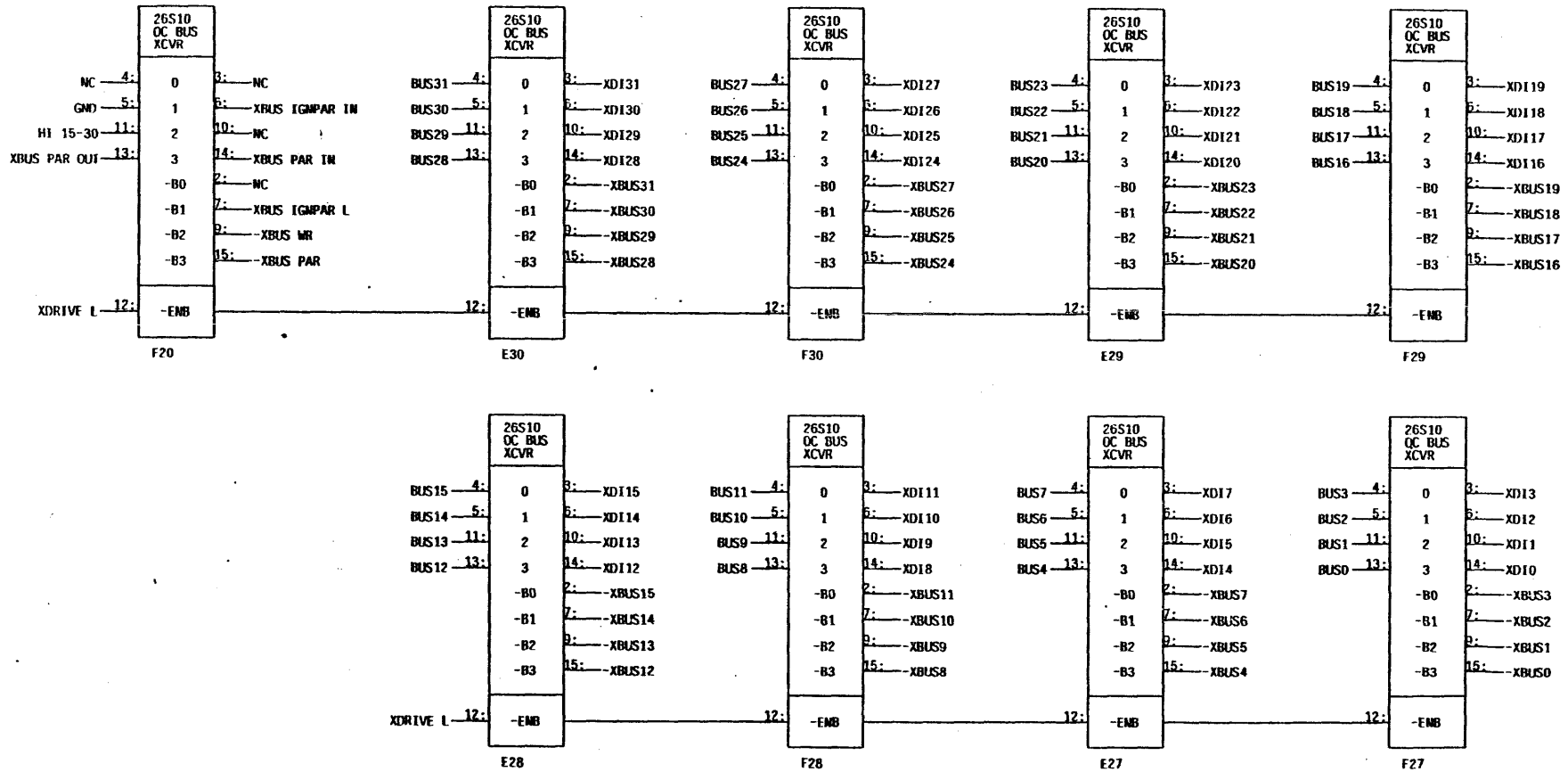

26S10
OC BUS
XCVR
GND 4:
GND 5:
XBUS EXTGRANT OUT 11:
GND 13:
0
1
2
3
-B0
-B1
-B2
-B3
-ENB
GND 12:
3: XBUS BUSY IN
6: XBUS EXTRQ IN
10: NC
14: XBUS INTR IN
2: XBUS BUSY L
7: XBUS EXTRQ L
9: XBUS EXTGRANT OUT L
15: XBUS INTR L
F22
XBUS REQUEST 4:
XADDR PAR OUT 5:
XA021 11:
XA020 13:
XADDRDRIVE L 12:
3: NC
6: NC
10: NC
14: NC
2: -XBUS RQ
7: -XADDR PAR
9: -XADDR21
15: -XADDR20
E26
XA019 4:
XA018 5:
XA017 11:
XA016 13:
3: NC
6: NC
10: NC
14: NC
2: -XADDR19
7: -XADDR18
9: -XADDR17
15: -XADDR16
F26
XA015 4:
XA014 5:
XA013 11:
XA012 13:
3: NC
6: NC
10: NC
14: NC
2: -XADDR15
7: -XADDR14
9: -XADDR13
15: -XADDR12
E25
RESET 4:
CLK0 5:
GND 11:
LM POWER RESET 13:
3: NC
6: NC
10: XBUS ACK IN
14: NC
2: XBUS INIT L
7: XBUS SYNC L
9: XBUS ACK L
15: XBUS POWER RESET L
F21
XA011 4:
XA010 5:
XA09 11:
XA08 13:
3: NC
6: NC
10: NC
14: NC
2: -XADDR11
7: -XADDR10
9: -XADDR9
15: -XADDR8
F25
XA07 4:
XA06 5:
XA05 11:
XA04 13:
3: NC
6: NC
10: NC
14: NC
2: -XADDR7
7: -XADDR6
9: -XADDR5
15: -XADDR4
F24
XA03 4:
XA02 5:
XA01 11:
XA00 13:
3: NC
6: NC
10: NC
14: NC
2: -XADDR3
7: -XADDR2
9: -XADDR1
15: -XADDR0
F23
LM POWER RESET L 1
74S04
2 LM POWER RESET
B13



CBUS	XBUS ADDRESS PARITY	10-DEC-1980 11:49	AI: CADR1; XAPAR



CBUS	XBUS TO BUS	10-DEC-1980 16:06	AI: CADR1; XBD



CBUS	XBUS DATA TRANSCEIVERS	10-DEC-1980 11:50	AI: CADR1; XD