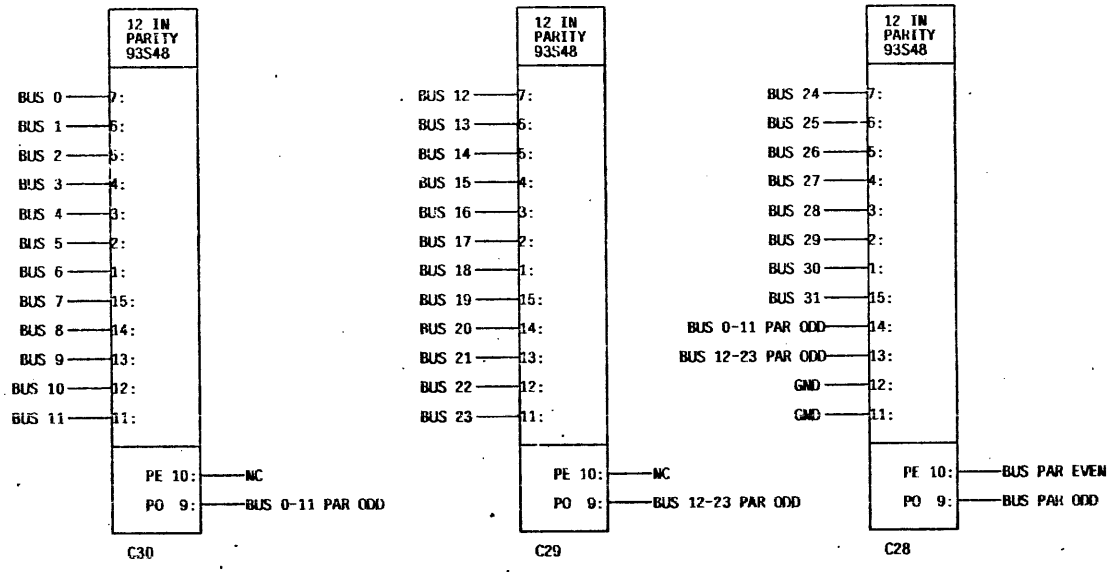
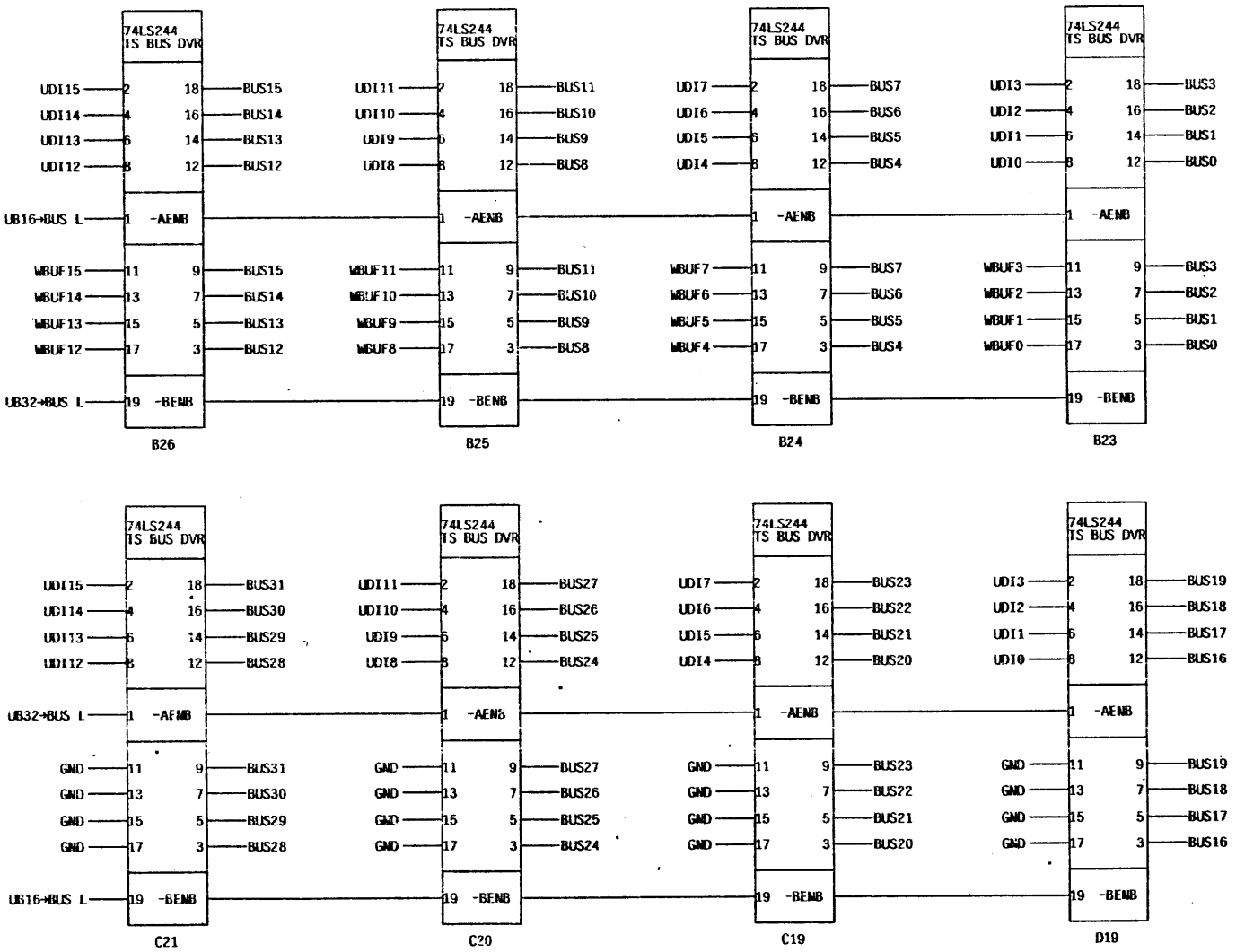
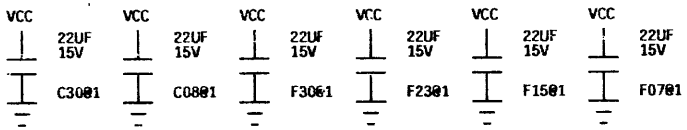
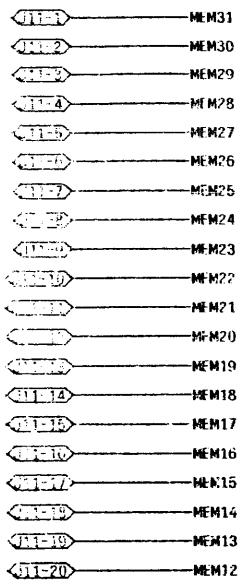

12 IN PARITY 93S48
BUS 0
BUS 1
BUS 2
BUS 3
BUS 4
BUS 5
BUS 6
BUS 7
BUS 8
BUS 9
BUS 10
BUS 11
7:
6:
5:
4:
3:
2:
1:
15:
14:
13:
12:
11:
PE 10:
PO 9:
NC
BUS 0-11 PAR ODD
C30
12 IN PARITY 93S48
BUS 12
BUS 13
BUS 14
BUS 15
BUS 16
BUS 17
BUS 18
BUS 19
BUS 20
BUS 21
BUS 22
BUS 23
7:
6:
5:
4:
3:
2:
1:
15:
14:
13:
12:
11:
PE 10:
PO 9:
NC
BUS 12-23 PAR ODD
C29
12 IN PARITY 93S48
BUS 24
BUS 25
BUS 26
BUS 27
BUS 28
BUS 29
BUS 30
BUS 31
BUS 0-11 PAR ODD
BUS 12-23 PAR ODD
GND
GND
7:
6:
5:
4:
3:
2:
1:
15:
14:
13:
12:
11:
PE 10:
PO 9:
BUS PAR EVEN
BUS PAR ODD
C28



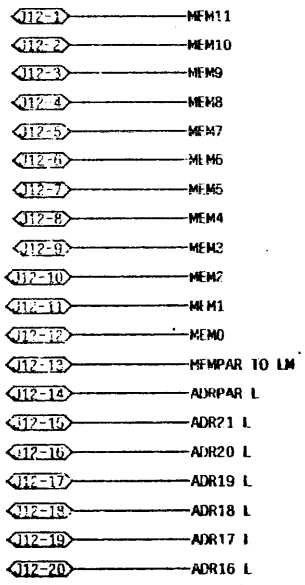
CBUS	BUS FROM UNIBUS	10-DEC-1980 10:05	AI: CADR1; BUSSEL



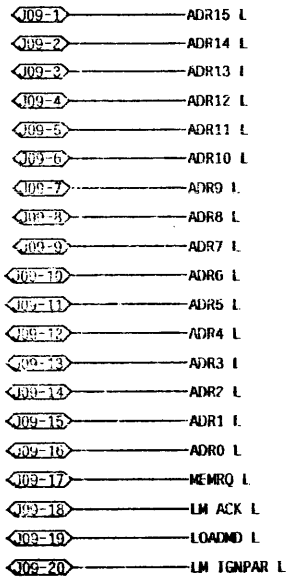
CBUS	BYPASS CAPACITORS	10-DEC-1980 10:06	AI: CADR1; CAPS



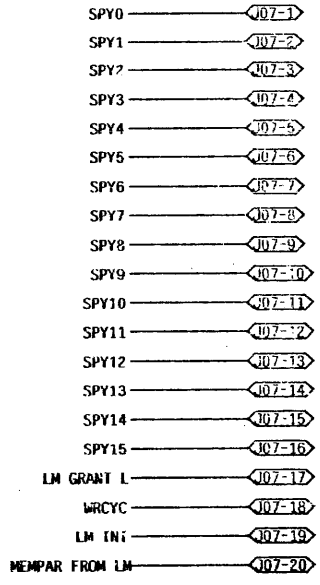
CADR; BCPINS
to 1AJ1



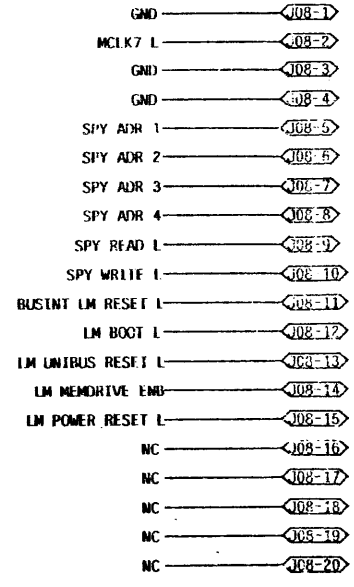
CADR; BCPINS
to 1BJ1



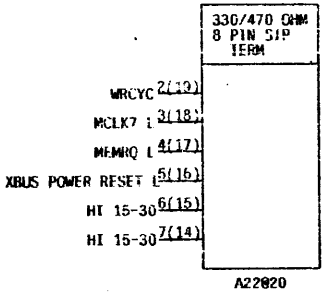
CADR; BCPINS
to 1CJ1

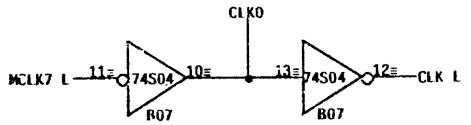


TO 3AJ1
CADR; BCPINS

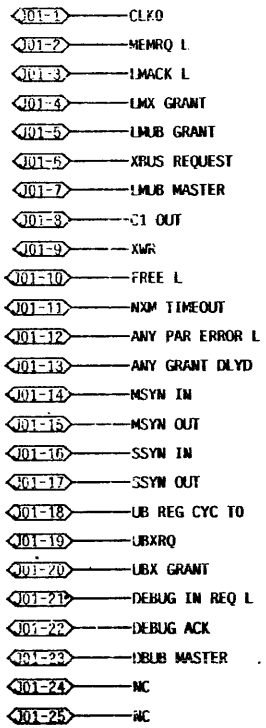


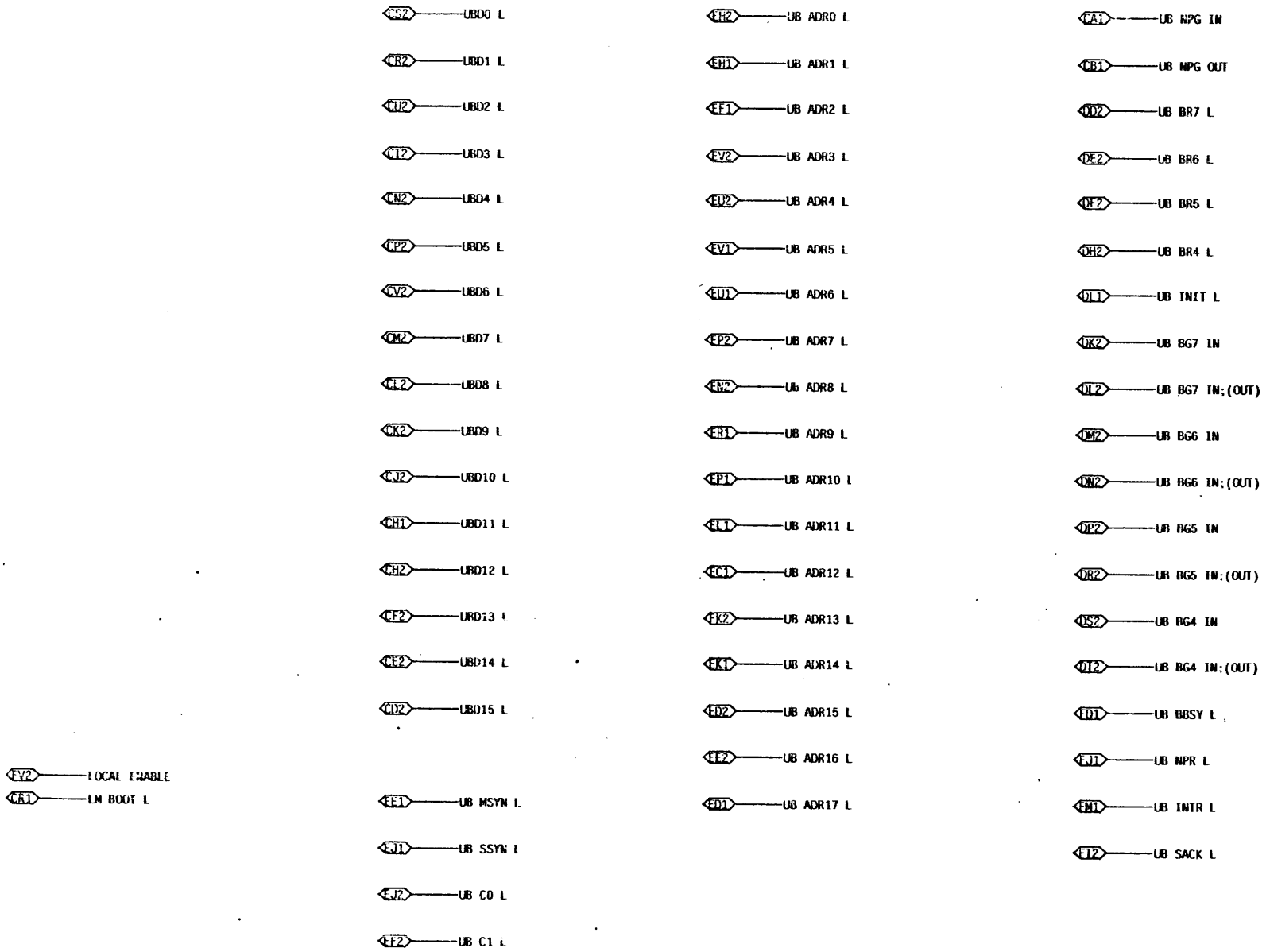
TO 5AJ1
CADR; MBCPIN



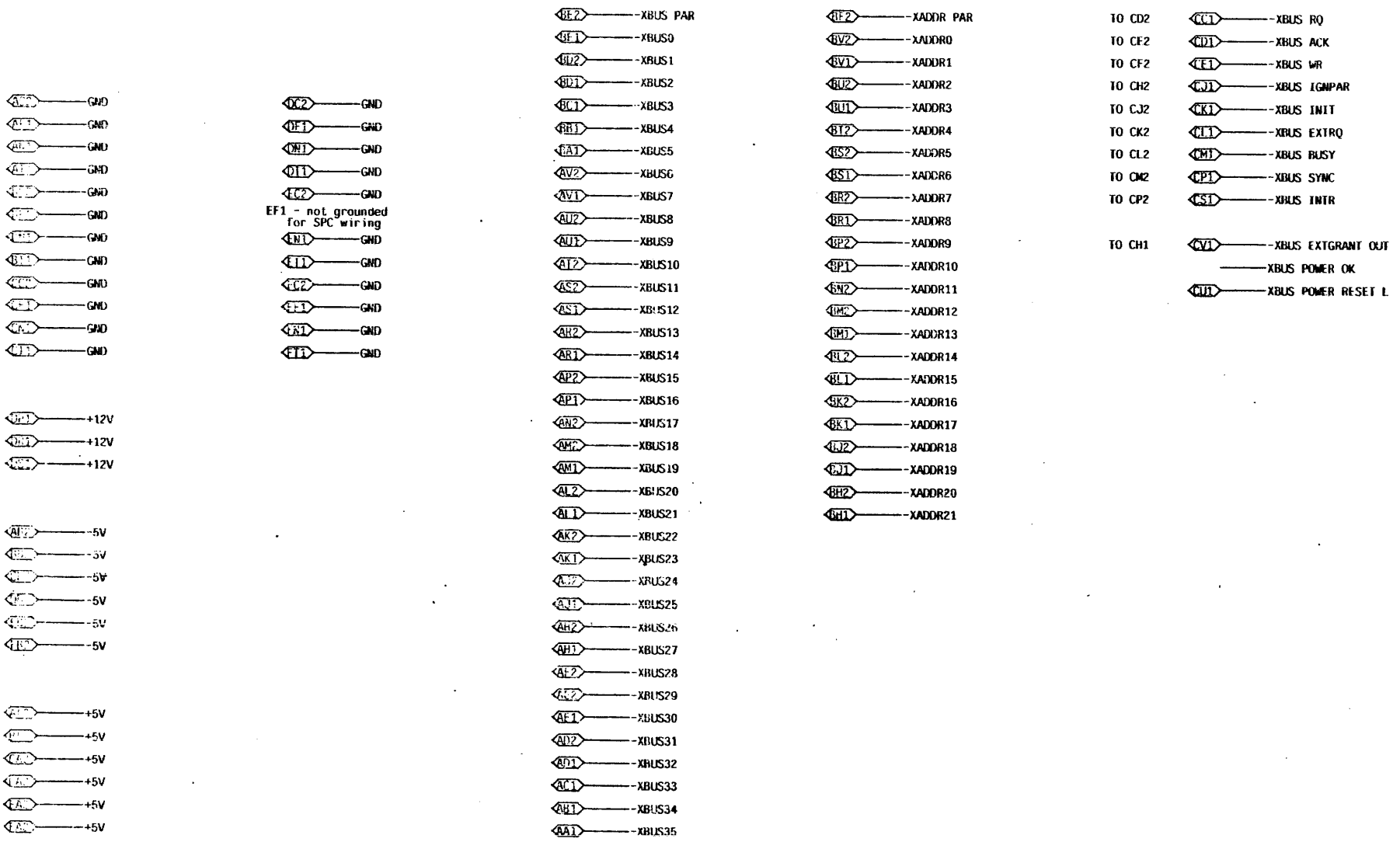


CBUS	CABLES TO PROCESSOR	10-DEC-1980 10:04	AI: CADR1; CLM

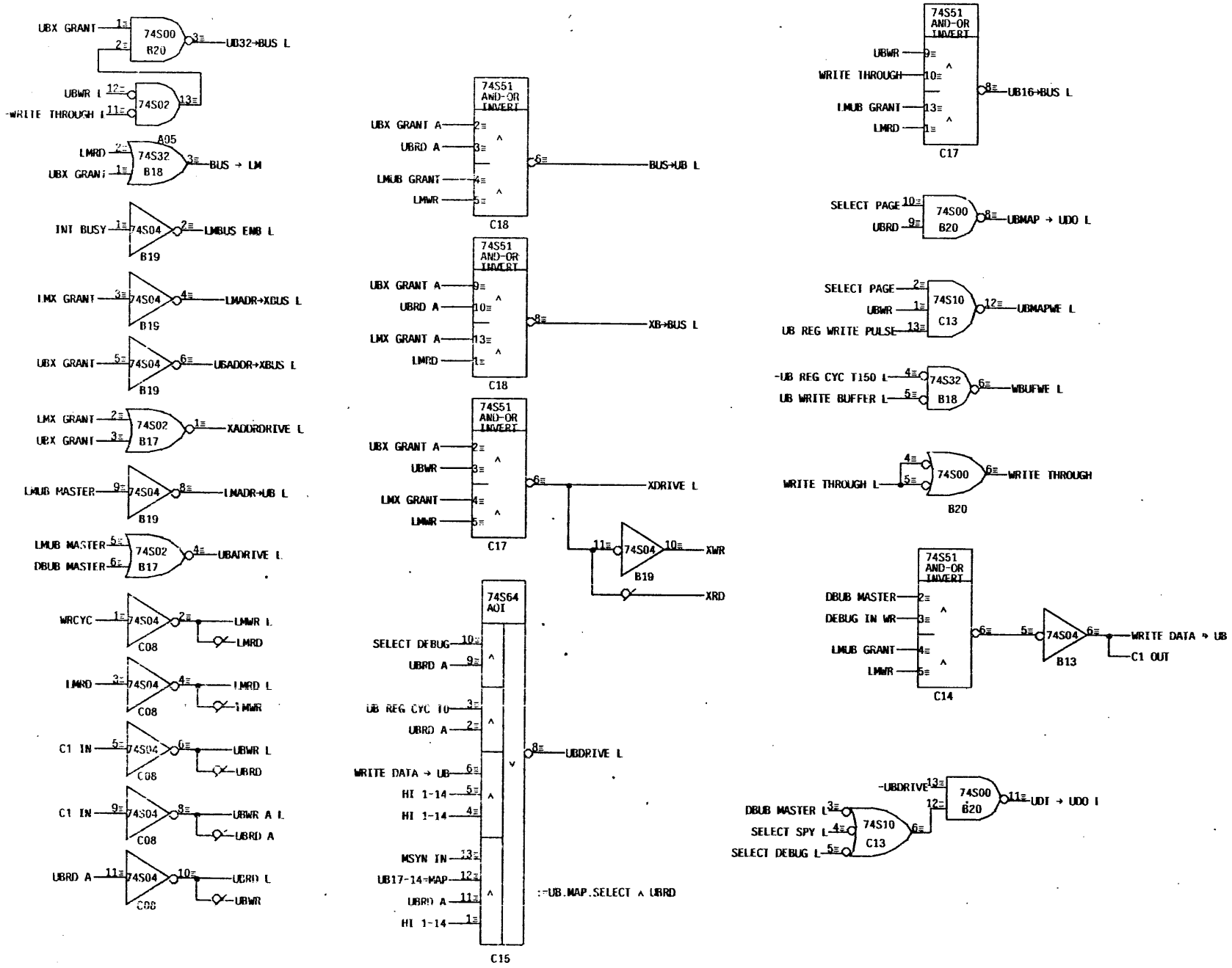

J01-1
CLKO
J01-2
MEMRQ L
J01-3
LMACK L
J01-4
LMX GRANT
J01-5
LMUB GRANT
J01-6
XBUS REQUEST
J01-7
LMUB MASTER
J01-8
C1 OUT
J01-9
XWR
J01-10
FREE L
J01-11
NXM TIMEOUT
J01-12
ANY PAR ERROR L
J01-13
ANY GRANT DLYD
J01-14
MSYN IN
J01-15
MSYN OUT
J01-16
SSYN IN
J01-17
SSYN OUT
J01-18
UB REG CYC TO
J01-19
UBXRQ
J01-20
UBX GRANT
J01-21
DEBUG IN REQ L
J01-22
DEBUG ACK
J01-23
DBUB MASTER
J01-24
NC
J01-25
NC



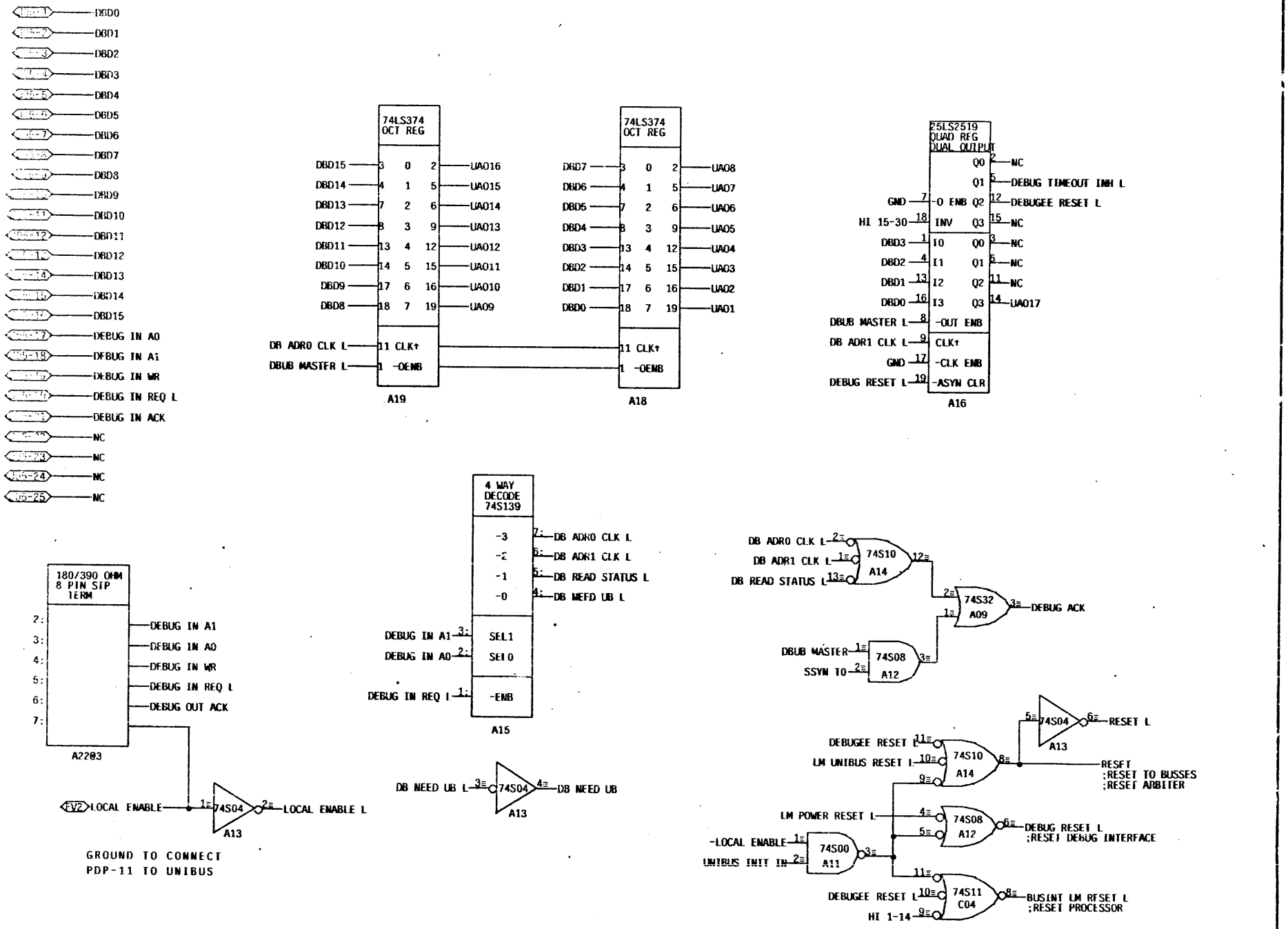
CBUS	UNIBUS SPC CONNS	3-OCT-1978 07:16	AI: CADR1; CUBUS



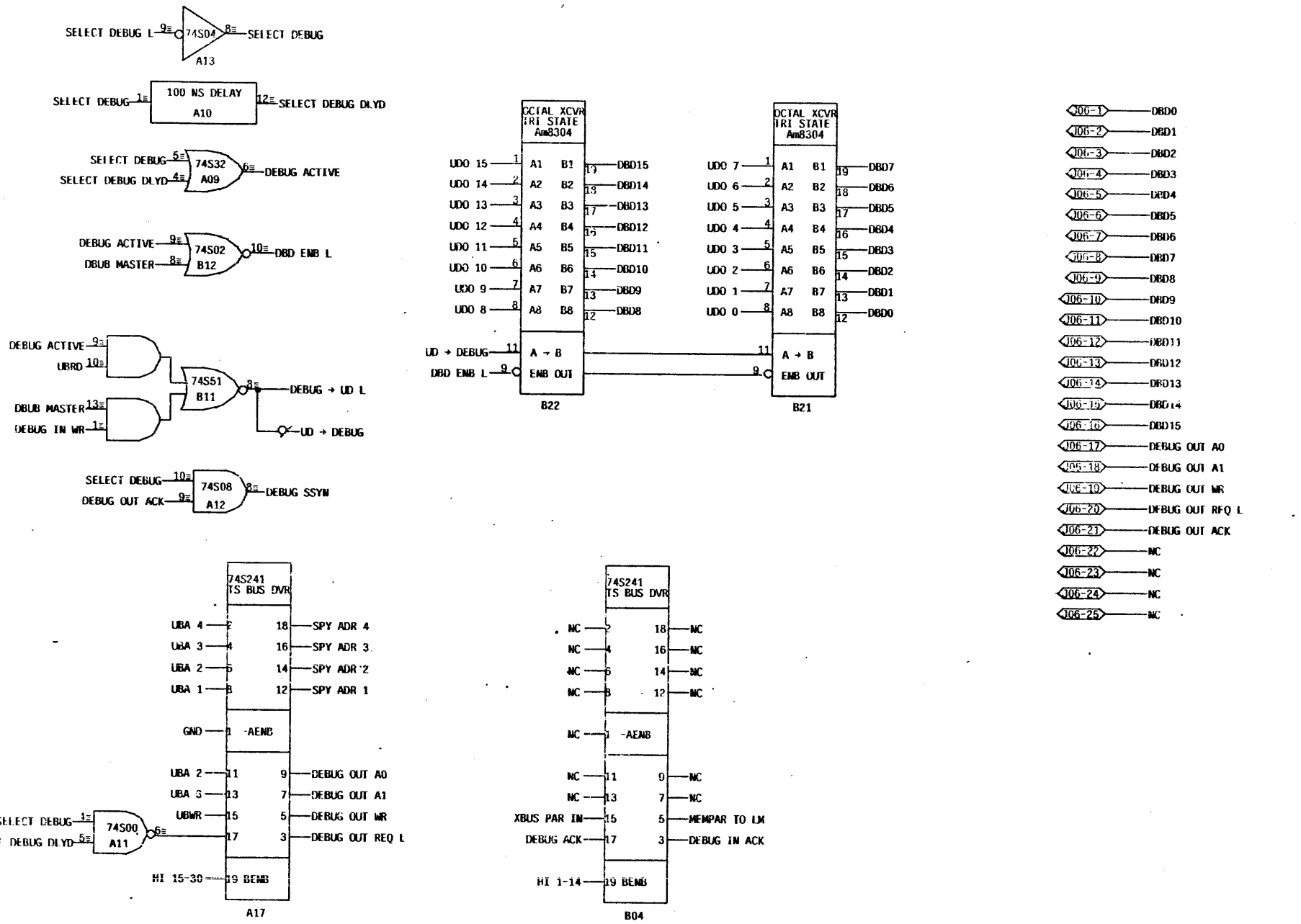
CBUS	XBUS BACKPLANE CONNS	10-DEC-1980 10:09	AI: CADR1; CXBUS



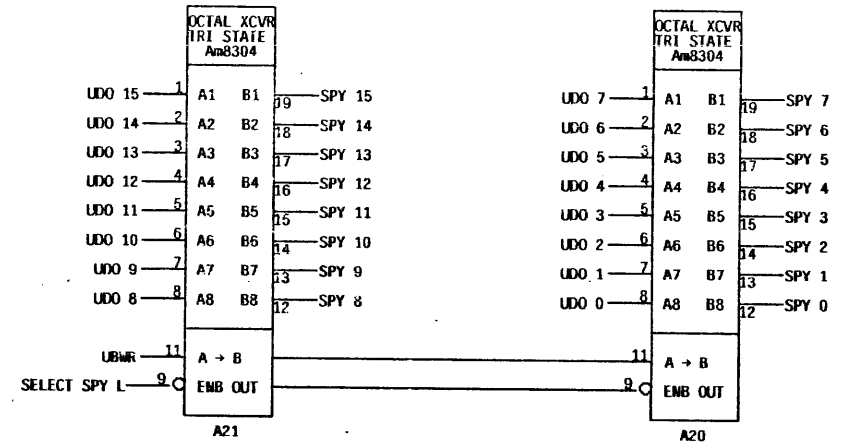
CBUS	DATA PATH CONTROL	10-DEC-1980 17:33	AI: CADR1; DATCTL

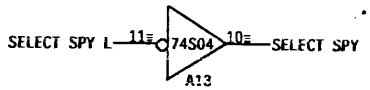


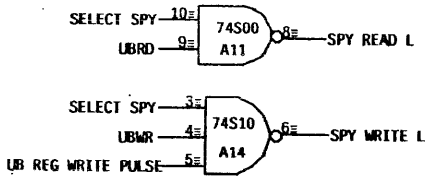
CBUS	DEBUGEE DATA PATH	10-DEC-1980 10:25	AI: CADR1; DBGIN

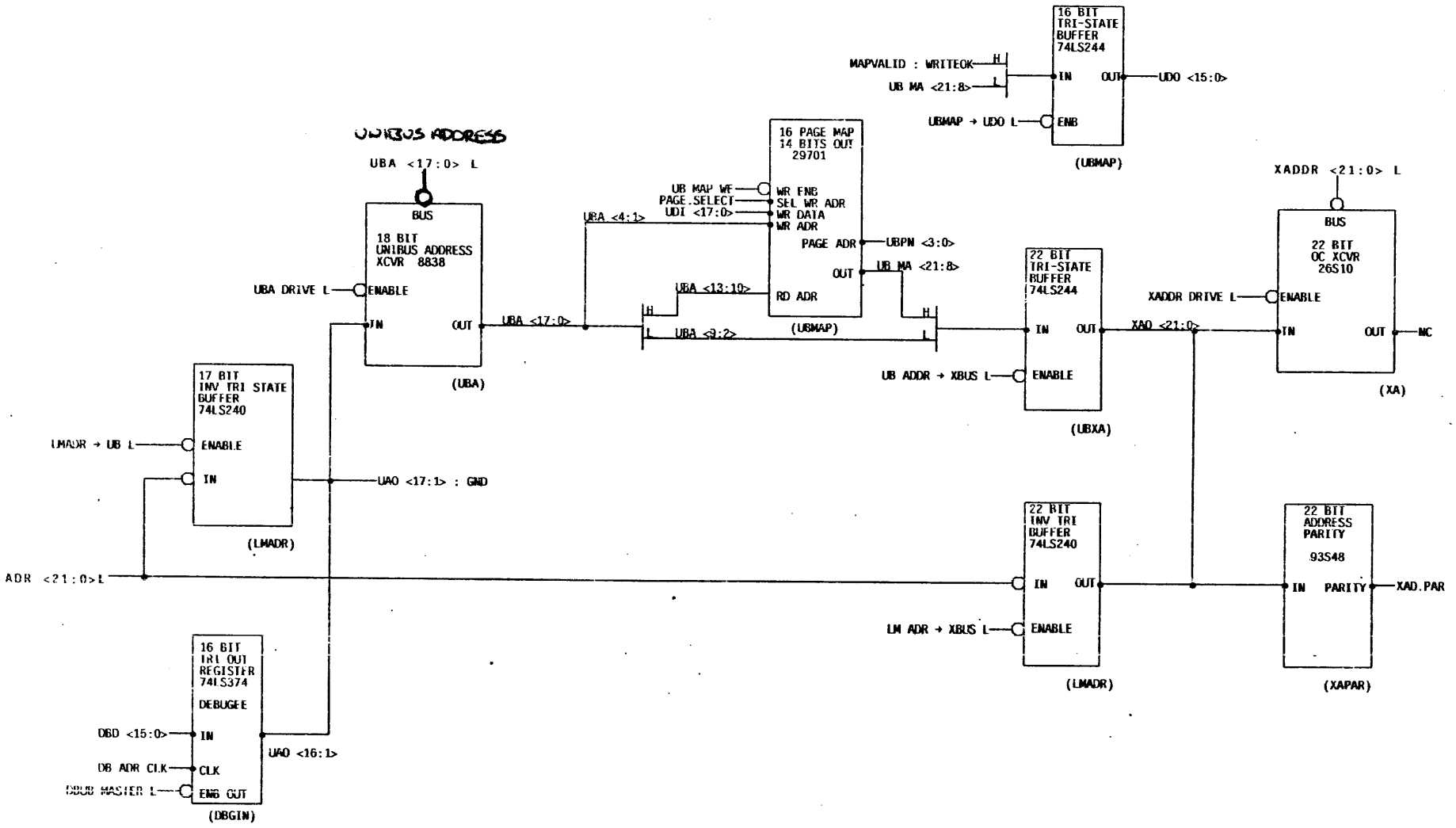


CBUS	DEBUGER DATA PATH	10-DEC-1980 10:26	AI: CADR1; DBGOUT

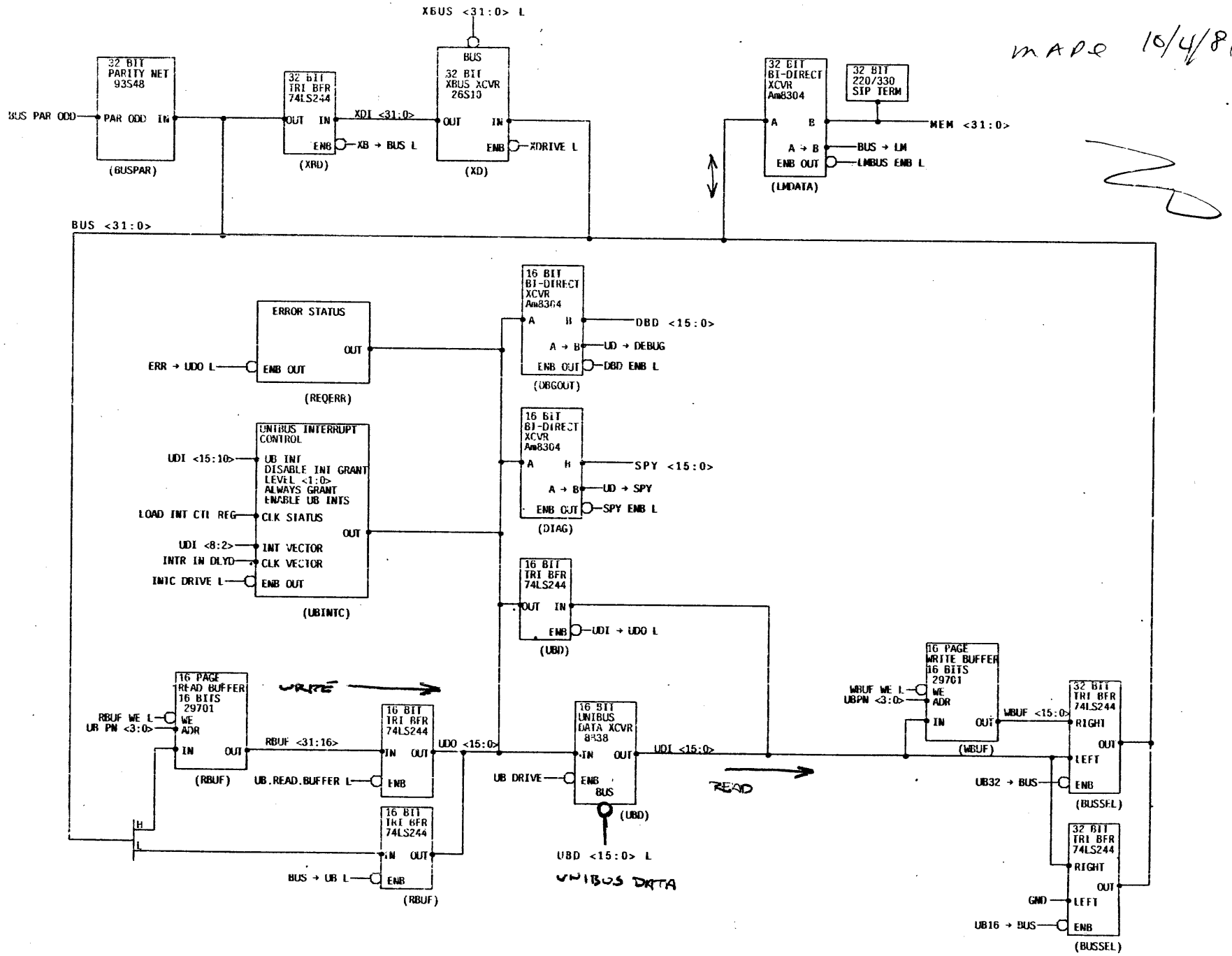

OCTAL XCVR
TRI STATE
Am8304
UDO 15
UDO 14
UDO 13
UDO 12
UDO 11
UDO 10
UDO 9
UDO 8
A1
A2
A3
A4
A5
A6
A7
A8
B1
B2
B3
B4
B5
B6
B7
B8
SPY 15
SPY 14
SPY 13
SPY 12
SPY 11
SPY 10
SPY 9
SPY 8
UBWR
SELECT SPY L
A → B
ENB OUT
A21
OCTAL XCVR
TRI STATE
Am8304
UDO 7
UDO 6
UDO 5
UDO 4
UDO 3
UDO 2
UDO 1
UDO 0
SPY 7
SPY 6
SPY 5
SPY 4
SPY 3
SPY 2
SPY 1
SPY 0
A → B
ENB OUT
A20


SELECT SPY L
74S04
SELECT SPY
A13

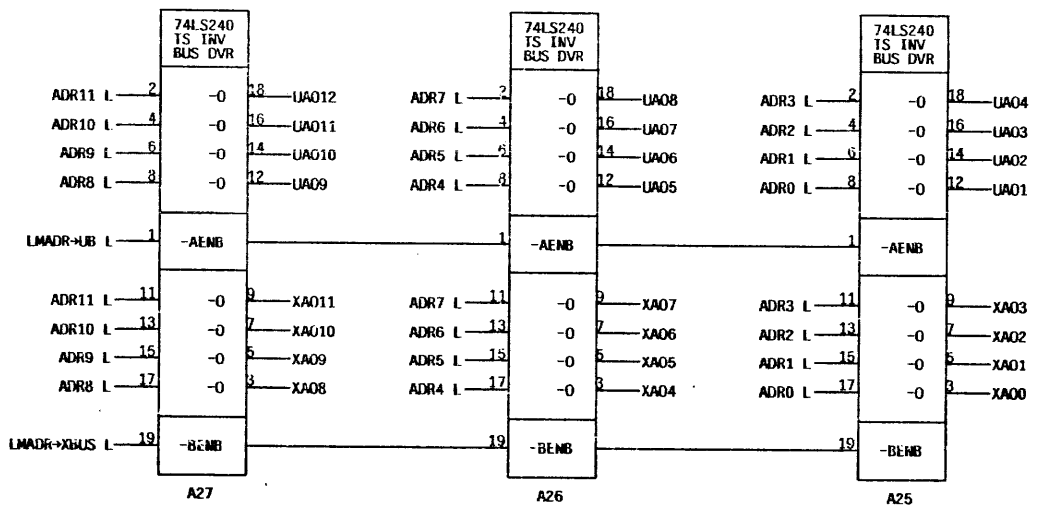

SELECT SPY
UBRD
74S00
A11
SPY READ L
SELECT SPY
UBWR
UB REG WRITE PULSE
74S10
A14
SPY WRITE L

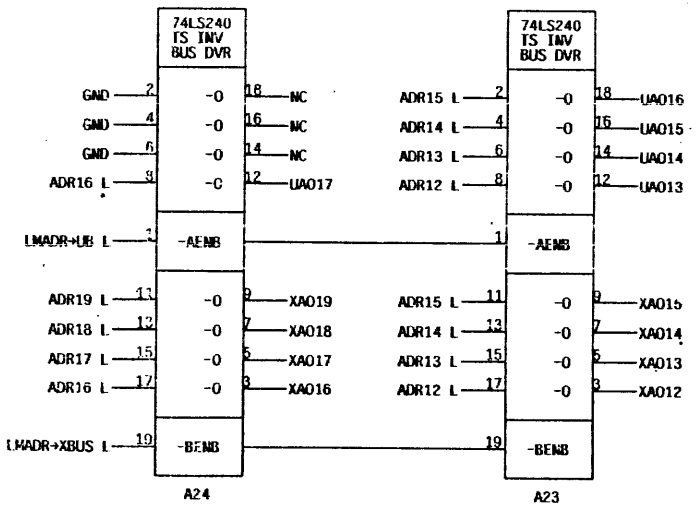


CBUS	DATA PATH - ADDRESS	25-MAY-1978 16:41	AI: CADR1; DPADR

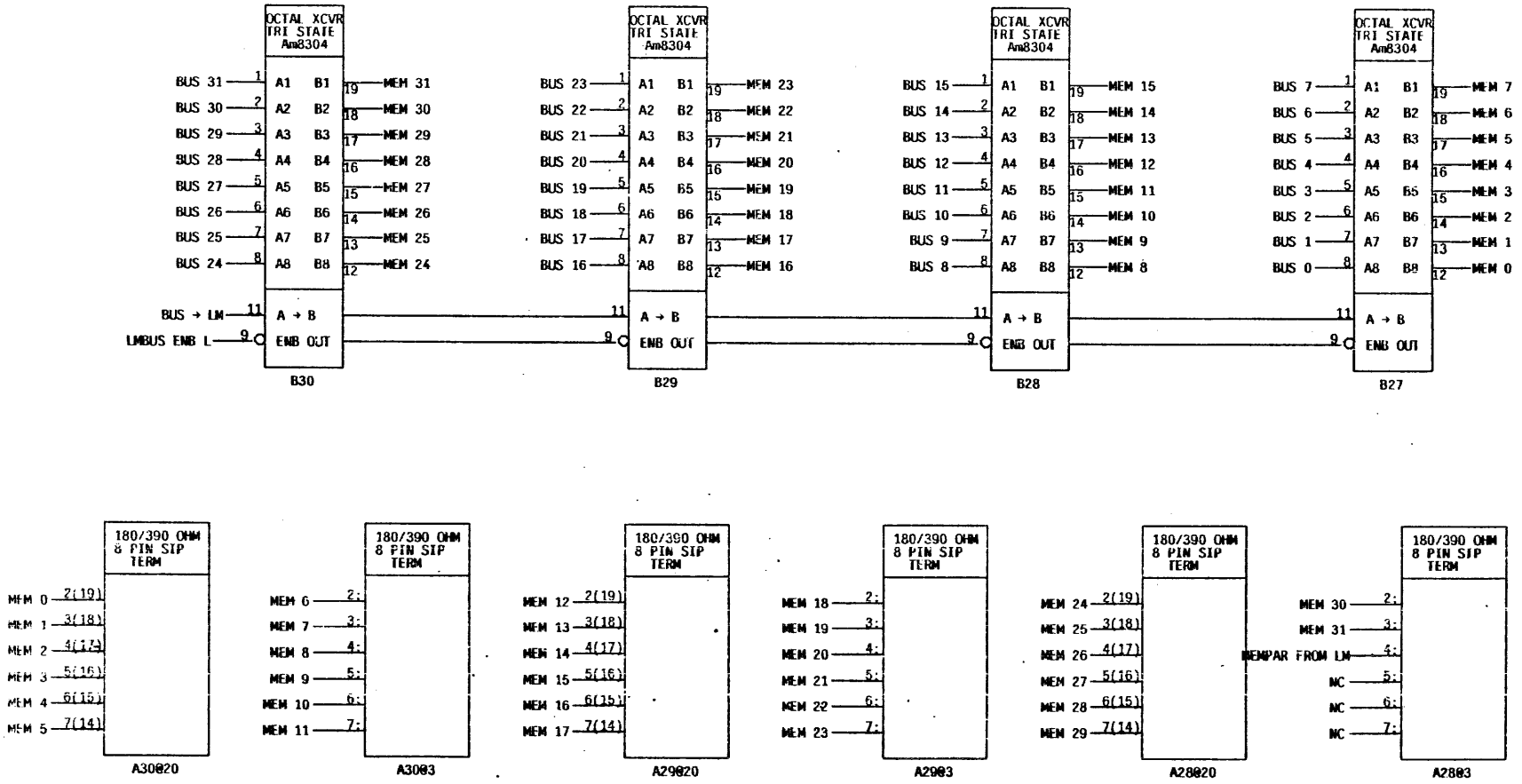


CBUS	DATA PATH - XBUS DATA	25-MAY-1978 16:47	AI: CADR1; DPDATA

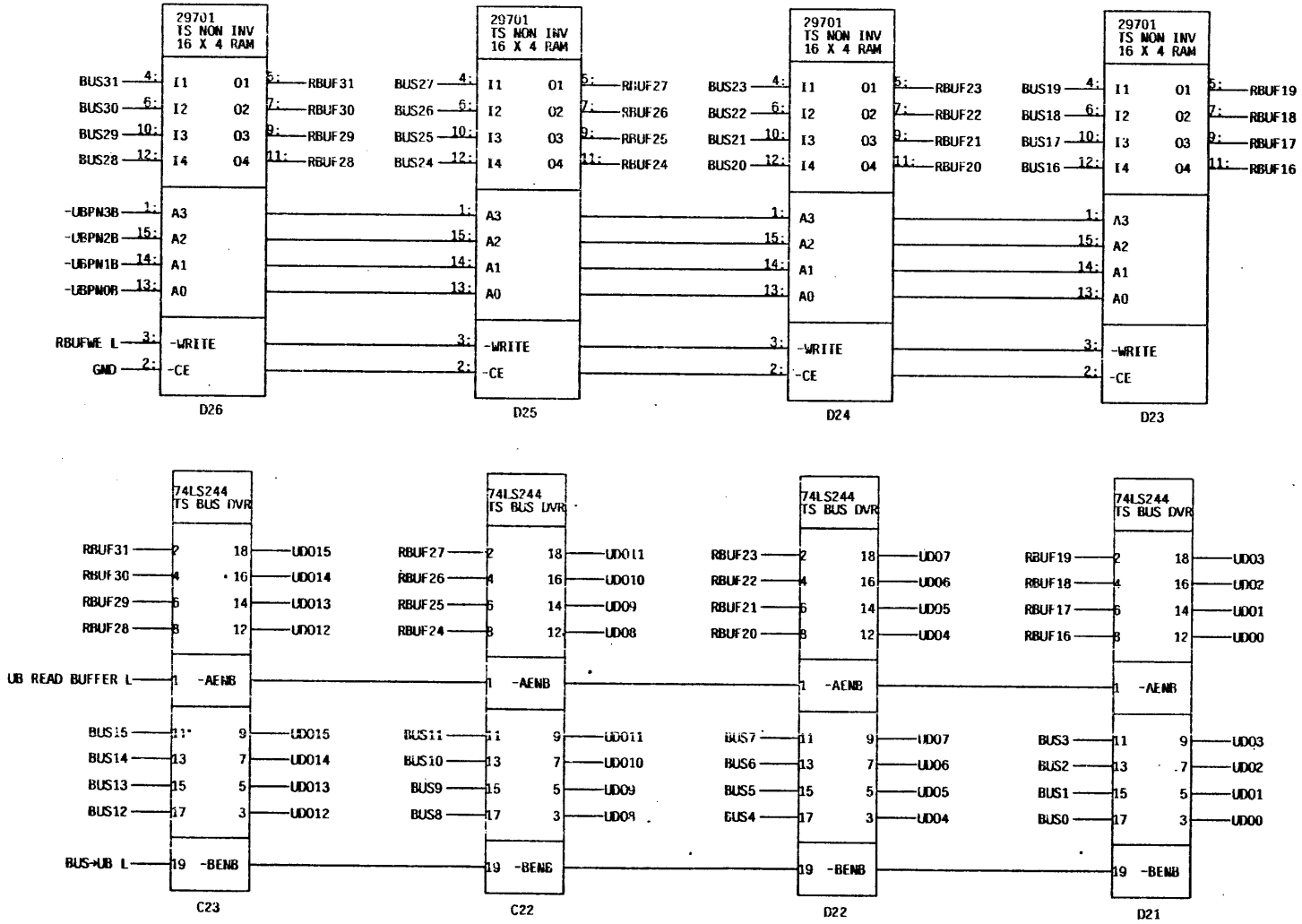




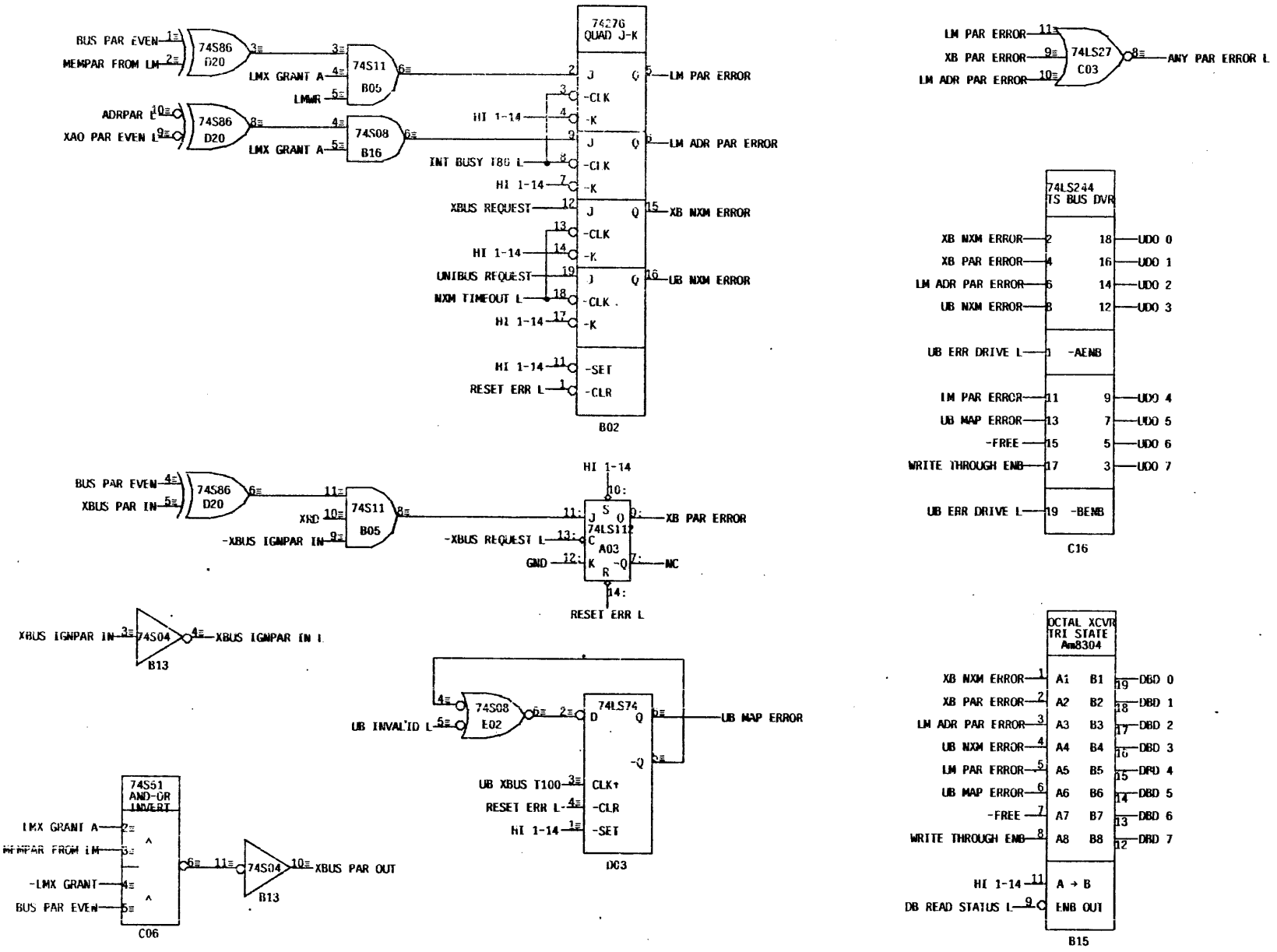
ADR <21:20> APPEAR
ON CADR1; UBINTC



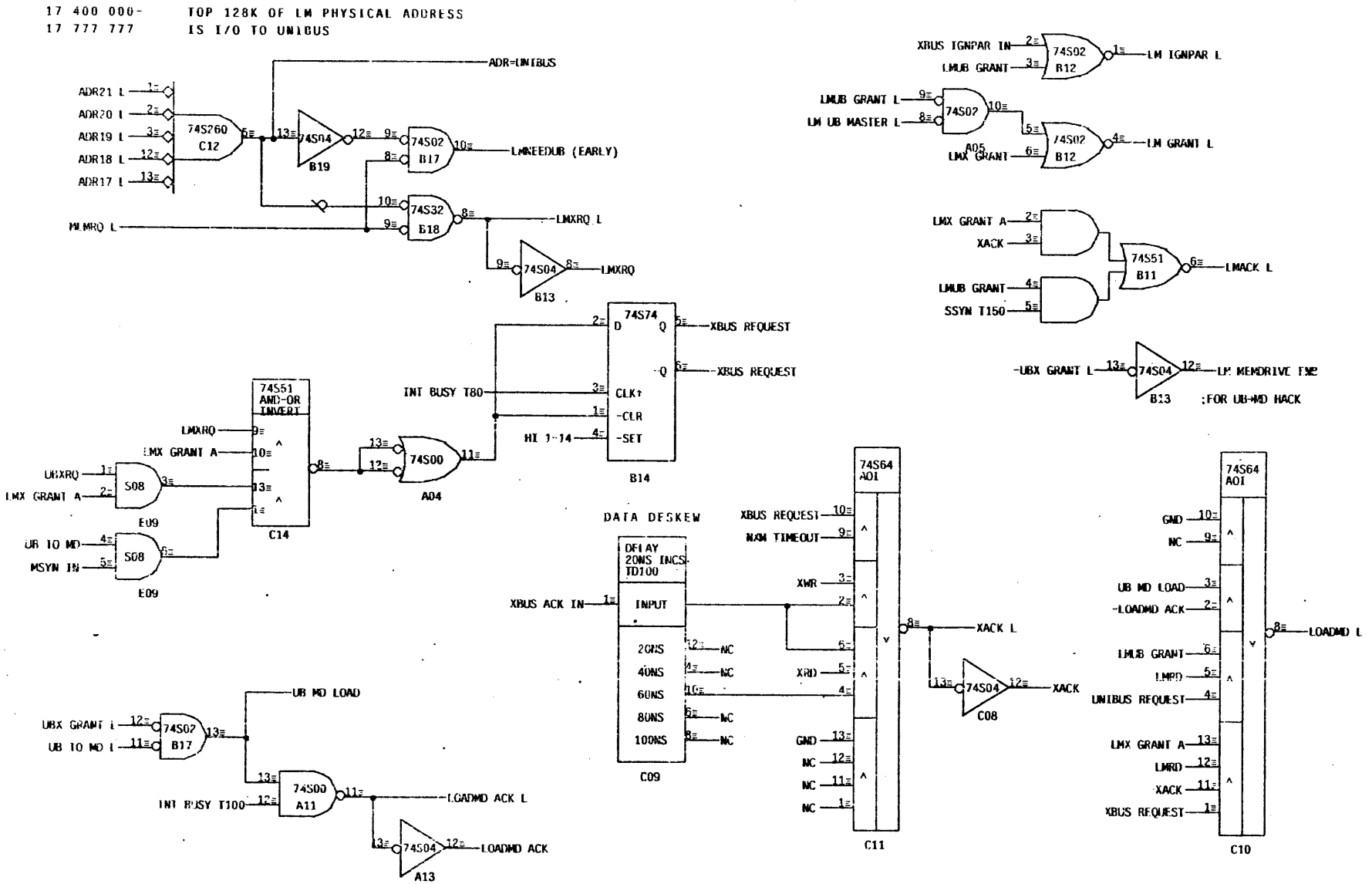
NOTE: MEMPAR TO LM is on DBGOUT



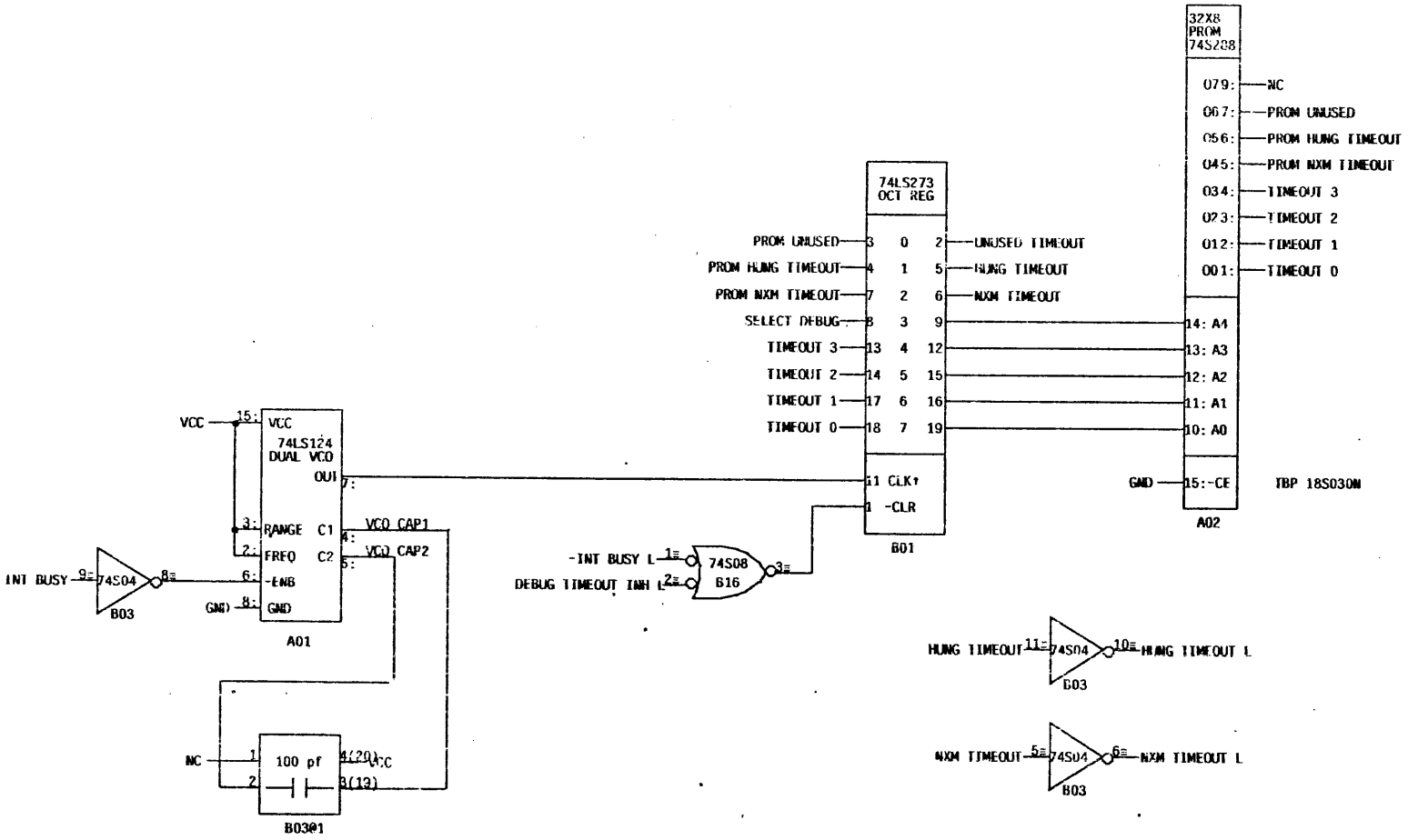
CBUS	READ BUFFER	10-DEC-1980 10:28	AI: CADR1; RBUF



CBUS	ERROR LOGIC	10-DEC-1980 10:40	AI: CADR1; REQERR



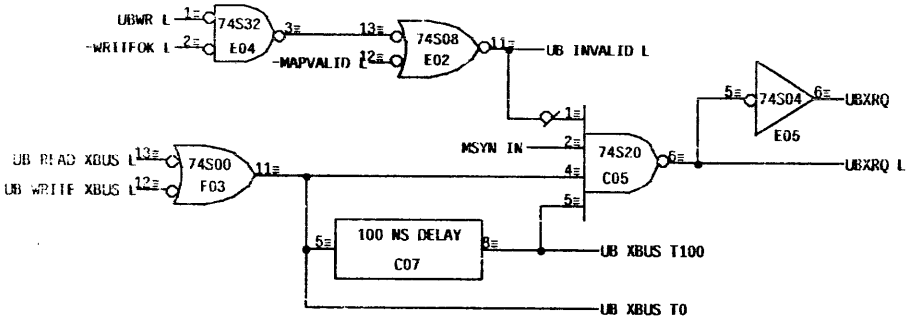
CSUS	XBUS REQ & ACK	10-DEC-1980 17:18	AI: CADR1; REQLM



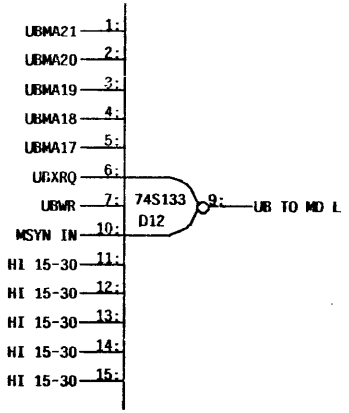
CBUS	XBUS & UNIBUS TIMEOUT	10-DEC-1980 15:26	AI: CADR1; REQTIM

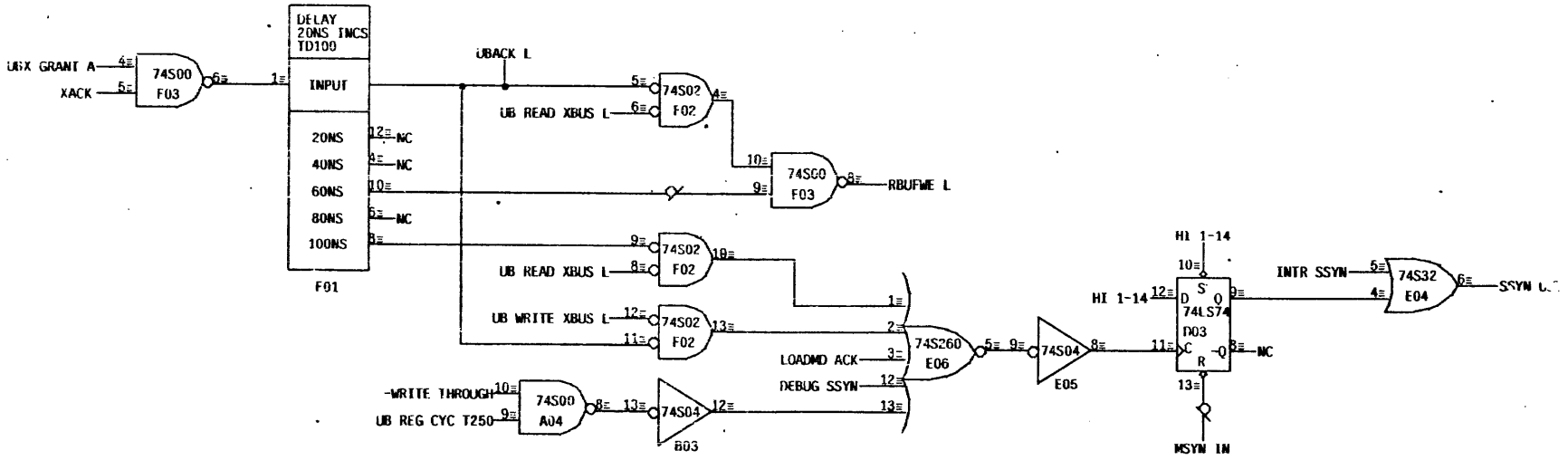
17 400 000 to
17 777 777

THESE ARE LM ADDRESSES THAT ARE MAPPED ONTO UNIBUS
THEY DON'T EXIST ON XBUS
THEREFORE THEY'LL MEAN UNIBUS TO MEMORY DATA REGISTER

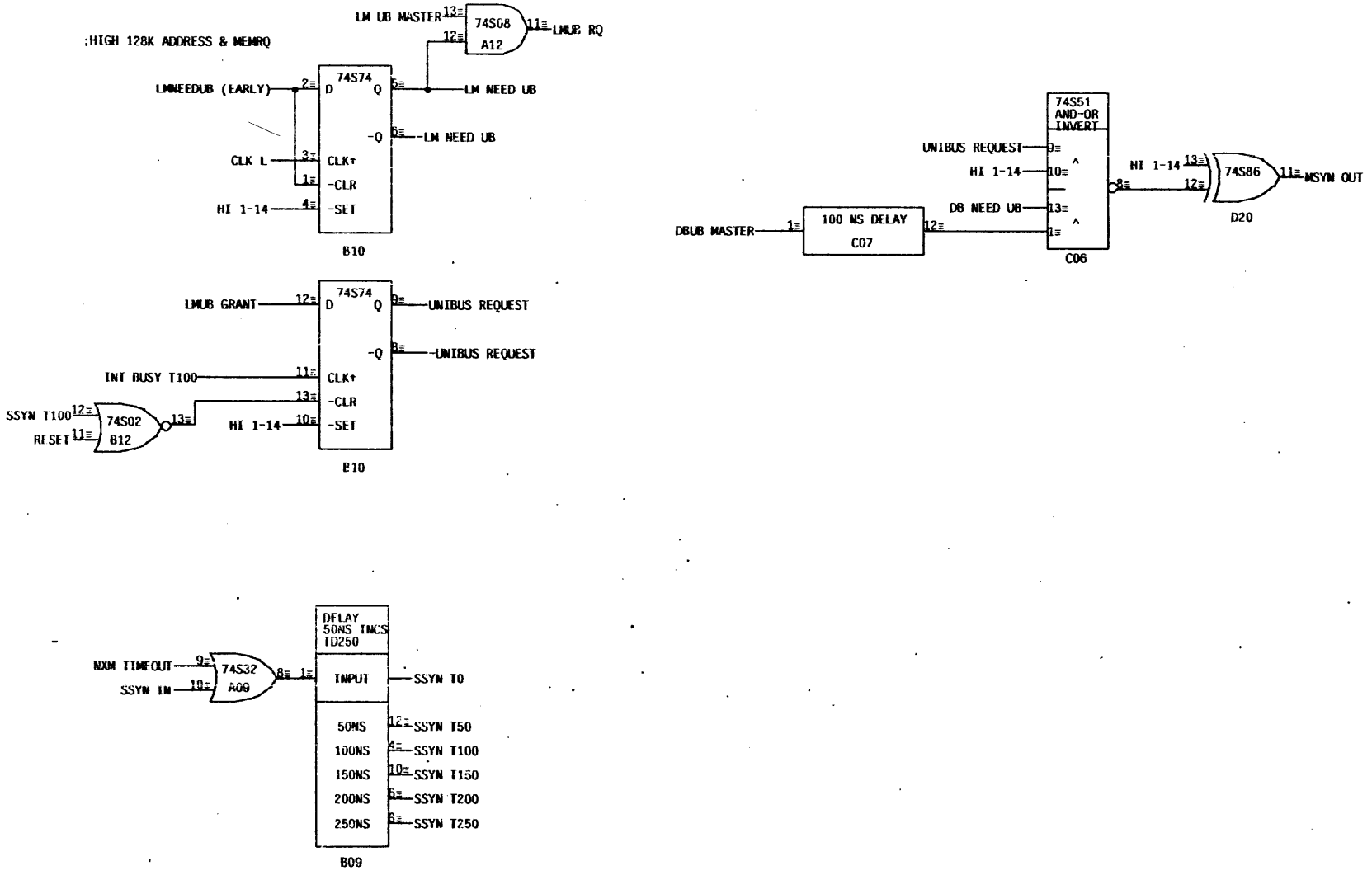


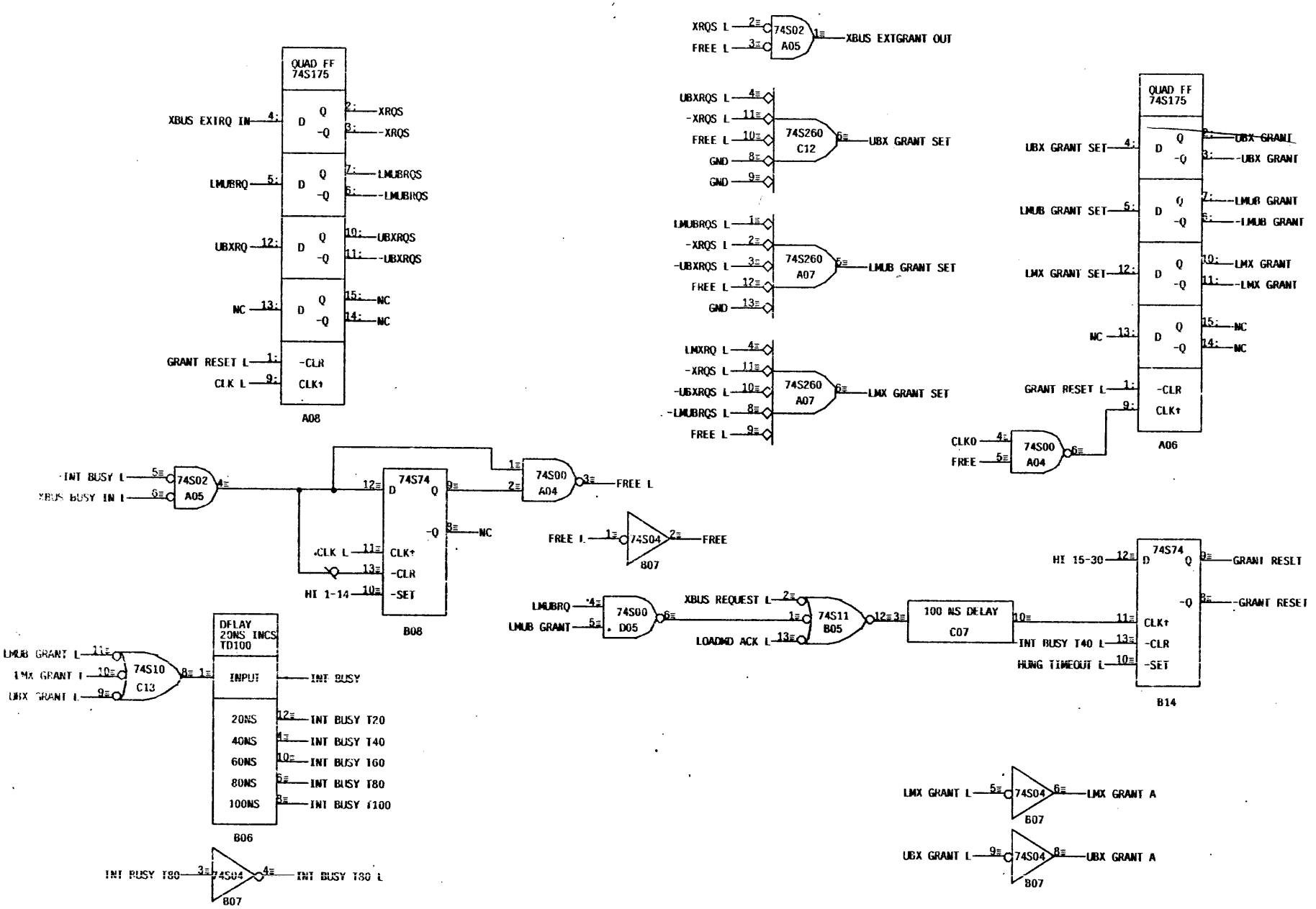
DELAY FOR MAPVALID



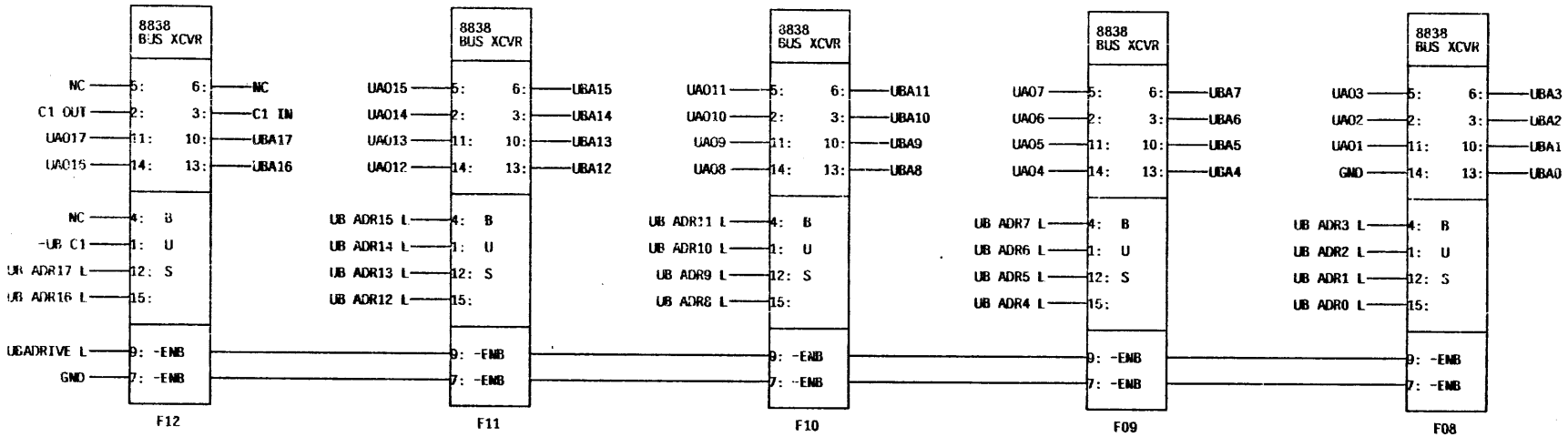


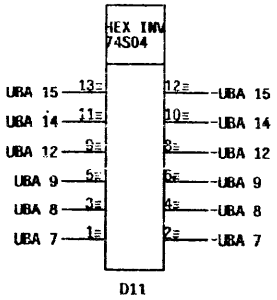
CBUS	XBUS REQUEST FROM UNIBUS	10-DEC-1980 15:36	AI: CADR1; REQU

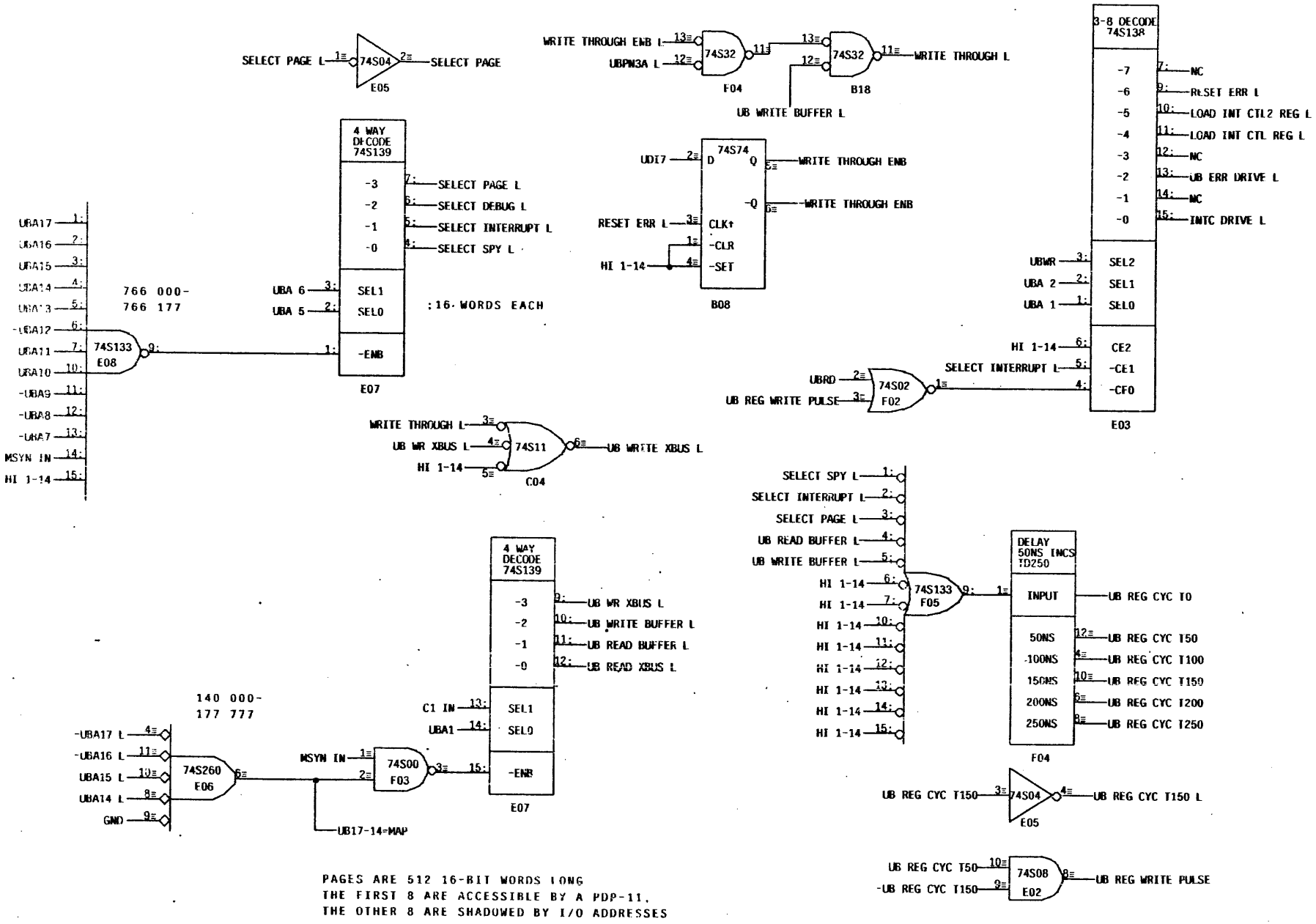

;HIGH 128K ADDRESS & MEMRQ
LM UB MASTER
74S68
A12
LMUB RQ
74S74
LMNEEDUB (EARLY)
D
Q
LM NEED UB
-Q
-LM NEED UB
CLK L
CLK↑
-CLR
HI 1-14
-SET
B10
LMUB GRANT
UNIBUS REQUEST
-UNIBUS REQUEST
INT BUSY T100
SSYN T100
RESET
74S02
B12
B10
74S51
AND-OR
INVERT
UNIBUS REQUEST
DB NEED UB
DBUB MASTER
100 NS DELAY
C07
C06
74S86
NSYN OUT
D20
DELAY
50NS INCS
TD250
NXM TIMEOUT
SSYN IN
74S32
A09
INPUT
SSYN T0
50NS
SSYN T50
100NS
SSYN T100
150NS
SSYN T150
200NS
SSYN T200
250NS
SSYN T250
B09

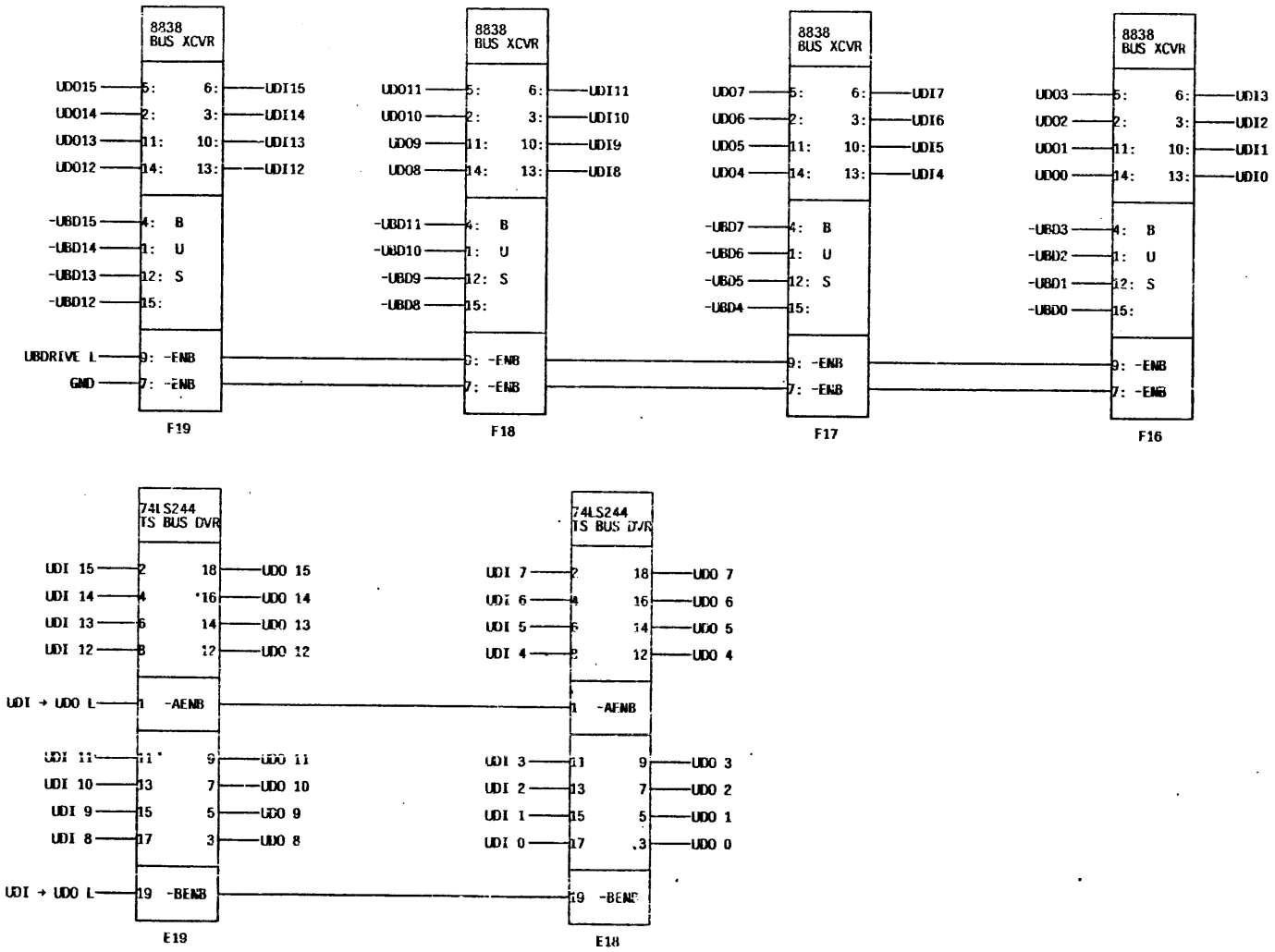


CBUS	REQUEST SYNCHRONIZER	10-DEC-1980 11:32	AI: CADR1; RQSYNC

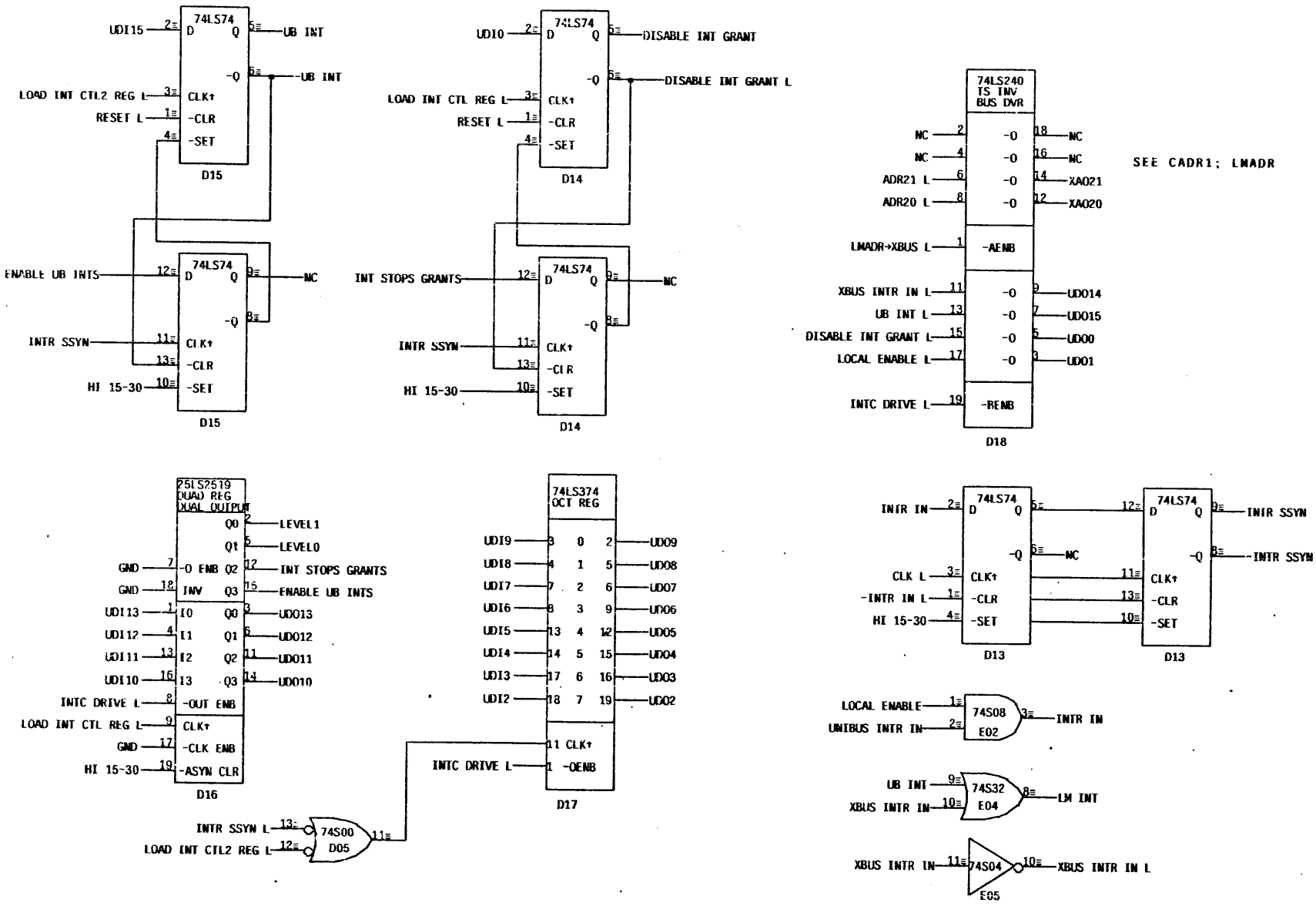

8838
BUS XCVR
NC
C1 OUT
UAO17
UAO16
NC
-UB C1
UB ADR17 L
UB ADR16 L
UBADRIVE L
GND
NC
C1 IN
UBA17
UBA16
F12
UAO15
UAO14
UAO13
UAO12
UB ADR15 L
UB ADR14 L
UB ADR13 L
UB ADR12 L
UBA15
UBA14
UBA13
UBA12
F11
UAO11
UAO10
UAO9
UAO8
UB ADR11 L
UB ADR10 L
UB ADR9 L
UB ADR8 L
UBA11
UBA10
UBA9
UBA8
F10
UAO7
UAO6
UAO5
UAO4
UB ADR7 L
UB ADR6 L
UB ADR5 L
UB ADR4 L
UBA7
UBA6
UBA5
UBA4
F09
UAO3
UAO2
UAO1
GND
UB ADR3 L
UB ADR2 L
UB ADR1 L
UB ADR0 L
UBA3
UBA2
UBA1
UBA0
F08


HEX INV
74S04
UBA 15
UBA 14
UBA 12
UBA 9
UBA 8
UBA 7
-UBA 15
-UBA 14
-UBA 12
-UBA 9
-UBA 8
-UBA 7
D11

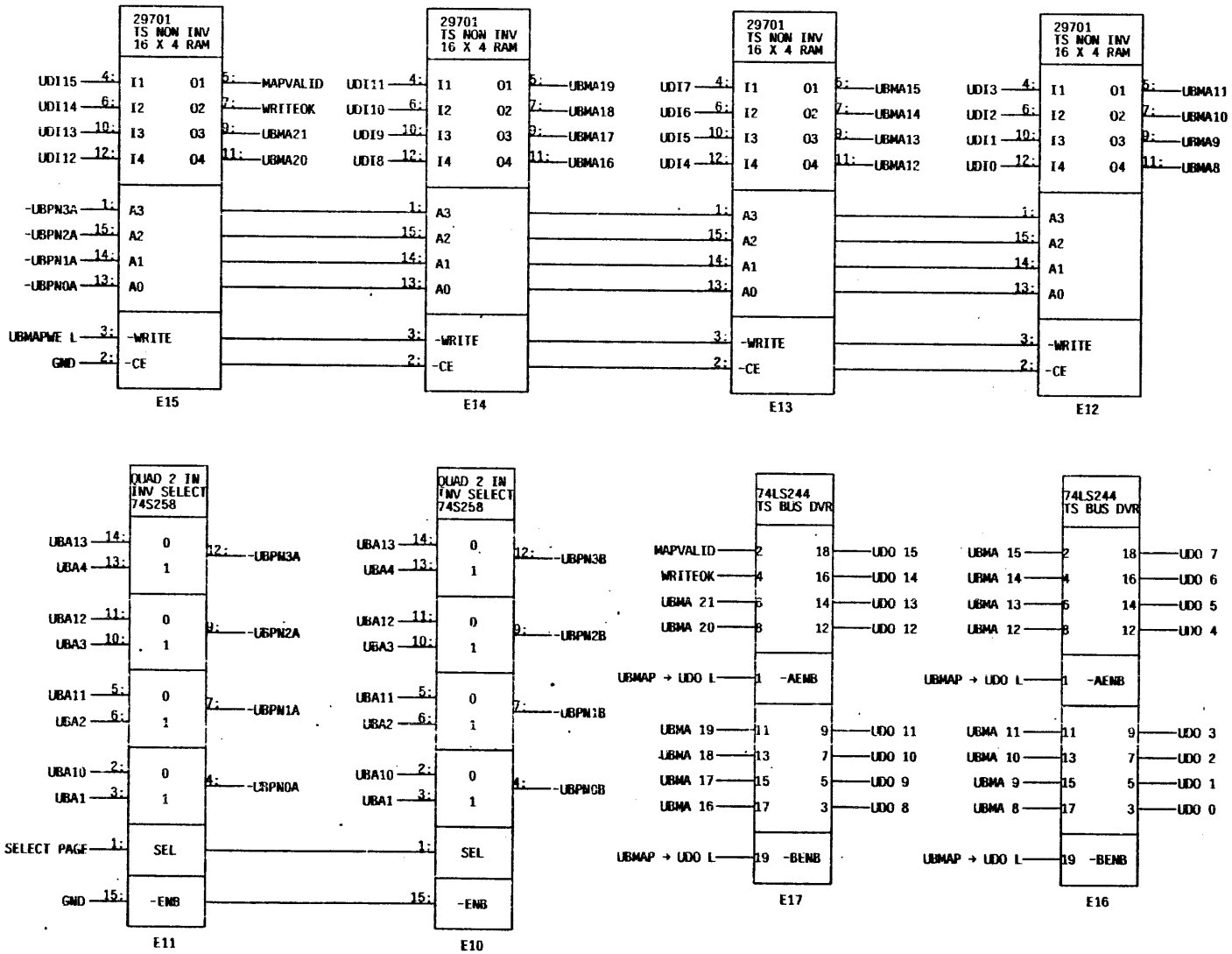

SELECT PAGE L
74S04
E05
SELECT PAGE
WRITE THROUGH ENB L
UBPW3A L
74S32
F04
74S32
B18
WRITE THROUGH L
UB WRITE BUFFER L
3-8 DECODE
74S138
-7
-6
-5
-4
-3
-2
-1
-0
NC
RESET ERR L
LOAD INT CTL2 REG L
LOAD INT CTL REG L
NC
UB ERR DRIVE L
NC
INTC DRIVE L
4 WAY
DECODE
74S139
-3
-2
-1
-0
SELECT PAGE L
SELECT DEBUG L
SELECT INTERRUPT L
SELECT SPY L
UBA 6
UBA 5
SEL1
SEL0
-ENB
E07
766 000-
766 177
:16. WORDS EACH
UBA17
UBA16
UBA15
UBA14
UBA13
-UBA12
UBA11
UBA10
-UBA9
-UBA8
-UBA7
MSYN IN
HI 1-14
74S133
E08
UDI7
74S74
D
Q
WRITE THROUGH ENB
-Q
WRITE THROUGH ENB
RESET ERR L
CLK↑
-CLR
-SET
HI 1-14
B08
UBWR
UBA 2
UBA 1
SEL2
SEL1
SEL0
HI 1-14
CE2
-CE1
-CF0
E03
UBRD
UB REG WRITE PULSE
74S02
F02
SELECT INTERRUPT L
WRITE THROUGH L
UB WR XBUS L
HI 1-14
74S11
C04
UB WRITE XBUS L
SELECT SPY L
SELECT INTERRUPT L
SELECT PAGE L
UB READ BUFFER L
UB WRITE BUFFER L
HI 1-14
74S133
F05
DELAY
50NS INCS
TD250
INPUT
UB REG CYC T0
50NS
100NS
150NS
200NS
250NS
UB REG CYC T50
UB REG CYC T100
UB REG CYC T150
UB REG CYC T200
UB REG CYC T250
F04
4 WAY
DECODE
74S139
-3
-2
-1
-0
UB WR XBUS L
UB WRITE BUFFER L
UB READ BUFFER L
UB READ XBUS L
C1 IN
UBA1
SEL1
SEL0
-ENB
E07
140 000-
177 777
-UBA17 L
-UBA16 L
UBA15 L
UBA14 L
GND
74S260
E06
MSYN IN
74S00
F03
UB17-14=MAP
UB REG CYC T150
74S04
E05
UB REG CYC T150 L
UB REG CYC T50
-UB REG CYC T150
74S08
E02
UB REG WRITE PULSE
PAGES ARE 512 16-BIT WORDS LONG
THE FIRST 8 ARE ACCESSIBLE BY A PDP-11.
THE OTHER 8 ARE SHADOWED BY I/O ADDRESSES



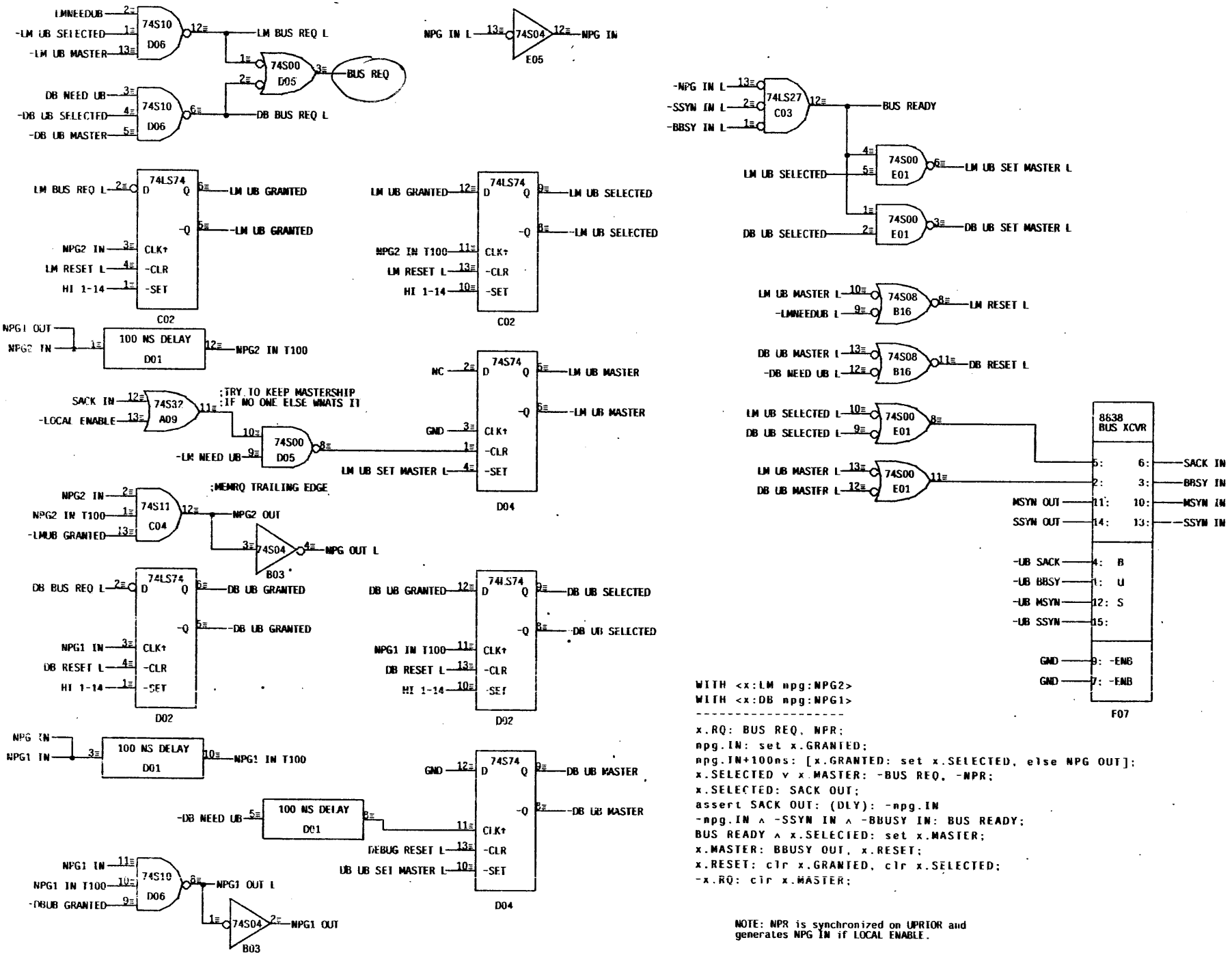
CBUS	UNIBUS DATA TRANSCEIVERS	10-DEC-1980 11:33	AI: CADR1; UBD

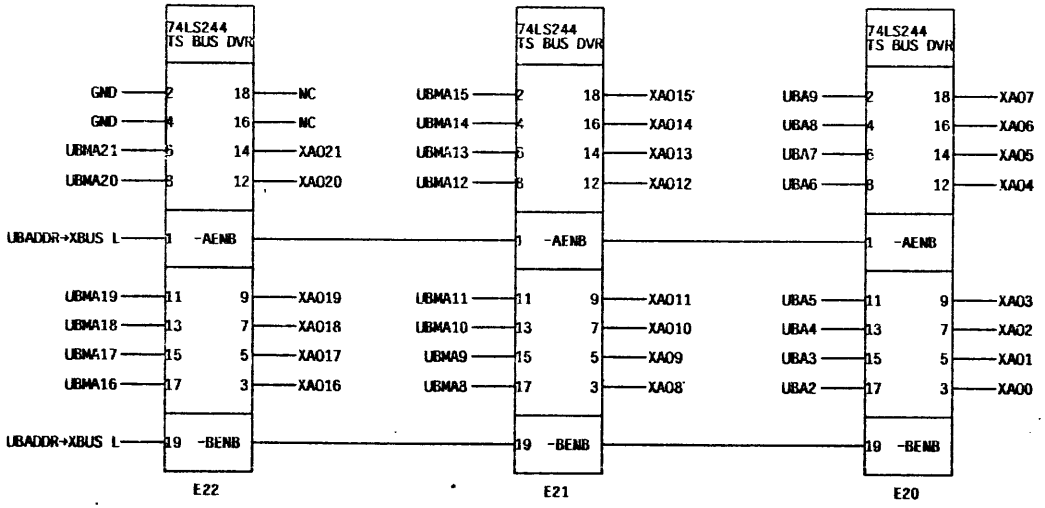


CBUS	UNIBUS INTERRUPT CONTROL	10-DEC-1980 11:34	AI: CADR1; UBINTC

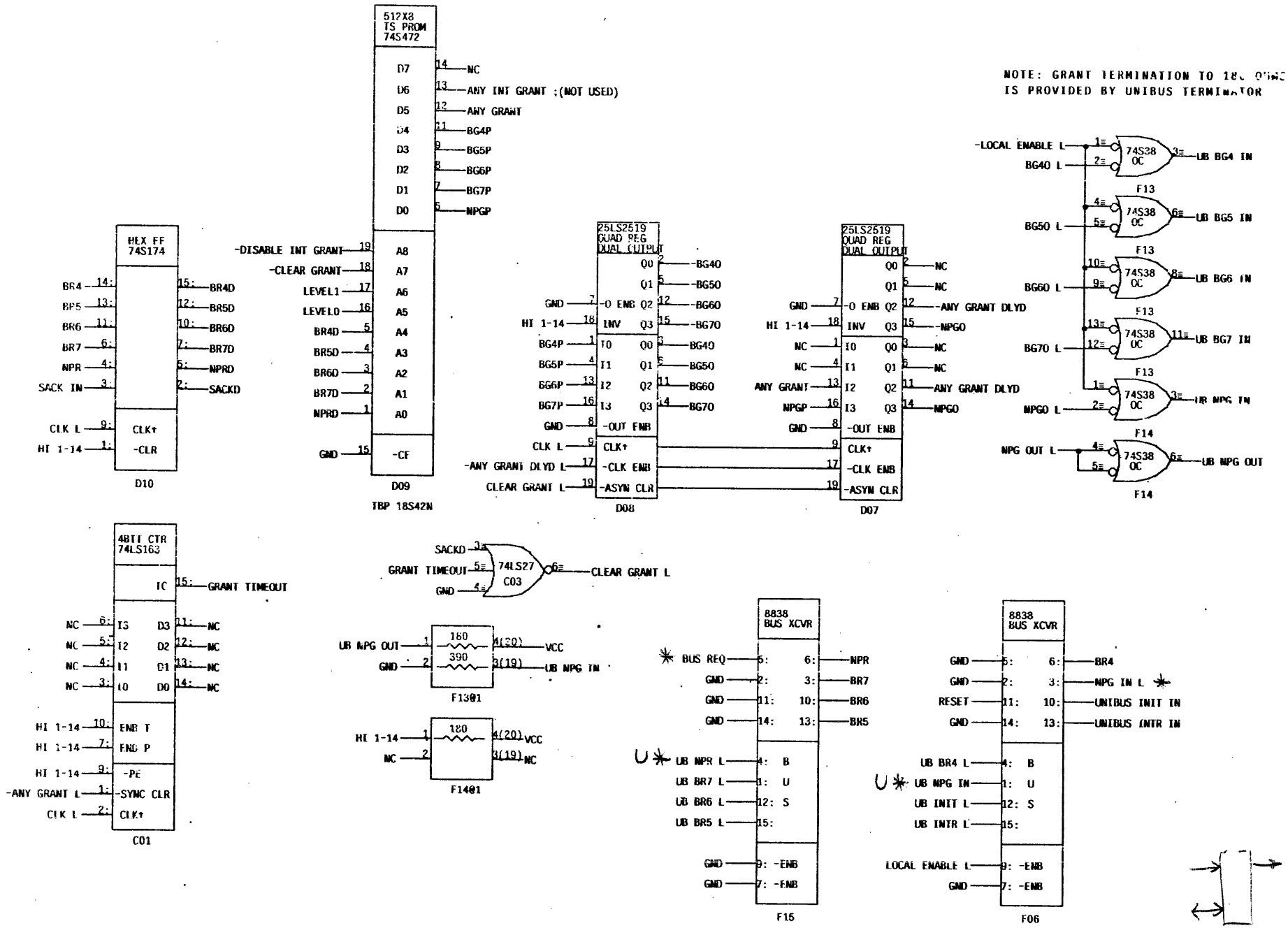


CBUS	UNIBUS MAP	10-DEC-1980 11:35	AI: CADR1; UBMAP

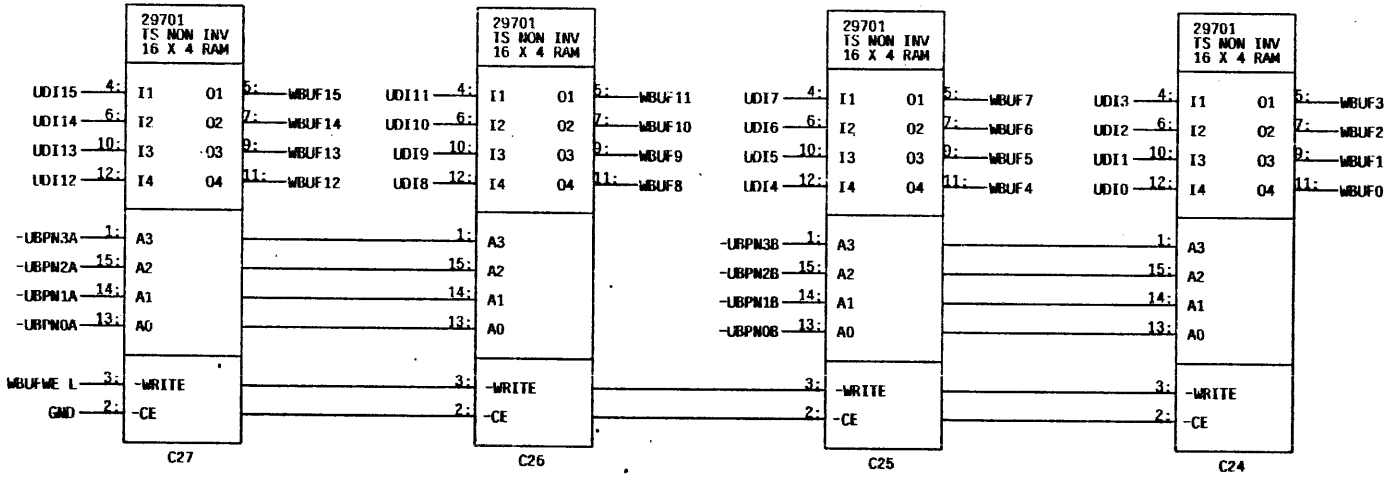

LMNEEDUB
-LM UB SELECTED
-LM UB MASTER
74S10 D06
LM BUS REQ L
74S00 D05
BUS REQ
DB NEED UB
-DB UB SELECTED
-DB UB MASTER
74S10 D06
DB BUS REQ L
NPG IN L
74S04 E05
NPG IN
-NPG IN L
-SSYN IN L
-BBSY IN L
74LS27 C03
BUS READY
LM UB SELECTED
74S00 E01
LM UB SET MASTER L
DB UB SELECTED
74S00 E01
DB UB SET MASTER L
LM BUS REQ L
74LS74 C02
LM UB GRANTED
-LM UB GRANTED
NPG2 IN
LM RESET L
HI 1-14
LM UB GRANTED
74LS74 C02
LM UB SELECTED
-LM UB SELECTED
NPG2 IN T100
LM RESET L
HI 1-14
LM UB MASTER L
-LMNEEDUB L
74S08 B16
LM RESET L
DB UB MASTER L
-DB NEED UB L
74S08 B16
DB RESET L
NPG1 OUT
NPG2 IN
100 NS DELAY D01
NPG2 IN T100
NC
74S74 D04
LM UB MASTER
-LM UB MASTER
GND
LM UB SET MASTER L
SACK IN
-LOCAL ENABLE
74S32 A09
;TRY TO KEEP MASTERSHIP
;IF NO ONE ELSE WANTS IT
-LM NEED UB
74S00 D05
;MEMRQ TRAILING EDGE
NPG2 IN
NPG2 IN T100
-LMUB GRANTED
74S11 C04
NPG2 OUT
74S04 B03
NPG OUT L
LM UB SELECTED L
DB UB SELECTED L
74S00 E01
LM UB MASTER L
DB UB MASTER L
74S00 E01
8838 BUS XCVR
SACK IN
BBSY IN
MSYN OUT
MSYN IN
SSYN OUT
SSYN IN
-UB SACK
-UB BBSY
-UB MSYN
-UB SSYN
B
U
S
GND
-ENB
GND
-ENB
F07
DB BUS REQ L
74LS74 D02
DB UB GRANTED
-DB UB GRANTED
NPG1 IN
DB RESET L
HI 1-14
DB UB GRANTED
74LS74 D02
DB UB SELECTED
-DB UB SELECTED
NPG1 IN T100
DB RESET L
HI 1-14
NPG IN
NPG1 IN
100 NS DELAY D01
NPG1 IN T100
-DB NEED UB
100 NS DELAY D01
DEBUG RESET L
UB UB SET MASTER L
GND
74S74 D04
DB UB MASTER
-DB UB MASTER
NPG1 IN
NPG1 IN T100
-DBUB GRANTED
74S10 D06
NPG1 OUT L
74S04 B03
NPG1 OUT
WITH <x:LM npg:NPG2>
WITH <x:DB npg:NPG1>
x.RQ: BUS REQ, NPR;
npg.IN: set x.GRANTED;
npg.IN+100ns: [x.GRANTED: set x.SELECTED, else NPG OUT];
x.SELECTED v x.MASTER: -BUS REQ, -NPR;
x.SELECTED: SACK OUT;
assert SACK OUT: (DLY): -npg.IN
-npg.IN ∧ -SSYN IN ∧ -BBUSY IN: BUS READY;
BUS READY ∧ x.SELECTED: set x.MASTER;
x.MASTER: BBUSY OUT, x.RESET;
x.RESET: clr x.GRANTED, clr x.SELECTED;
-x.RQ: clr x.MASTER;
NOTE: NPR is synchronized on UPRIOR and
generates NPG IN if LOCAL ENABLE.



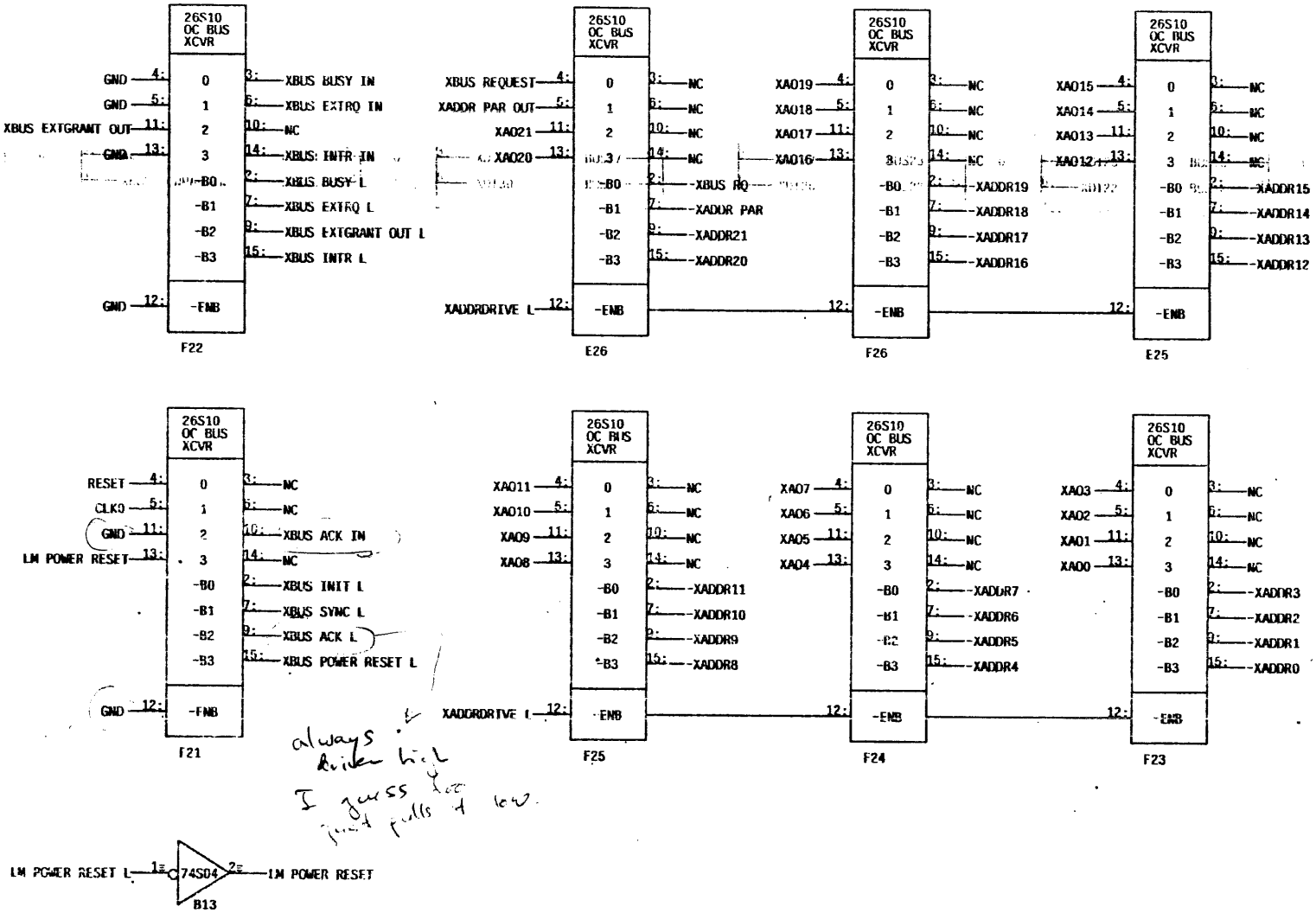
CBUS	UNIBUS ADDRESS TO XBUS	10-DEC-1980 11:36	AI: CADR1; UBXA

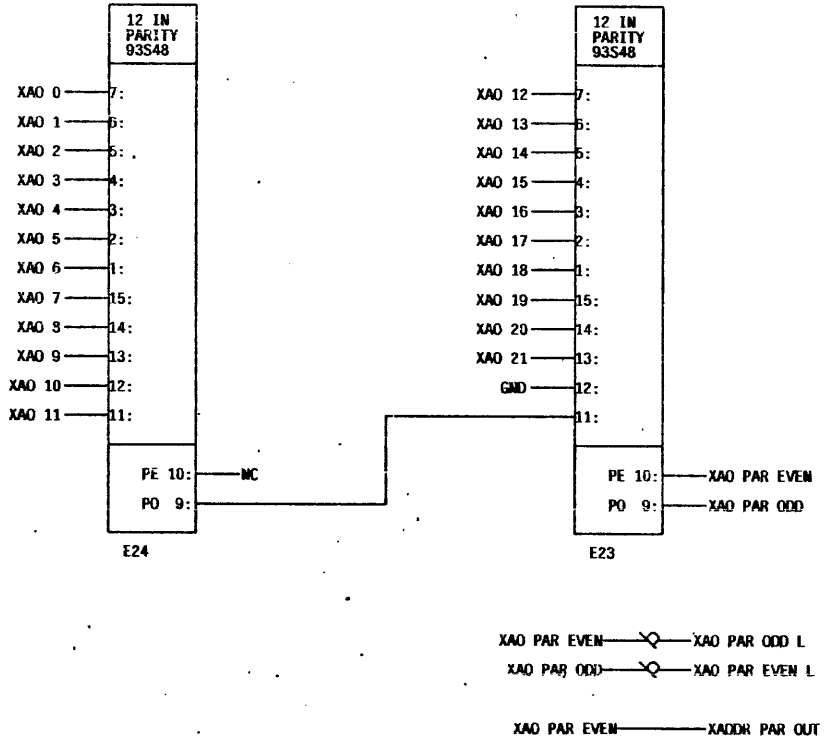


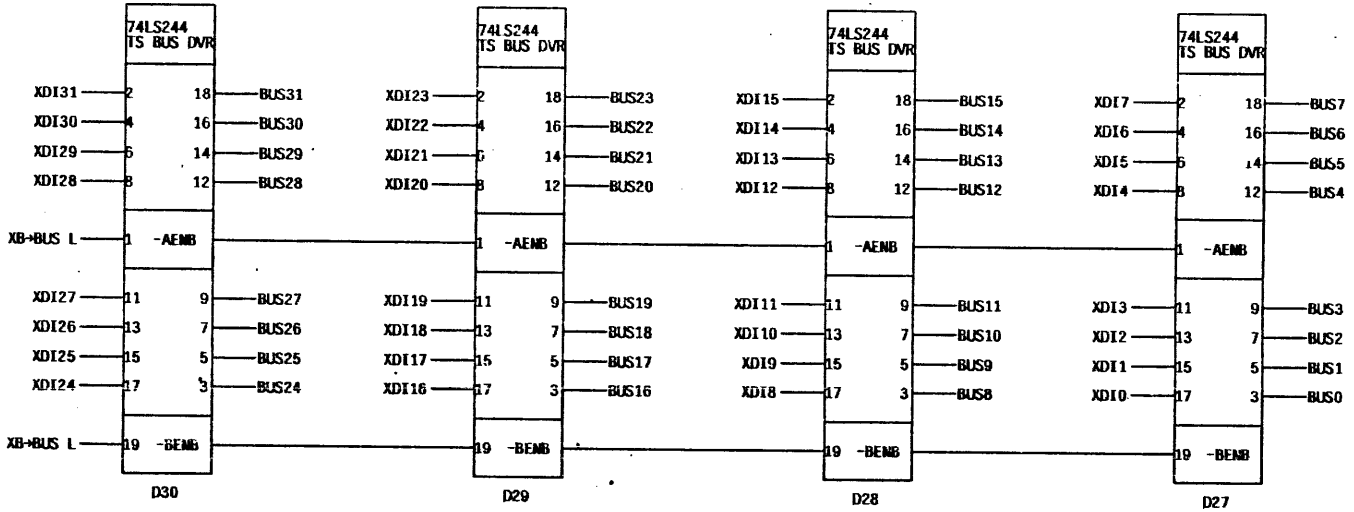
CBUS	UNIBUS BUS GRANT	10-DEC-1980 13:15	AI: CADR1; UPRIOR



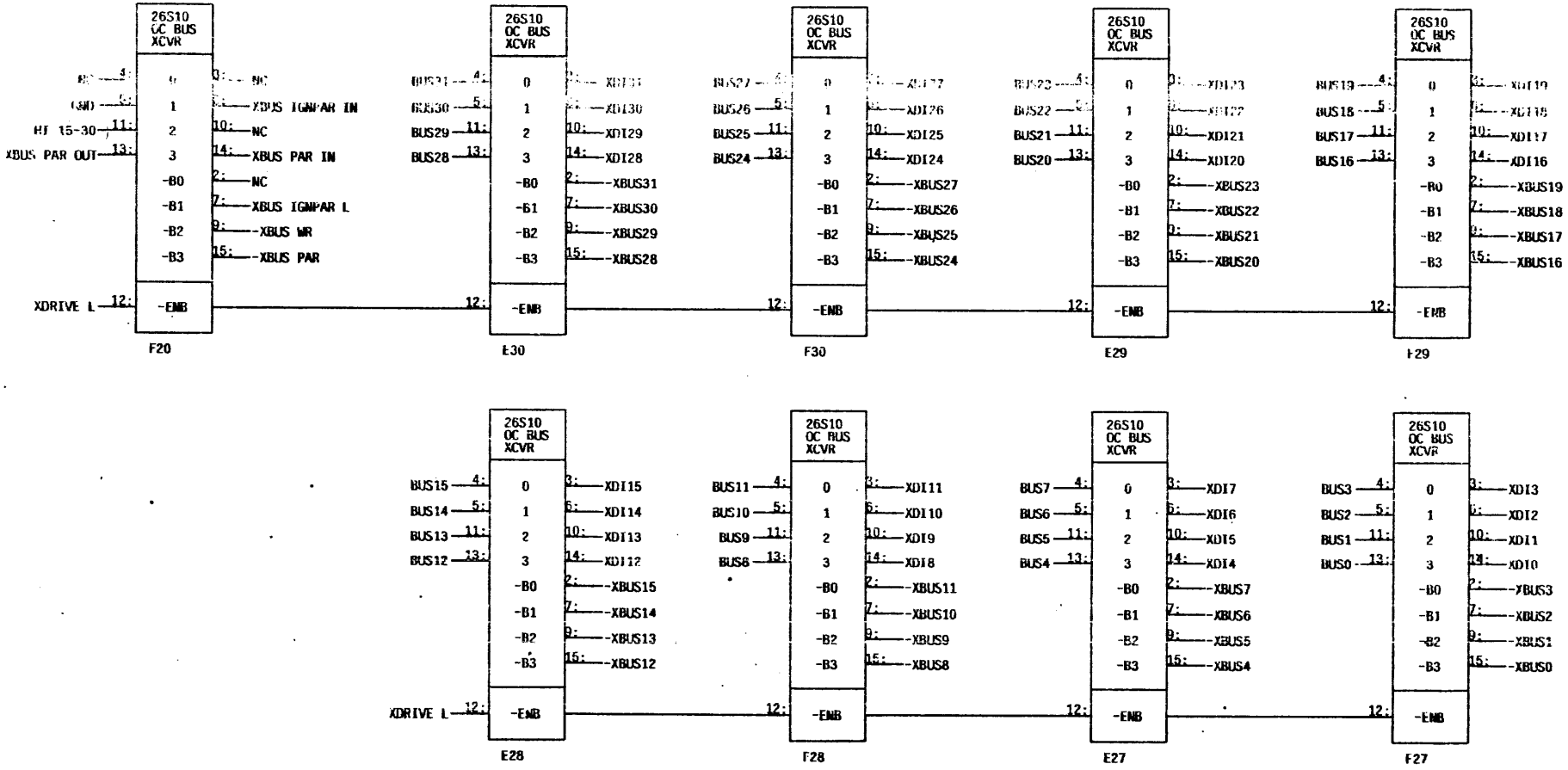
CBUS	WRITE BUFFER	10-DEC-1980 11:37	AI: CADR1; WBUF


26S10
OC BUS
XCVR
GND
GND
XBUS EXTGRANT OUT
GND
0
1
2
3
-B0
-B1
-B2
-B3
-ENB
XBUS BUSY IN
XBUS EXTRQ IN
XBUS INTR IN
XBUS BUSY L
XBUS EXTRQ L
XBUS EXTGRANT OUT L
XBUS INTR L
F22
XBUS REQUEST
XADDR PAR OUT
XA021
XA020
XADDRDRIVE L
XBUS RQ
XADDR PAR
XADDR21
XADDR20
E26
XA019
XA018
XA017
XA016
XADDR19
XADDR18
XADDR17
XADDR16
F26
XA015
XA014
XA013
XA012
XADDR15
XADDR14
XADDR13
XADDR12
E25
RESET
CLK9
GND
LM POWER RESET
XBUS ACK IN
XBUS INIT L
XBUS SYNC L
XBUS ACK L
XBUS POWER RESET L
F21
XA011
XA010
XA009
XA008
XADDR11
XADDR10
XADDR9
XADDR8
F25
XA007
XA006
XA005
XA004
XADDR7
XADDR6
XADDR5
XADDR4
F24
XA003
XA002
XA001
XA000
XADDR3
XADDR2
XADDR1
XADDR0
F23
NC
always driven high
I guess but pulls it low
LM POWER RESET L
74S04
LM POWER RESET
B13


12 IN PARITY 93S48
XAO 0
XAO 1
XAO 2
XAO 3
XAO 4
XAO 5
XAO 6
XAO 7
XAO 8
XAO 9
XAO 10
XAO 11
7:
6:
5:
4:
3:
2:
1:
15:
14:
13:
12:
11:
PE 10:
PO 9:
NC
E24
12 IN PARITY 93S48
XAO 12
XAO 13
XAO 14
XAO 15
XAO 16
XAO 17
XAO 18
XAO 19
XAO 20
XAO 21
GND
7:
6:
5:
4:
3:
2:
1:
15:
14:
13:
12:
11:
PE 10:
PO 9:
XAO PAR EVEN
XAO PAR ODD
E23
XAO PAR EVEN
XAO PAR ODD L
XAO PAR ODD
XAO PAR EVEN L
XAO PAR EVEN
XADDR PAR OUT



CBUS	XBUS TO BUS	10-DEC-1980 16:06	AI: CADR1; XBD



CBUS	XBUS DATA TRANSCEIVERS	10-DEC-1980 11:50	AI: CADR1; XD