

# Breadboard 8088 PC Ver 3.0

<table><tr><td>GND</td><td>VCC</td></tr><tr><td>A14</td><td>A15</td></tr><tr><td>A13</td><td>A16S3</td></tr><tr><td>A12</td><td>A17S4</td></tr><tr><td>A11</td><td>A18S5</td></tr><tr><td>A10</td><td>A19S6</td></tr><tr><td>A9</td><td>HIGH</td></tr><tr><td>A8</td><td>MNMX</td></tr><tr><td>AD7</td><td>RD</td></tr><tr><td>AD6</td><td>RQGT0</td></tr><tr><td>AD5</td><td>RQGT1</td></tr><tr><td>AD4</td><td>LOCK</td></tr><tr><td>AD3</td><td>MSZ</td></tr><tr><td>AD2</td><td>ST</td></tr><tr><td>AD1</td><td>Q0</td></tr><tr><td>AD0</td><td>QS0</td></tr><tr><td>NMI</td><td>QS1</td></tr><tr><td>INTR</td><td>TEST</td></tr><tr><td>CLK</td><td>READY</td></tr><tr><td>GND</td><td>RESET</td></tr></table>	GND	VCC	A14	A15	A13	A16S3	A12	A17S4	A11	A18S5	A10	A19S6	A9	HIGH	A8	MNMX	AD7	RD	AD6	RQGT0	AD5	RQGT1	AD4	LOCK	AD3	MSZ	AD2	ST	AD1	Q0	AD0	QS0	NMI	QS1	INTR	TEST	CLK	READY	GND	RESET	<table><tr><td>CsycgVcc</td><td>A7</td></tr><tr><td>Pclk 2 X1</td><td>A6</td></tr><tr><td>Aen14 X2</td><td>A5</td></tr><tr><td>Rdy1 Axy</td><td>A4</td></tr><tr><td>Rdy EF1</td><td>A3</td></tr><tr><td>Rdy2 F/C</td><td>A2</td></tr><tr><td>Aen2 Osc</td><td>A1</td></tr><tr><td>CLK Res</td><td>A0</td></tr><tr><td>GND Rst</td><td></td></tr></table> <table><tr><td>IOB8/Vcc</td><td>A7</td></tr><tr><td>CLK S0</td><td>A6</td></tr><tr><td>ST S2</td><td>A5</td></tr><tr><td>Dt/K mpt</td><td>A4</td></tr><tr><td>ALE Den</td><td>A3</td></tr><tr><td>AEN Cen</td><td>A2</td></tr><tr><td>mrd Tnta</td><td>A1</td></tr><tr><td>amw Torc</td><td>A0</td></tr><tr><td>mwT Atow</td><td></td></tr><tr><td>GND Tgw</td><td></td></tr></table>	CsycgVcc	A7	Pclk 2 X1	A6	Aen14 X2	A5	Rdy1 Axy	A4	Rdy EF1	A3	Rdy2 F/C	A2	Aen2 Osc	A1	CLK Res	A0	GND Rst		IOB8/Vcc	A7	CLK S0	A6	ST S2	A5	Dt/K mpt	A4	ALE Den	A3	AEN Cen	A2	mrd Tnta	A1	amw Torc	A0	mwT Atow		GND Tgw		<table><tr><td>TOR</td><td>A7</td></tr><tr><td>TOW</td><td>A6</td></tr><tr><td>MEMR</td><td>A5</td></tr><tr><td>MEMW</td><td>A4</td></tr><tr><td>Pin 5</td><td>A3</td></tr><tr><td>Ready</td><td>A2</td></tr><tr><td>HLDA</td><td>A1</td></tr><tr><td>ADstb</td><td>A0</td></tr><tr><td>AEN</td><td>A0</td></tr><tr><td>HRQ</td><td>VCC</td></tr><tr><td>Dack2</td><td>DB0</td></tr><tr><td>CLK</td><td>DB1</td></tr><tr><td>RESET</td><td>DB2</td></tr><tr><td>Dack3</td><td>DB3</td></tr><tr><td>Dack3</td><td>DB4</td></tr><tr><td>Dreg3</td><td>Dack0</td></tr><tr><td>Dreg2</td><td>Dack1</td></tr><tr><td>Dreg1</td><td>DB5</td></tr><tr><td>Dreg0</td><td>DB6</td></tr><tr><td>GND</td><td>DB7</td></tr></table>	TOR	A7	TOW	A6	MEMR	A5	MEMW	A4	Pin 5	A3	Ready	A2	HLDA	A1	ADstb	A0	AEN	A0	HRQ	VCC	Dack2	DB0	CLK	DB1	RESET	DB2	Dack3	DB3	Dack3	DB4	Dreg3	Dack0	Dreg2	Dack1	Dreg1	DB5	Dreg0	DB6	GND	DB7	<table><tr><td>D2</td><td>8</td><td>D1</td></tr><tr><td>D3</td><td>2</td><td>D0</td></tr><tr><td>RxD</td><td>1</td><td>Vcc</td></tr><tr><td>GND</td><td></td><td></td></tr><tr><td>D4</td><td>U</td><td>DTR</td></tr><tr><td>D5</td><td>A</td><td>TRS</td></tr><tr><td>D6</td><td>R</td><td>DSR</td></tr><tr><td>D7</td><td></td><td>RESET</td></tr><tr><td>TxC</td><td></td><td>CLK</td></tr><tr><td>WR</td><td></td><td>TxD</td></tr><tr><td>CS</td><td></td><td>TxEmp</td></tr><tr><td>C/D</td><td></td><td>CTS</td></tr><tr><td>RD</td><td></td><td>Syn/Bd</td></tr><tr><td>RxRdy</td><td></td><td>TxRdy</td></tr></table>	D2	8	D1	D3	2	D0	RxD	1	Vcc	GND			D4	U	DTR	D5	A	TRS	D6	R	DSR	D7		RESET	TxC		CLK	WR		TxD	CS		TxEmp	C/D		CTS	RD		Syn/Bd	RxRdy		TxRdy	<table><tr><td>D7</td><td>Vcc</td></tr><tr><td>D6</td><td>WR</td></tr><tr><td>D5</td><td>RD</td></tr><tr><td>D4</td><td>CS</td></tr><tr><td>D3</td><td>A1</td></tr><tr><td>D2</td><td>A0</td></tr><tr><td>D1</td><td>CLK2</td></tr><tr><td>D0</td><td>OUT2</td></tr><tr><td>CLK0</td><td>Gate2</td></tr><tr><td>OUT0</td><td>CLK1</td></tr><tr><td>Gate0</td><td>Gate1</td></tr><tr><td>GND</td><td>OUT1</td></tr></table>	D7	Vcc	D6	WR	D5	RD	D4	CS	D3	A1	D2	A0	D1	CLK2	D0	OUT2	CLK0	Gate2	OUT0	CLK1	Gate0	Gate1	GND	OUT1	<table><tr><td>CS</td><td>8</td><td>Vcc</td></tr><tr><td>WR</td><td>2</td><td>A0</td></tr><tr><td>RD</td><td>5</td><td>INTA</td></tr><tr><td>D7</td><td>I</td><td>IR7</td></tr><tr><td>D6</td><td>n</td><td>IR6</td></tr><tr><td>D5</td><td>t</td><td>IR5</td></tr><tr><td>D4</td><td>r</td><td>IR4</td></tr><tr><td>D3</td><td>o</td><td>IR3</td></tr><tr><td>D2</td><td>n</td><td>IR2</td></tr><tr><td>D1</td><td>t</td><td>IR1</td></tr><tr><td>D0</td><td>o</td><td>IR0</td></tr><tr><td>CAS0</td><td>I</td><td>INT</td></tr><tr><td>CAS1</td><td>e</td><td>SP/EN</td></tr><tr><td>GND</td><td>r</td><td>CAS2</td></tr></table>	CS	8	Vcc	WR	2	A0	RD	5	INTA	D7	I	IR7	D6	n	IR6	D5	t	IR5	D4	r	IR4	D3	o	IR3	D2	n	IR2	D1	t	IR1	D0	o	IR0	CAS0	I	INT	CAS1	e	SP/EN	GND	r	CAS2	<table><tr><td>PA3</td><td>PA4</td></tr><tr><td>PA2</td><td>8</td><td>PA5</td></tr><tr><td>PA1</td><td>5</td><td>PA6</td></tr><tr><td>PA0</td><td>5</td><td>PA7</td></tr><tr><td>RD</td><td>p</td><td>WR</td></tr><tr><td>CS</td><td>e</td><td>RESET</td></tr><tr><td>GND</td><td>i</td><td>D0</td></tr><tr><td>A1</td><td>p</td><td>D1</td></tr><tr><td>A0</td><td>h</td><td>D2</td></tr><tr><td>PC7</td><td>d</td><td>D3</td></tr><tr><td>PC6</td><td>a</td><td>D4</td></tr><tr><td>PC5</td><td>D5</td><td></td></tr><tr><td>PC4</td><td>I</td><td>D6</td></tr><tr><td>PC0</td><td>D7</td><td></td></tr><tr><td>PC1</td><td>Vcc</td><td></td></tr><tr><td>PC2</td><td>PB7</td><td></td></tr><tr><td>PC3</td><td>PB6</td><td></td></tr><tr><td>PB0</td><td>PB5</td><td></td></tr><tr><td>PB1</td><td>PB4</td><td></td></tr><tr><td>PB2</td><td>PB3</td><td></td></tr></table>	PA3	PA4	PA2	8	PA5	PA1	5	PA6	PA0	5	PA7	RD	p	WR	CS	e	RESET	GND	i	D0	A1	p	D1	A0	h	D2	PC7	d	D3	PC6	a	D4	PC5	D5		PC4	I	D6	PC0	D7		PC1	Vcc		PC2	PB7		PC3	PB6		PB0	PB5		PB1	PB4		PB2	PB3		<table><tr><td>Vss</td><td>VS</td></tr><tr><td>RESET</td><td>HS</td></tr><tr><td>LPSTB</td><td>RA0</td></tr><tr><td>MA0</td><td>RA1</td></tr><tr><td>MA1</td><td>RA2</td></tr><tr><td>MA2</td><td>RA3</td></tr><tr><td>MA3</td><td>RA4</td></tr><tr><td>MA4</td><td>D0</td></tr><tr><td>MA5</td><td>H</td><td>D1</td></tr><tr><td>MA6</td><td>D</td><td>D2</td></tr><tr><td>MA7</td><td>6</td><td>D3</td></tr><tr><td>MA8</td><td>5</td><td>D4</td></tr><tr><td>MA9</td><td>0</td><td>D5</td></tr><tr><td>MA10</td><td>D6</td><td></td></tr><tr><td>MA11</td><td>D7</td><td></td></tr><tr><td>MA12</td><td>CS</td><td></td></tr><tr><td>MA13</td><td>RS</td><td></td></tr><tr><td>DE</td><td>E</td><td></td></tr><tr><td>CUR</td><td>R/W</td><td></td></tr><tr><td>Vcc</td><td>CLK</td><td></td></tr></table>	Vss	VS	RESET	HS	LPSTB	RA0	MA0	RA1	MA1	RA2	MA2	RA3	MA3	RA4	MA4	D0	MA5	H	D1	MA6	D	D2	MA7	6	D3	MA8	5	D4	MA9	0	D5	MA10	D6		MA11	D7		MA12	CS		MA13	RS		DE	E		CUR	R/W		Vcc	CLK		<table><tr><td>TEST0</td><td>Vcc</td></tr><tr><td>XTAL1</td><td>TEST1</td></tr><tr><td>XTAL2</td><td>P27</td></tr><tr><td>RESET</td><td>P26</td></tr><tr><td>THSS</td><td>P25</td></tr><tr><td>CS</td><td>P24</td></tr><tr><td>TLEA</td><td>P17</td></tr><tr><td>RD</td><td>P16</td></tr><tr><td>A0</td><td>V</td><td>P15</td></tr><tr><td>WR</td><td>T</td><td>P14</td></tr><tr><td>SYNC</td><td>2</td><td>P13</td></tr><tr><td>D0</td><td>8</td><td>P12</td></tr><tr><td>D1</td><td>4</td><td>P11</td></tr><tr><td>D2</td><td>2</td><td>P10</td></tr><tr><td>D3</td><td>THSSP</td><td></td></tr><tr><td>D4</td><td>THPR</td><td></td></tr><tr><td>D5</td><td>P23</td><td></td></tr><tr><td>D6</td><td>P23</td><td></td></tr><tr><td>D7</td><td>P21</td><td></td></tr><tr><td>GND</td><td>P20</td><td></td></tr></table>	TEST0	Vcc	XTAL1	TEST1	XTAL2	P27	RESET	P26	THSS	P25	CS	P24	TLEA	P17	RD	P16	A0	V	P15	WR	T	P14	SYNC	2	P13	D0	8	P12	D1	4	P11	D2	2	P10	D3	THSSP		D4	THPR		D5	P23		D6	P23		D7	P21		GND	P20		<table><tr><td>Red</td><td>Vdd</td></tr><tr><td>Green</td><td>RS1</td></tr><tr><td>Blue</td><td>I</td><td>RS0</td></tr><tr><td>IRef</td><td>M</td><td>WR</td></tr><tr><td>P0</td><td>G</td><td>D7</td></tr><tr><td>P1</td><td>1</td><td>D6</td></tr><tr><td>P2</td><td>7</td><td>D5</td></tr><tr><td>P3</td><td>P</td><td>D4</td></tr><tr><td>P4</td><td>D3</td><td></td></tr><tr><td>P5</td><td>D2</td><td></td></tr><tr><td>P6</td><td>D1</td><td></td></tr><tr><td>P7</td><td>D0</td><td></td></tr><tr><td>PCLK</td><td>Blank</td><td></td></tr><tr><td>Vss</td><td>RD</td><td></td></tr></table>	Red	Vdd	Green	RS1	Blue	I	RS0	IRef	M	WR	P0	G	D7	P1	1	D6	P2	7	D5	P3	P	D4	P4	D3		P5	D2		P6	D1		P7	D0		PCLK	Blank		Vss	RD		<table><tr><td>Vss</td><td>CA1</td></tr><tr><td>PA0</td><td>CA2</td></tr><tr><td>PA1</td><td>IRQA</td></tr><tr><td>PA2</td><td>IRQB</td></tr><tr><td>PA3</td><td>RS0</td></tr><tr><td>PA4</td><td>RS1</td></tr><tr><td>PA5</td><td>RESET</td></tr><tr><td>PA6</td><td>D0</td></tr><tr><td>PA7</td><td>M</td><td>D1</td></tr><tr><td>PB0</td><td>C</td><td>D2</td></tr><tr><td>PB1</td><td>8</td><td>D3</td></tr><tr><td>PB2</td><td>B</td><td>D4</td></tr><tr><td>PB3</td><td>1</td><td>D5</td></tr><tr><td>PB4</td><td>D6</td><td></td></tr><tr><td>PB5</td><td>D7</td><td></td></tr><tr><td>PB6</td><td>E</td><td></td></tr><tr><td>PB7</td><td>CS1</td><td></td></tr><tr><td>CB1</td><td>CS2</td><td></td></tr><tr><td>CB2</td><td>CS0</td><td></td></tr><tr><td>Vcc</td><td>R/W</td><td></td></tr></table>	Vss	CA1	PA0	CA2	PA1	IRQA	PA2	IRQB	PA3	RS0	PA4	RS1	PA5	RESET	PA6	D0	PA7	M	D1	PB0	C	D2	PB1	8	D3	PB2	B	D4	PB3	1	D5	PB4	D6		PB5	D7		PB6	E		PB7	CS1		CB1	CS2		CB2	CS0		Vcc	R/W	
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Intel Chips

## Intel Chips

## Memory Chips RAM & EEPROM

NC	Vcc	A14	Vcc	NC	Vcc	A18	Vcc	A14	Vcc	A14	Vcc
A12	WE	A12	WE	A16	A15	A16	A15	A12	WE	A12	WE
A7	A	A7	A	A14	A	A14	A	A7	A	A7	A
A6	T	A6	T	A12	S	A12	S	A6	T	A6	T
A5	8	A5	8	A7	C	A7	C	A5	8	A5	8
A4	C	A4	C	A6	1	A6	1	A4	6	A4	6
A3	4	A3	2	A5	0	A5	0	A3	S	A3	S
A2	B	A2	5	A4	8	A4	8	A2	A	A2	A
A1	CE	A1	6	A3	OE	A3	OE	A1	CE	A1	CE
A0	1/O7	A0	1/O7	A2	A10	A2	A10	A0	1/O7	A0	1/O7
1/O0	1/O6	1/O0	1/O6	A1	CE	A1	CE	1/O0	1/O6	1/O0	1/O6
1/O1	1/O5	1/O1	1/O5	A0	DQ7	A0	DQ7	1/O1	1/O5	1/O1	1/O5
1/O2	1/O4	1/O2	1/O4	DQ0	DQ6	DQ0	DQ6	1/O2	1/O4	1/O2	1/O4
Vss	1/O3	Vss	1/O3	DQ1	DQ5	DQ1	DQ5	Vss	1/O3	Vss	1/O3
				DQ2	DQ4	DQ2	DQ4				
				Vss	DQ3	Vss	DQ3				

74 Series Logic Chips (0I indicate zero indexed)

Dir	Vcc	Dir	Vcc	G1	Vcc	OE	Vcc	OE	Vcc	OE	Vcc	OE	Vcc	OE	Vcc
A0	7	A0	7	A0	7	0D	7	0D	7	0D	7	0D	7	0D	7
A1	4	A1	4	A1	4	1D	4	1D	4	1D	4	1D	4	1D	4
A2	A	A2	A	A2	A	2D	L	2D	L	2D	L	2D	L	2D	L
A3	S	A3	S	A3	S	3D	S	3D	S	3D	S	3D	S	3D	S
A4	2	A4	2	A4	2	4D	7	4D	7	4D	7	4D	7	4D	7
A5	4	A5	5	A5	4	5D	3	5D	3	5D	4	5D	4	5D	5
A6	B5	A6	B5	A6	0	6D	0	6D	0	6D	0	6D	0	6D	0
A7	0	A7	0	A7	A	7D	1	7D	1	7D	1	7D	1	7D	1
A8	B1	A8	B1	A8	Y	GND	LE	GND	LE	GND	CLK	GND	CLK	GND	CLK
A9	B7	A9	B7	A9	Y0										

SV	GND	D7	D6	D5	D4
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MEMR	MEMW	A18	A17	A16
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Q0	Q1	Q2	Q3	RA0
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CEC	Vcc	R/W	CEC	A11L	R/WR	A10L	A11R	OE	A10R	A0L	OE	A1L	A0R	A2L	A1R	A3L	I	A2R	A4L	T	A3R	A5L	7	A4R	A6L	1	A5R	A7L	4	A6R	A8L	A7R	A9L	A8R	1/O0L	A9R	1/O1L	1/O7R	1/O2L	1/O6R	1/O3L	1/O5R	1/O4L	1/O4R	1/O5L	1/O3R	1/O6L	1/O2R	1/O7L	1/O1R	GND	1/O0R
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## 74 Series Logic Chips (0I indicate zero indexed)

Dir Vcc		Dir Vcc		G1 Vcc		G1 Vcc		OE Vcc		OE Vcc		OE Vcc		OE Vcc		OE Vcc		5V		MEMR		I/O5L I/O3R	
A0 7 OE		A0 7 OE		A6 7 G2		A0 7 G2		0D 7 0Q		0D 7 0Q		0D 7 0Q		0D 7 0Q		0D 7 0Q		GND		MEMW		I/O6L I/O2R	
A1 4 B0		A1 4 B0		A7 4 Y7		A4 4 Y0		1D 4 1Q		1D 4 1Q		1D 4 1Q		1D 4 1Q		1D 4 1Q						I/O7L I/O1R	
A2 A B1		A2 A B1		A5 L Y6		A2 L Y1		2D L 2Q		2D L 2Q		2D L 2Q		2D L 2Q		2D L 2Q						GND I/O0R	
A3 S B2		A3 S B2		A4 S Y5		A3 S Y2		3D S 3Q		3D S 3Q		3D S 3Q		3D S 3Q		3D S 3Q				A19			
A4 2 B3		A4 2 B3		A5 4 Y4		A4 4 Y3		4D 7 4Q		4D 7 4Q		4D 7 4Q		4D 7 4Q		4D 7 4Q				A18			
A5 S B4		A5 S B4		A2 1 Y3		A5 1 Y4		5D 3 5Q		5D 3 5Q		5D 4 5Q		5D 4 5Q		5D 4 5Q							
A6 B5		A6 B5		A1 0 Y2		A6 0 Y5		6D 0 6Q		6D 0 6Q		6D 0 6Q		6D 0 6Q		6D 0 6Q				A17			
A7 0 B6		A7 0 B6		A0 1 Y1		A7 R Y6		7D 1 7Q		7D 1 7Q		7D 1 7Q		7D 1 7Q		7D 1 7Q				A16			
GND B7		GND B7		GND Y0		GND Y7		GND LE		GND LE		GND CLK		GND CLK		GND CLK							
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																				A14		Q1	
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																						PA6	
																						NMI	
																						RST	
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