Selecting Decoupling Capacitors for Atmel's PLDs

Erasable Programmable Logic Device

Application Note

Introduction

This application note provides a summary of information needed when selecting decoupling capacitors for Atmel Programmable Logic Devices. A 0.22 mF, multi-layer ceramic or plastic dielectric capacitor is recommended for such use. Either surface-mount (SMD) or radial-leaded devices should be used. Because of their high parasitic resistance and/or inductance, tantalum, aluminum electrolytic, and axially leaded capacitors are not recommended.

When is a Capacitor Not a Capacitor

Unfortunately, capacitors are not the perfect charge storage devices we would like them to be. Their lead wires and internal construction create parasitic resistance and inductance in series with the capacitance. These parasitics are usually referred to as ESR (equivalent series resistance) and ESL (equivalent series inductance), respectively. As will be shown, these parasitics can seriously reduce the ability of many types of capacitors to decouple supply noise in high-speed systems. Table 1 gives typical ESR and ESL values for various types of capacitors.

As shown, ESR values range from 0.01 ohm to as high as 9 ohms. ESL varies from 2 nH for typical surface mount devices to 20 nH for electrolytic capacitors. These numbers are typical values, taken from data from several manufacturers. As expected, there is some variation between manufacturers. Also, worst case specification values will be significantly higher, especially for ESR values.

How ESR and ESL Can Affect High Speed Operation

The effects of these parasitics may be best illustrated by a simple example. Consider the case of a 22V10L. In the standby mode, Icc current is typically only 5 mA. When an input switches, I_{CC} may temporarily go as high as 100 mA. This increase in current draws charge from the local decoupling capacitor. This capacitor current will create voltage drops across the ESR and ESL parasitic elements. To see how these voltage drops can cause problems in a system, look at a typical decoupling application.

In this example the design goal of the capacitor is to keep local supply noise below 0.2 volts, a reasonable expectation. This immediately sets an upper limit on ESR of 2 ohms.

$ESR_{max} = V_{noise} / I_{max}$

I_{max} = Highest Expected Capacitor Current

The upper limit on ESL is determined by how quickly the capacitor's current must change, as well as how much supply noise will be tolerated during that change. For high-speed logic devices, I_{CC} must be able to switch from standby to active levels within 2 to 3 nanoseconds.

$ESL_{max} = V_{noise} \cdot I_{max} / \Delta t;$

Δt = Time allowed for capacitor current to switch

In this example, an upper limit on ESL of 4 to 6 nH is set.

Consider what can happen if these limits are exceeded. If an axially leaded multilayer ceramic capacitor with ESR of 0.15 ohm is used, the resistance drop in

Rev. 0484C–09/99

our application will not be significant (100 mA × 0.15 ohm = 15 mV). However, the inductance will not allow the current to reach 100 mA in 6 nanoseconds. This can slow the logic device switching by several nanoseconds.

What Types to Use: Multi-layered Ceramic and Plastic Dielectrics

From this example, it is apparent that the parasitic elements on capacitors can easily limit their telecopying ability. Therefore, users of high-speed logic need to pick their capacitors with care. The data in Table 1 shows that the best bets are surface-mount, multi-layered ceramic (MLC) or plastic dielectrics. Of the leaded devices, only radial types are recommended.

Within the MLCs, there are different classes of dielectric. Class I has the best characteristics, but its small dielectric constant makes it impractical for decoupling values. Class II is highly recommended, as it has good temperature stability (percent variation -55°C to 125°C) and aging characteristics (10 percent in ten years). Class III, on the other hand, drops to less than 50 percent of its rated capacitance at 85°C, and to only 25 percent at -55°C. Class III dielectric also loses 20 percent of its rated value in ten years. Therefore, Class III MLCs are only recommended for applications where temperature excursions are minimal.

Plastic dielectric capacitors in general offer performance as good as Class II MLCs. Among the dielectrics available today are polypropylene, polyester, polycarbonate, polystyrene and teflon. Capacitance variation with temperature depends on the particular material, but is generally less than ±20 percent from -55°C to 125°C. Aging is minimal, usually less than 2 percent in 10 years. Unfortunately, not many manufacturers make surface-mount plastic dielectric capacitors. That should change soon, as surface-mount technology advances and becomes more common.

When using radial leaded cases, be sure to minimize lead lengths, as ESL increases quickly with longer leads. For example, if a capacitor has 6 nH of inductance with 2 mm leads, extending leads to 5 mm will increase ESL to 10 nH.

What Types Not to Use: Aluminum Electrolytic, Tantalum, and Anything Axial

The design example above together with the numbers given in Table 1 show that some types are not suitable at all for decoupling high-speed devices. Specifically, the high inductance of axially leaded capacitors puts them on the “don’t use” list. Also, tantalum and aluminum electrolytic devices are generally not recommended, as they have high ESR and/or ESL, even in radial and surface-mount configurations.

In Any Case, Know Your ESL and ESR

ESR data is often found in catalogs. However, this will normally be only low-frequency data, and ESR is frequency dependent (dropping at higher f). ESL data is not usually given in catalogs. The best thing to do is get Z versus frequency data from the manufacturer. From such a graph (with frequency up to at least 10 MHz), you can extract high frequency ESR and ESL.

How Much Capacitance Do You Need

For decoupling Atmel’s PLDs a 0.22 µF capacitor is recommended. In many cases, this will be overkill. However, determining how much less you could get by with for a particular application is dependent upon several factors. The number of PC board supply planes, the board’s dielectric thickness and dielectric constant, the value (*and* ESR *and* ESL!) of power entry decoupling capacitors, among other things, will determine just how much is really needed. The best bet is to use a good 0.22 µF and be safe. Besides, the more decoupling is taken care of by local capacitors, the lower the board’s HF emissions will be.

Summary

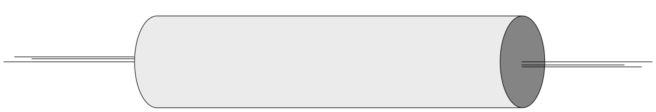
Choosing the right decoupling capacitor is an important part of high-speed circuit design. Choosing the wrong one can introduce supply noise that can slow down signal switching or even end up giving incorrect data. For decoupling Atmel PLDs, 0.22 µF capacitors are recommended. These should be of either multi-layer ceramic or plastic dielectric type. Surface-mount devices are best, with radial leaded cases also being acceptable.

Table 1.

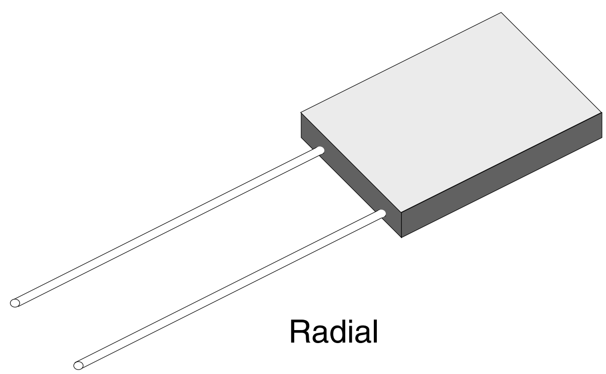
Dielectric	Body	L (nH,typ)	R (ohm,typ)	Rating	Comments
Ceramic II	SMD	2	0.02	E	Highly recommended
	Radial	6	0.07	G	Keep leads short
	Axial	12	0.07	S	Axial always = Higher L
Ceramic III	SMD	2	0.04	G	C loss hot/cold/old
	Radial	6	0.15+	S	
	Axial	12	0.15+	X	
Plastics	SMD	2	0.03	E	Hard to find
	Radial	5+	0.01+	G	Get R and L data
	Axial	12+	0.01+	X	
Aluminum Electrolytic	SMD	13	9.0	X	Forget it
	Radial	15+	1.5+	X	
	Axial	20	1.5	X	
Tantalum	SMD	?	3.0	X	
	Radial	10+	1.0	X	
	Axial	15+	1.0	X	

Ratings code:

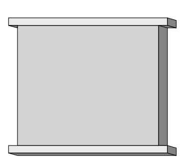
E Excellent; highly recommended
G Good; will perform well in most applications
S Satisfactory; be aware of specific vendor's device performance
X Not recommended



Axial



Radial



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