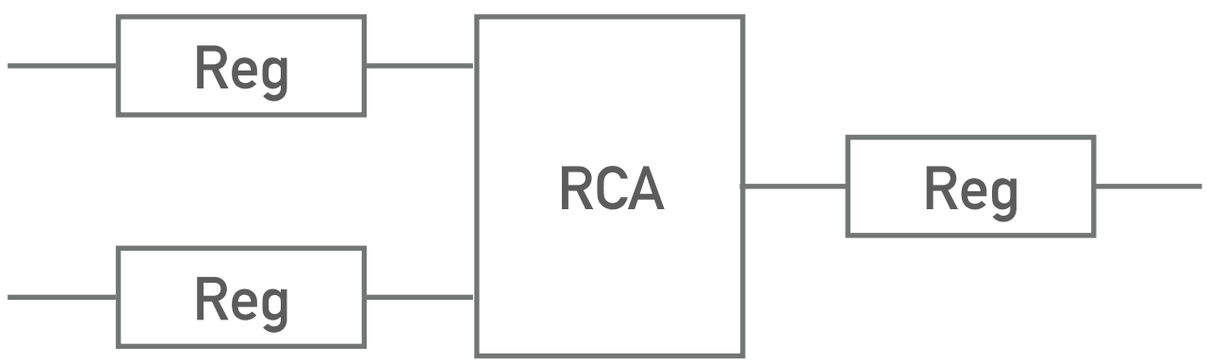
FILE FORMAT

Project 7 - Design environment for FPGA-based Designs

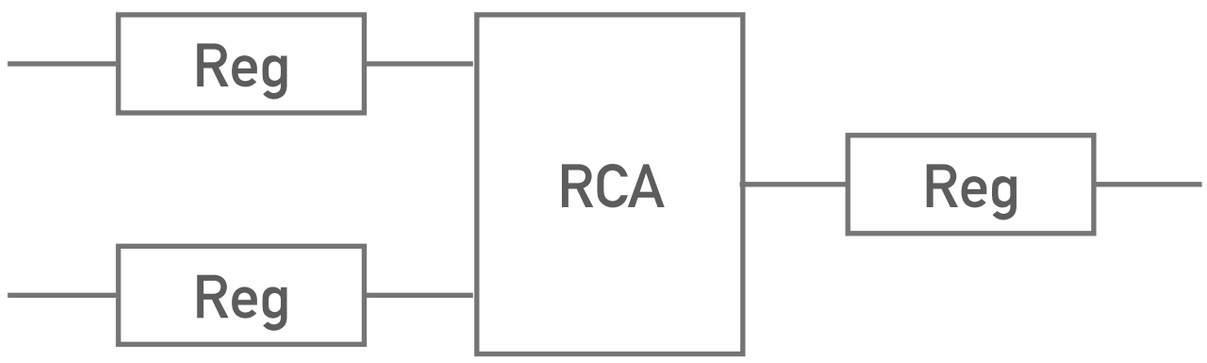
TOP LEVEL CODE GENERATOR MODULE

- Top-Level-Code-Generator module - the module to generate top-level VHDL files by 2 character files:
  - IP information file
  - Signal information file
- These 2 input files contains all the information we need to describe a system. For example, let's consider a system with 3 registers and 1 RCA:



EXAMPLE

- We need to logically define IDs for IP components and signals. Then we put corresponding IP component and signal information into IP information file and signal information file respectively.
  - IP component - The instance of IP core with its own function
  - Signal - Describe the topology connection between two components



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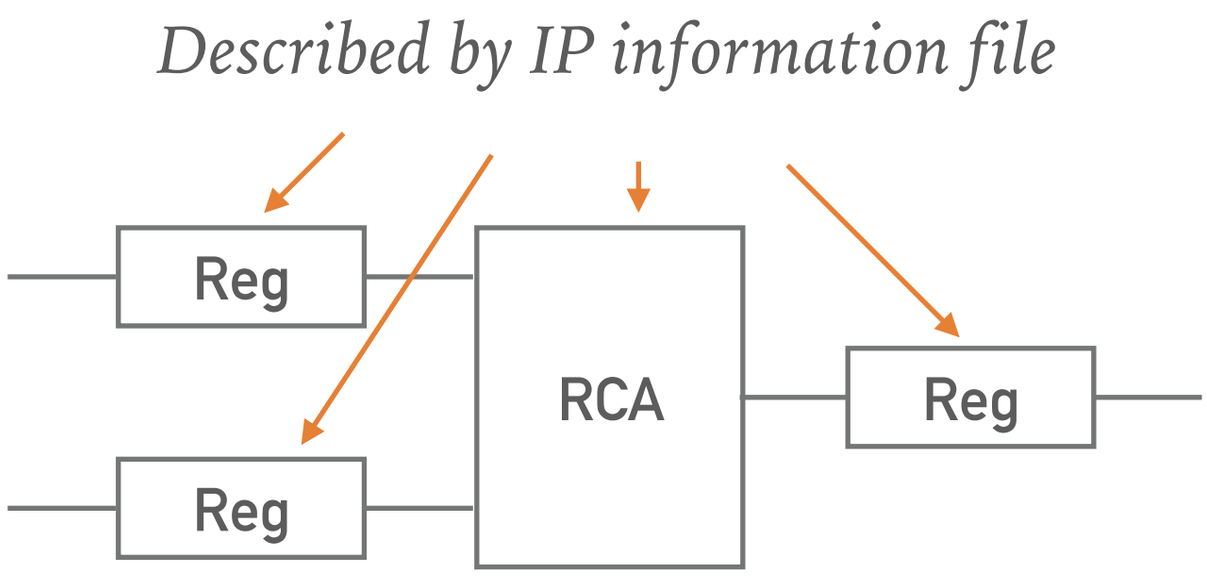

EXAMPLE

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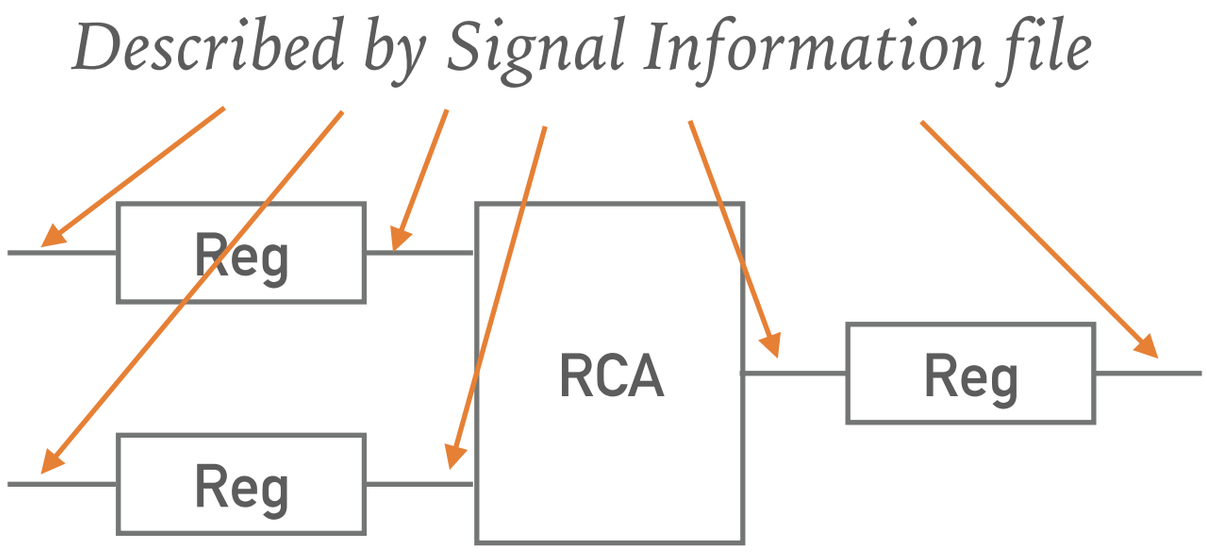
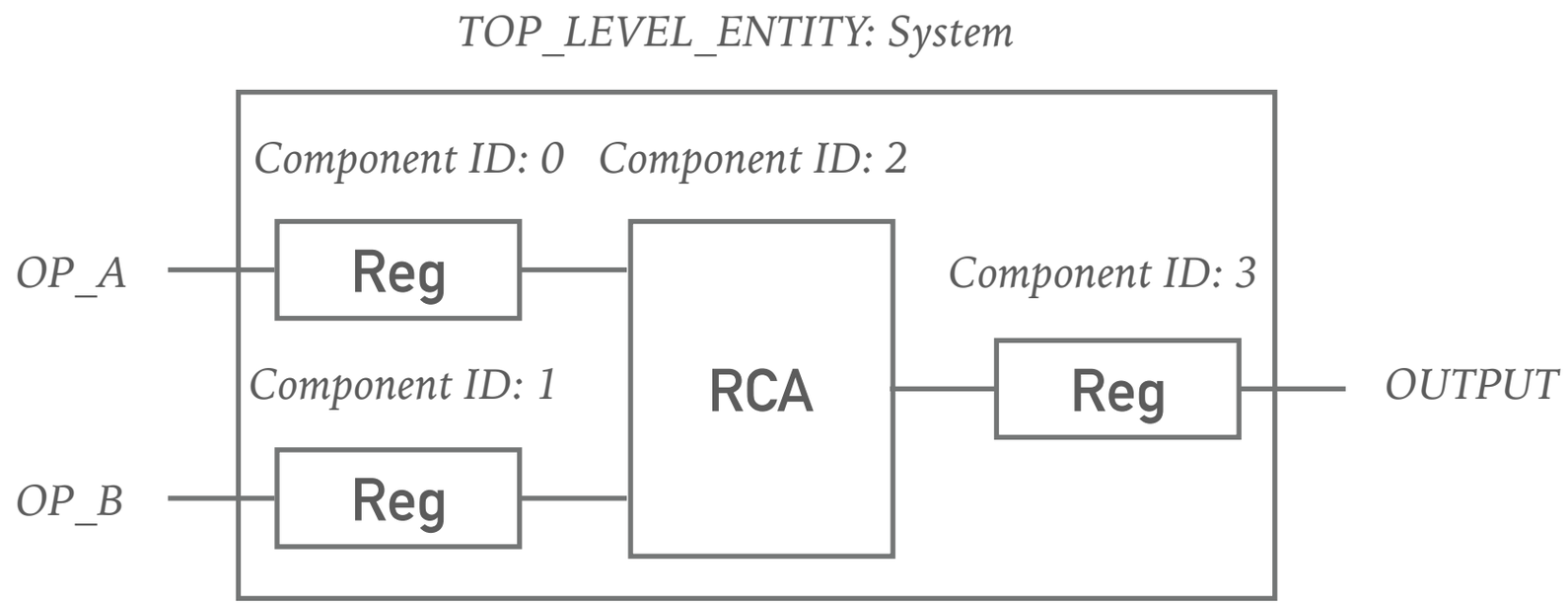


IP INFORMATION FILE

- Key Information in IP information file
  - IP ID
    - ID of corresponding IP component
    - The value is assigned by GUI
  - IP Name
    - Name of corresponding IP component
  - Input port number and output port number
  - Port information
    - Port name
    - Port type
    - Port ID
    - Port direction
  - Instance component ID
    - Component ID in current system
    - One IP may have various instance component ID

IP INFORMATION FILE

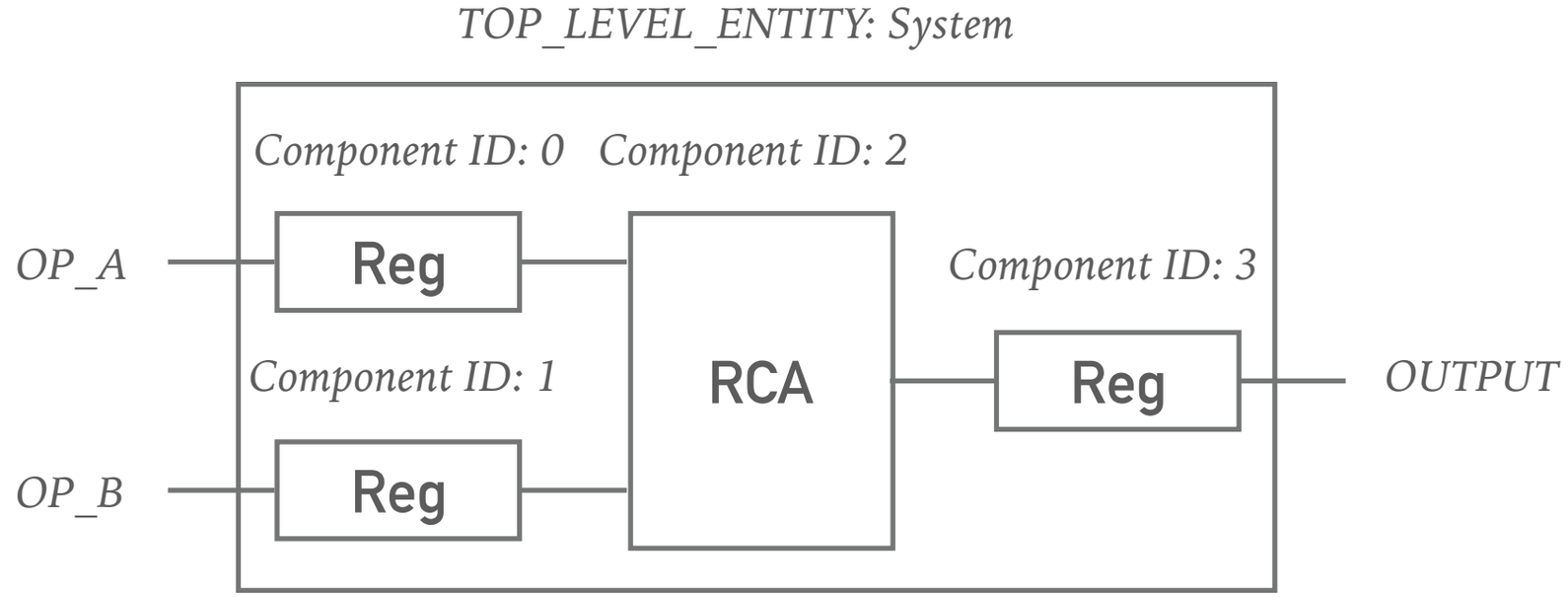
- Example




```
0 System 2 1
OP_A std_logic_vector(7 downto 0) 0 in
OP_B std_logic_vector(7 downto 0) 1 in
OUTPUT std_logic_vector(7 downto 0) 2 out
0
1 Reg_8 1 1
data_in std_logic_vector(7 downto 0) 0 in
data_out std_logic_vector(7 downto 0) 1 out
1 2 4
2 RCA 2 1
A std_logic_vector(7 downto 0) 0 in
B std_logic_vector(7 downto 0) 1 in
OUT std_logic_vector(7 downto 0) 2 out
3
```

IP INFORMATION FILE

- Example



TOP_LEVEL_ENTITY: System

```
0 System 2 1
OP_A std_logic_vector(7 downto 0) 0 in
OP_B std_logic_vector(7 downto 0) 1 in
OUTPUT std_logic_vector(7 downto 0) 2 out
0
```

IP 1: Reg_8

```
1 Reg_8 1 1
data_in std_logic_vector(7 downto 0) 0 in
data_out std_logic_vector(7 downto 0) 1 out
1 2 4
```

IP 2: RCA

```
2 RCA 2 1
A std_logic_vector(7 downto 0) 0 in
B std_logic_vector(7 downto 0) 1 in
OUT std_logic_vector(7 downto 0) 2 out
3
```

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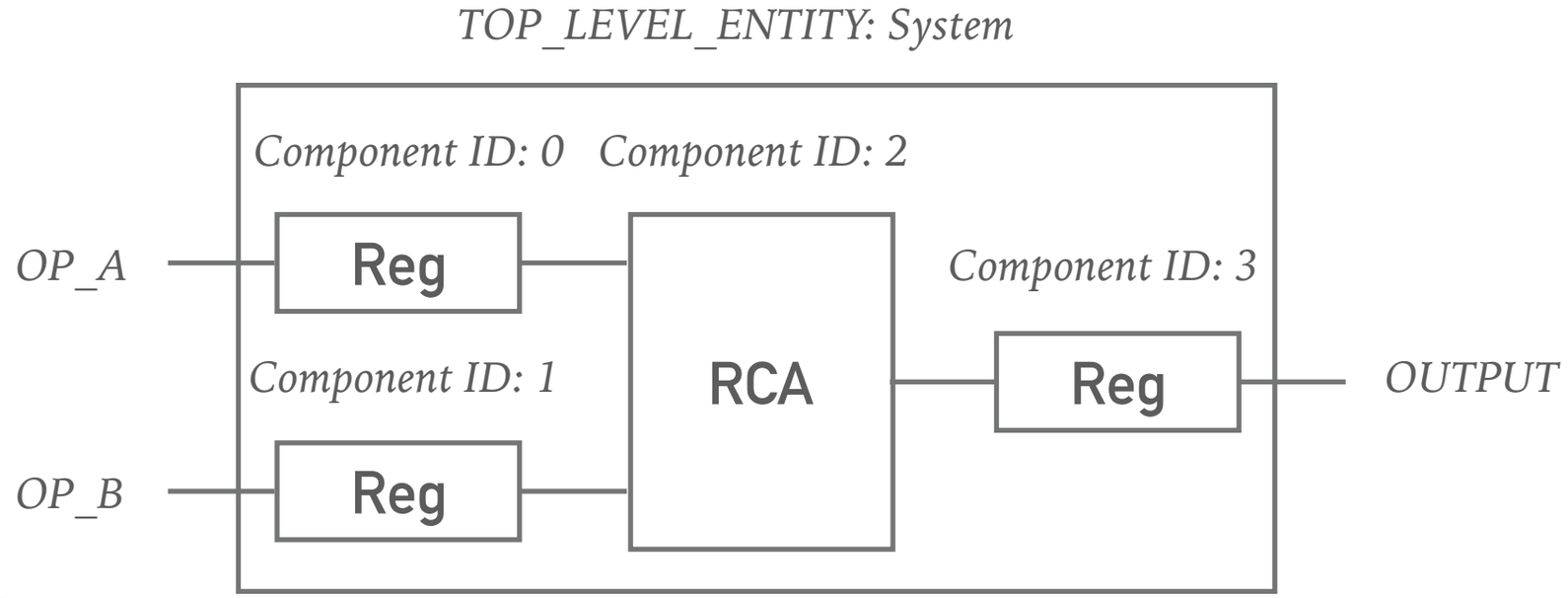
IP INFORMATION FILE

- Example



TOP_LEVEL_ENTITY: System

IP_ID = 0 →

```
0 System 2 1
OP_A std_logic_vector(7 downto 0) 0 in
OP_B std_logic_vector(7 downto 0) 1 in
OUTPUT std_logic_vector(7 downto 0) 2 out
0
```

ID of Top Level entity is always 0

IP 1: Reg_8

IP_ID = 1 →

```
1 Reg_8 1 1
data_in std_logic_vector(7 downto 0) 0 in
data_out std_logic_vector(7 downto 0) 1 out
1 2 4
```

IP 2: RCA

IP_ID = 2 →

```
2 RCA 2 1
A std_logic_vector(7 downto 0) 0 in
B std_logic_vector(7 downto 0) 1 in
OUT std_logic_vector(7 downto 0) 2 out
3
```

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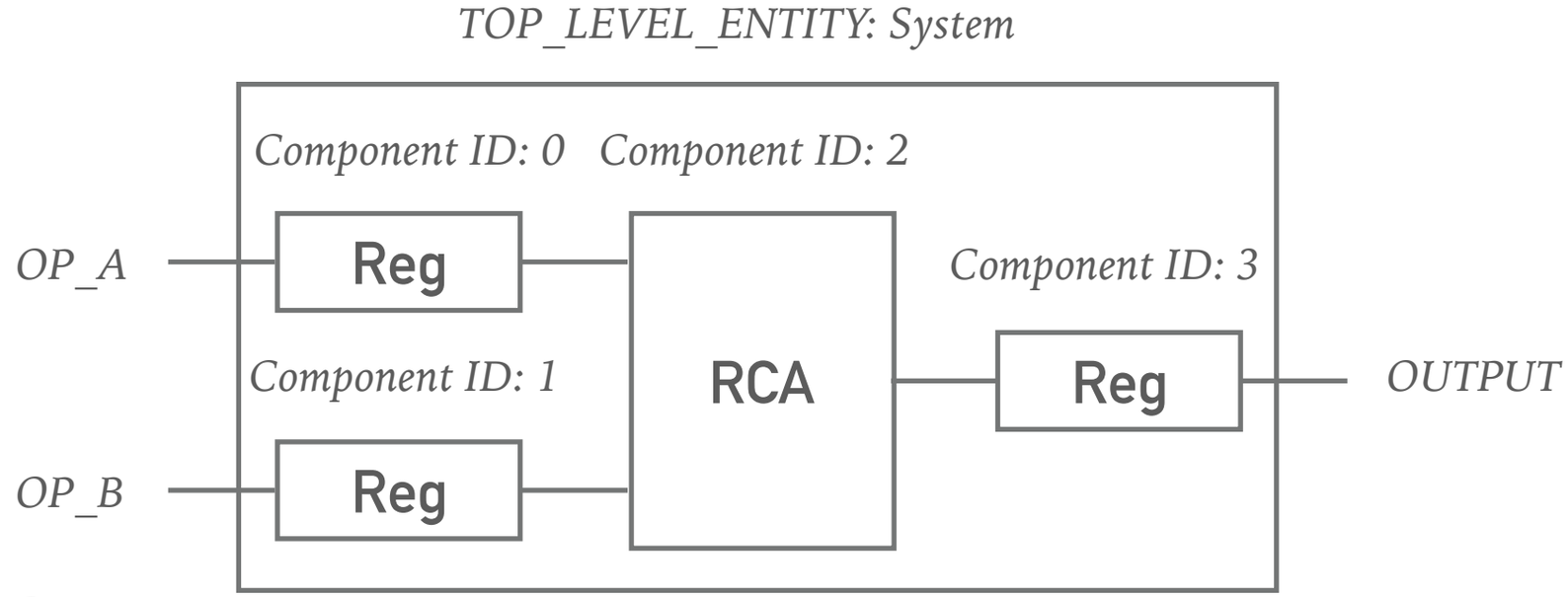
IP INFORMATION FILE

- Example



TOP_LEVEL_ENTITY: System

IP_NAME = System

```
0 System 2 1
OP_A std_logic_vector(7 downto 0) 0 in
OP_B std_logic_vector(7 downto 0) 1 in
OUTPUT std_logic_vector(7 downto 0) 2 out
0
```

IP 1: Reg_8

IP_NAME = Reg_8

```
1 Reg_8 1 1
data_in std_logic_vector(7 downto 0) 0 in
data_out std_logic_vector(7 downto 0) 1 out
1 2 4
```

IP 2: RCA

IP_NAME = RCA

```
2 RCA 2 1
A std_logic_vector(7 downto 0) 0 in
B std_logic_vector(7 downto 0) 1 in
OUT std_logic_vector(7 downto 0) 2 out
3
```

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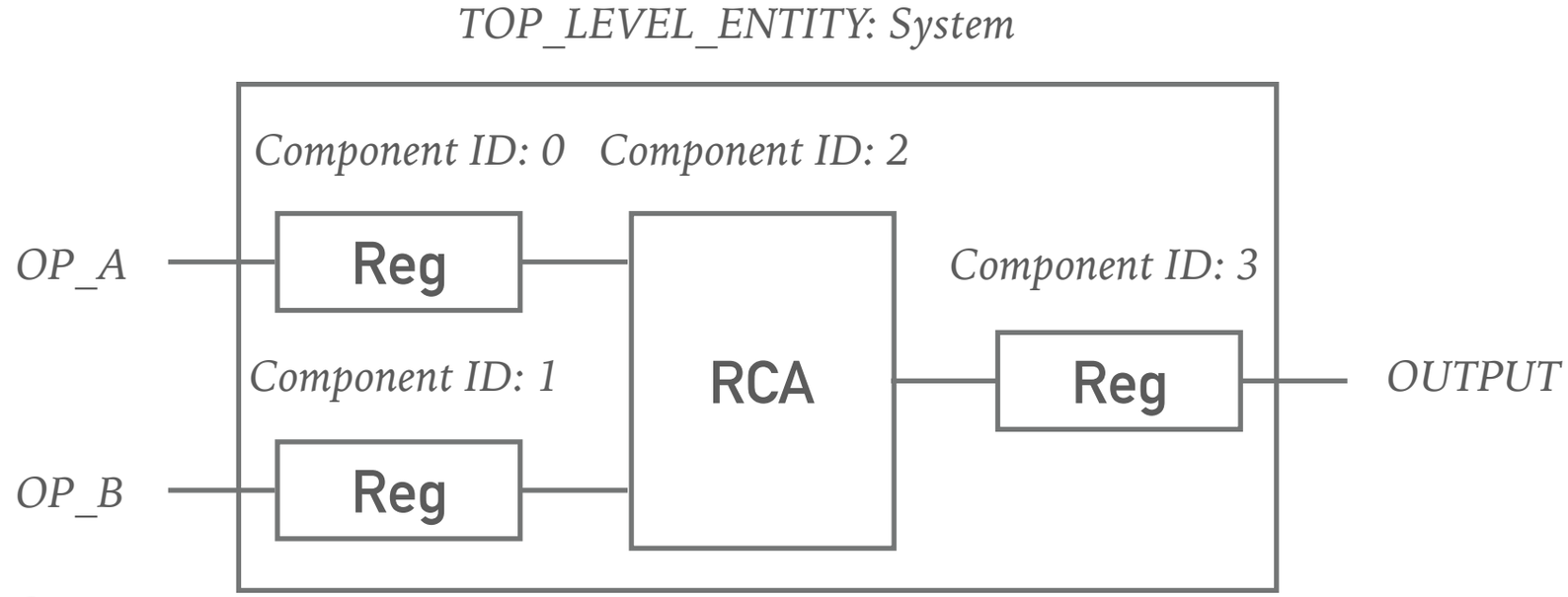
IP INFORMATION FILE

- Example



TOP_LEVEL_ENTITY: System

Input port number = 2
Output port number = 1

IP 1: Reg_8

Input port number = 1
Output port number = 1

IP 2: RCA

Input port number = 2
Output port number = 1

```
0 System 2 1
OP_A std_logic_vector(7 downto 0) 0 in
OP_B std_logic_vector(7 downto 0) 1 in
OUTPUT std_logic_vector(7 downto 0) 2 out
0
1 Reg_8 1 1
data_in std_logic_vector(7 downto 0) 0 in
data_out std_logic_vector(7 downto 0) 1 out
1 2 4
2 RCA 2 1
A std_logic_vector(7 downto 0) 0 in
B std_logic_vector(7 downto 0) 1 in
OUT std_logic_vector(7 downto 0) 2 out
3
```

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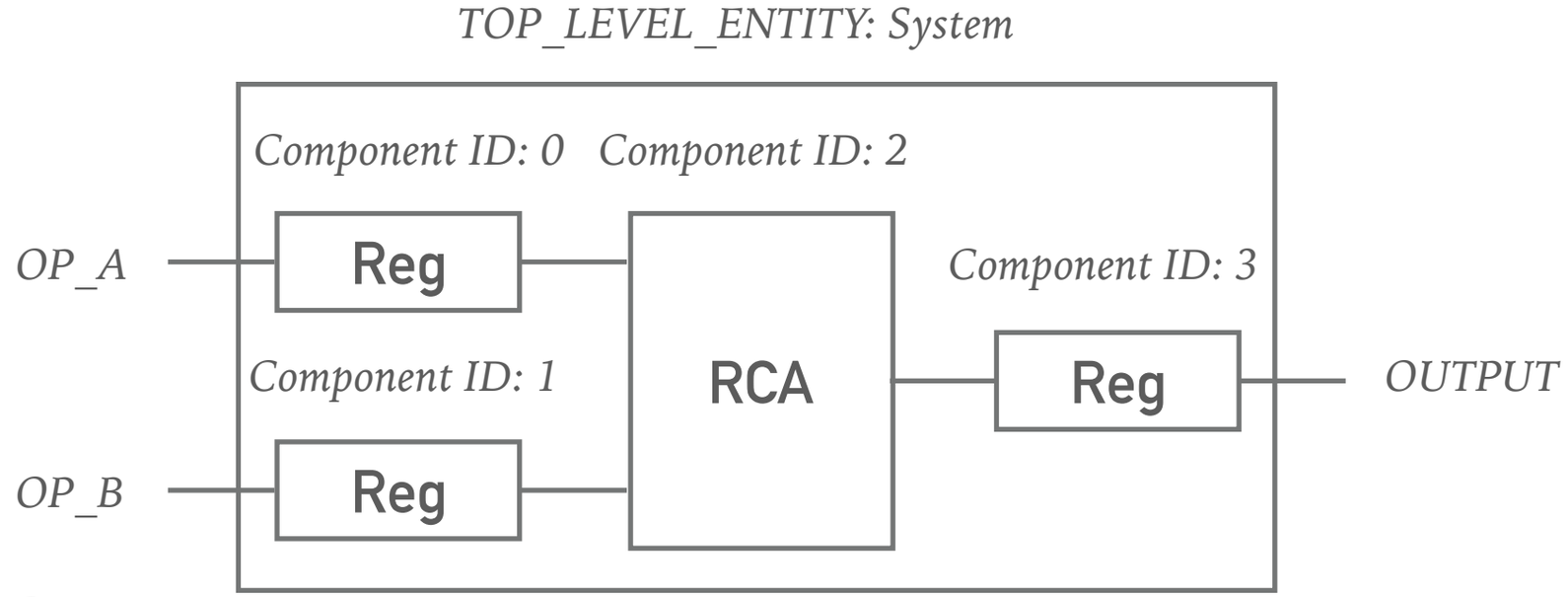
IP INFORMATION FILE

- Example



TOP_LEVEL_ENTITY: System

Port information

```
0 System 2 1
OP_A std_logic_vector(7 downto 0) 0 in
OP_B std_logic_vector(7 downto 0) 1 in
OUTPUT std_logic_vector(7 downto 0) 2 out
0
```

IP 1: Reg_8

Port information

```
1 Reg_8 1 1
data_in std_logic_vector(7 downto 0) 0 in
data_out std_logic_vector(7 downto 0) 1 out
1 2 4
```

IP 2: RCA

Port information

```
2 RCA 2 1
A std_logic_vector(7 downto 0) 0 in
B std_logic_vector(7 downto 0) 1 in
OUT std_logic_vector(7 downto 0) 2 out
3
```

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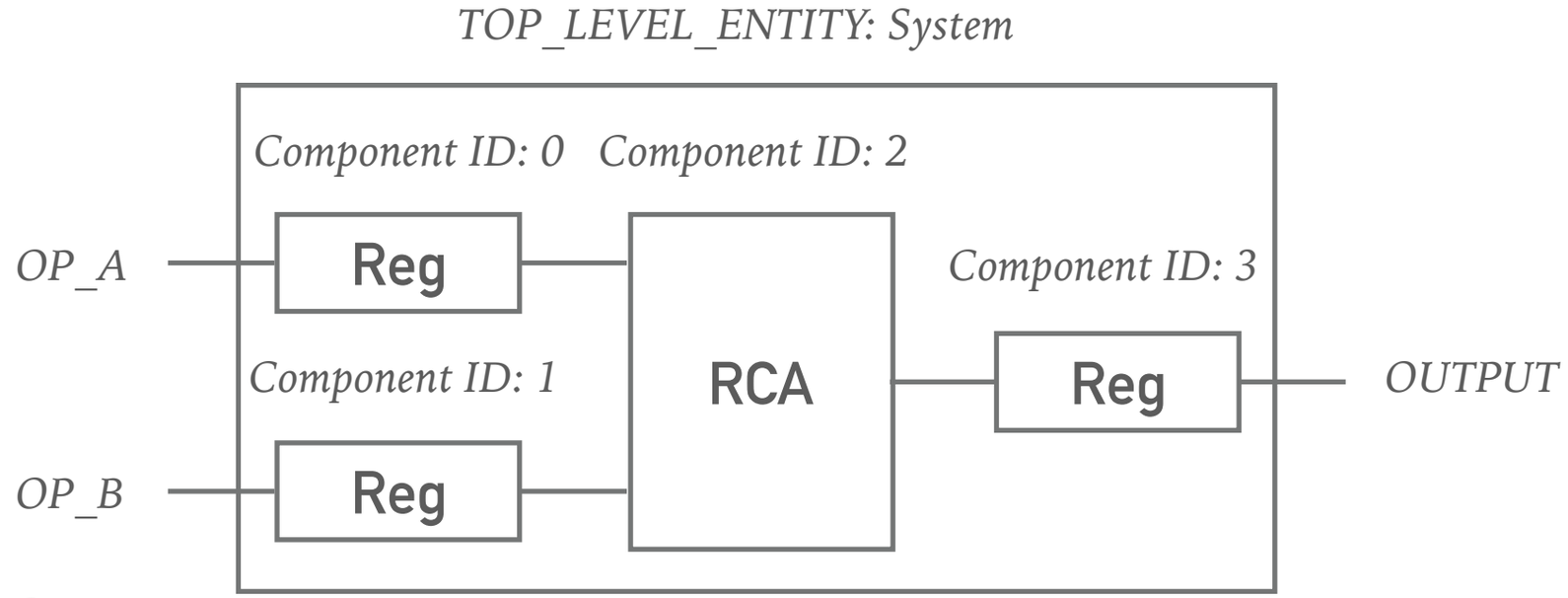
IP INFORMATION FILE

- Example



TOP_LEVEL_ENTITY: System

Instance component ID : 0

IP 1: Reg_8

Instance component ID : 1, 2 and 4

IP 2: RCA

Instance component ID : 3

```
0 System 2 1
OP_A std_logic_vector(7 downto 0) 0 in
OP_B std_logic_vector(7 downto 0) 1 in
OUTPUT std_logic_vector(7 downto 0) 2 out
0
1 Reg_8 1 1
data_in std_logic_vector(7 downto 0) 0 in
data_out std_logic_vector(7 downto 0) 1 out
1 2 4
2 RCA 2 1
A std_logic_vector(7 downto 0) 0 in
B std_logic_vector(7 downto 0) 1 in
OUT std_logic_vector(7 downto 0) 2 out
3
```

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SIGNAL INFORMATION FILE

- Key Information in signal information file
  - Signal ID
    - ID of signal
    - The value is assigned by GUI
  - Departure component ID
    - Component ID which the connection departs from
  - Departure port ID
    - Port ID which the connection departs from
  - Destination component ID
    - Component ID which the connection arrives
  - Destination port ID
    - Port ID which the connection arrives

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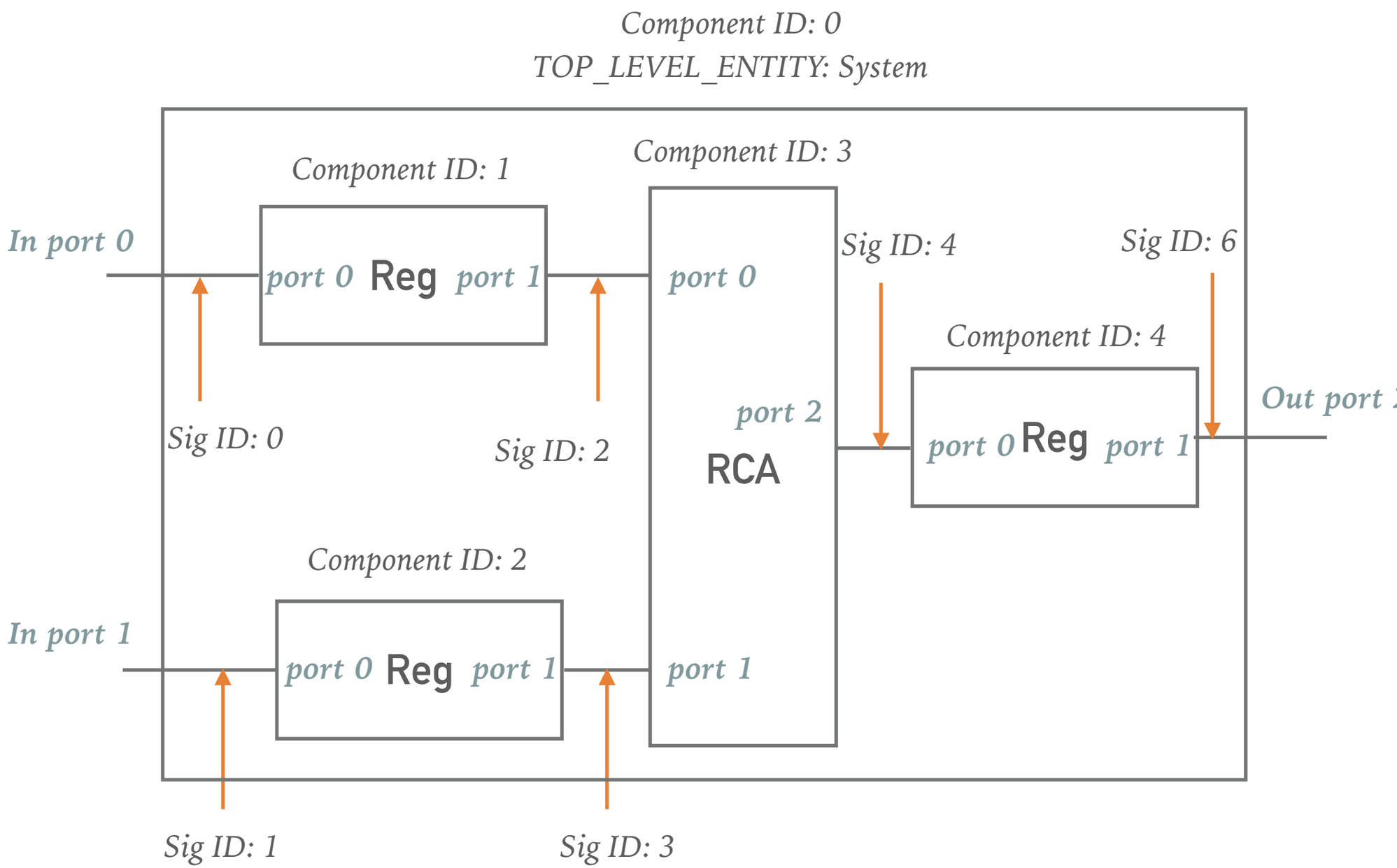
SIGNAL INFORMATION FILE

- Example

0	0	0	1	0
1	0	1	2	0
2	1	1	3	0
3	2	1	3	1
4	3	2	4	0
6	4	1	0	2



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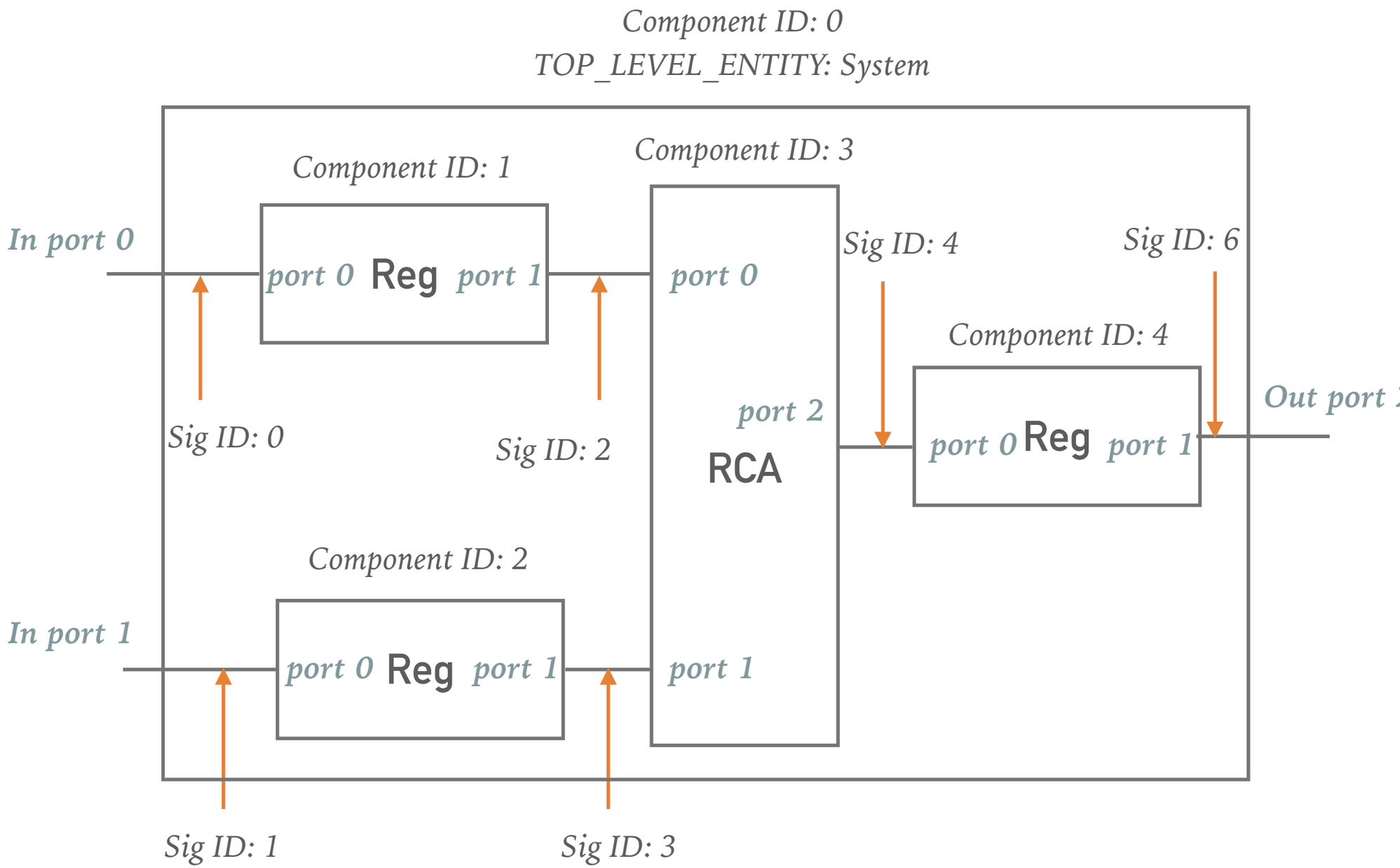
SIGNAL INFORMATION FILE

- Example

0	0	0	1	0
1	0	1	2	0
2	1	1	3	0
3	2	1	3	1
4	3	2	4	0
6	4	1	0	2

Signal_id



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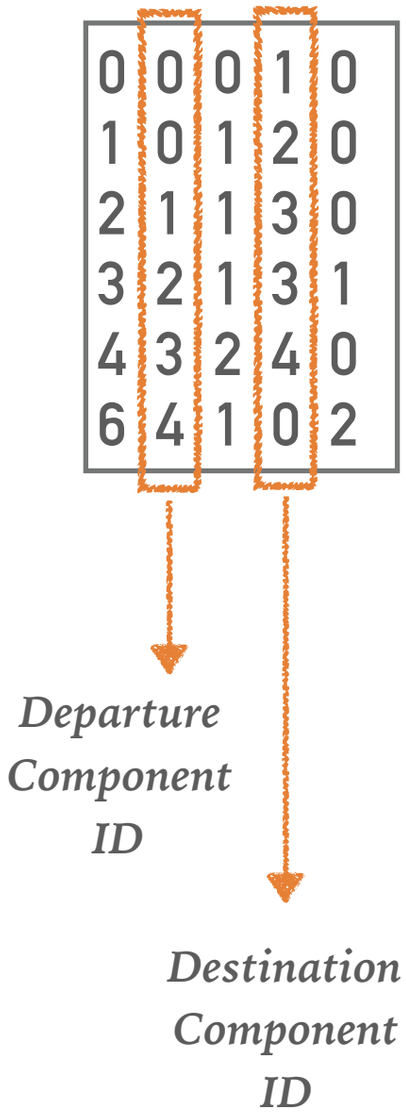
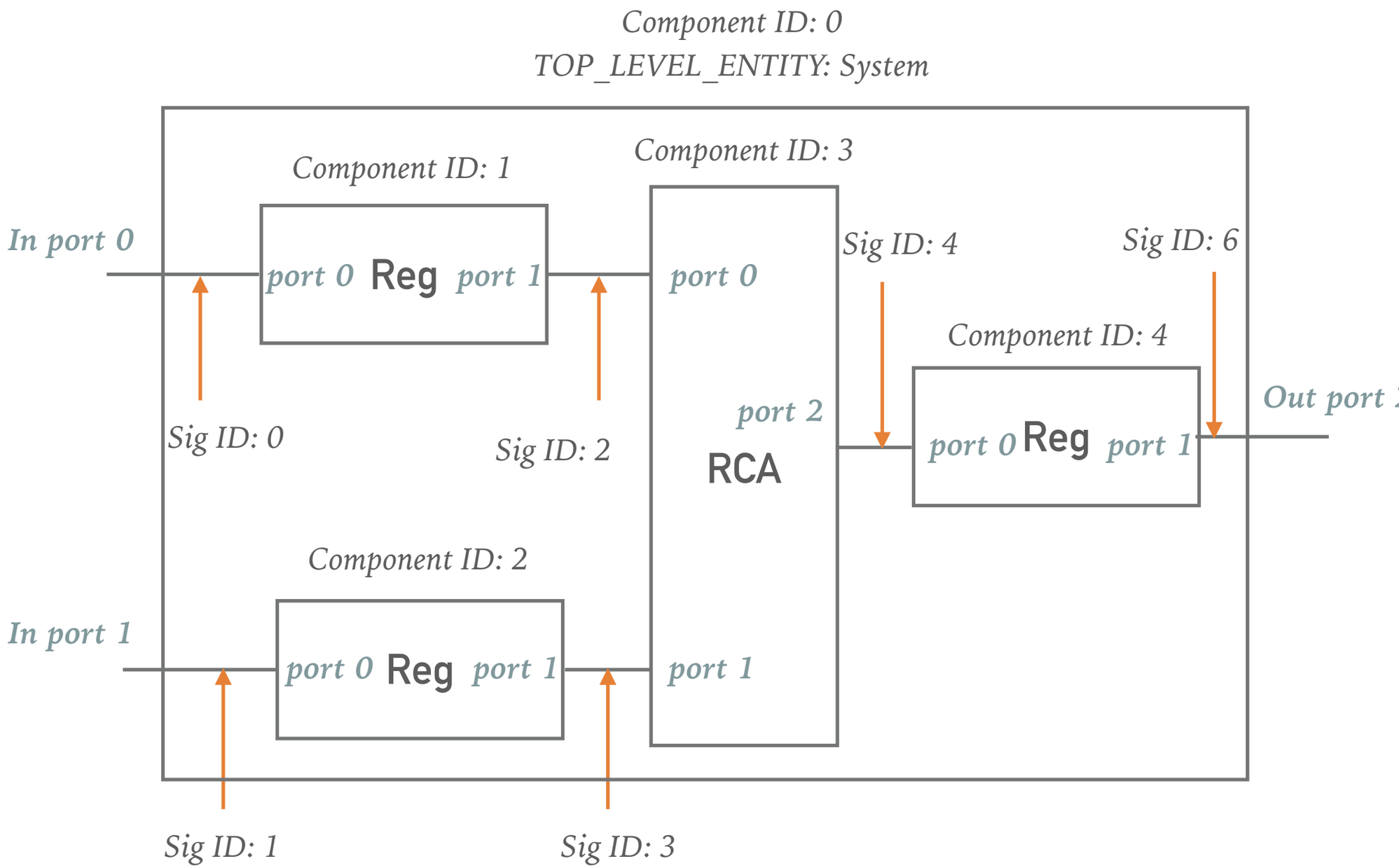
SIGNAL INFORMATION FILE

- Example





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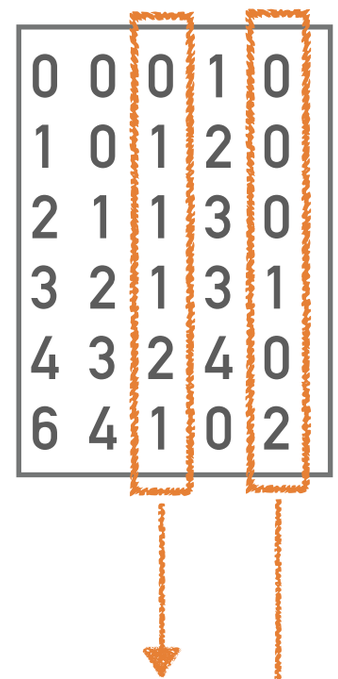

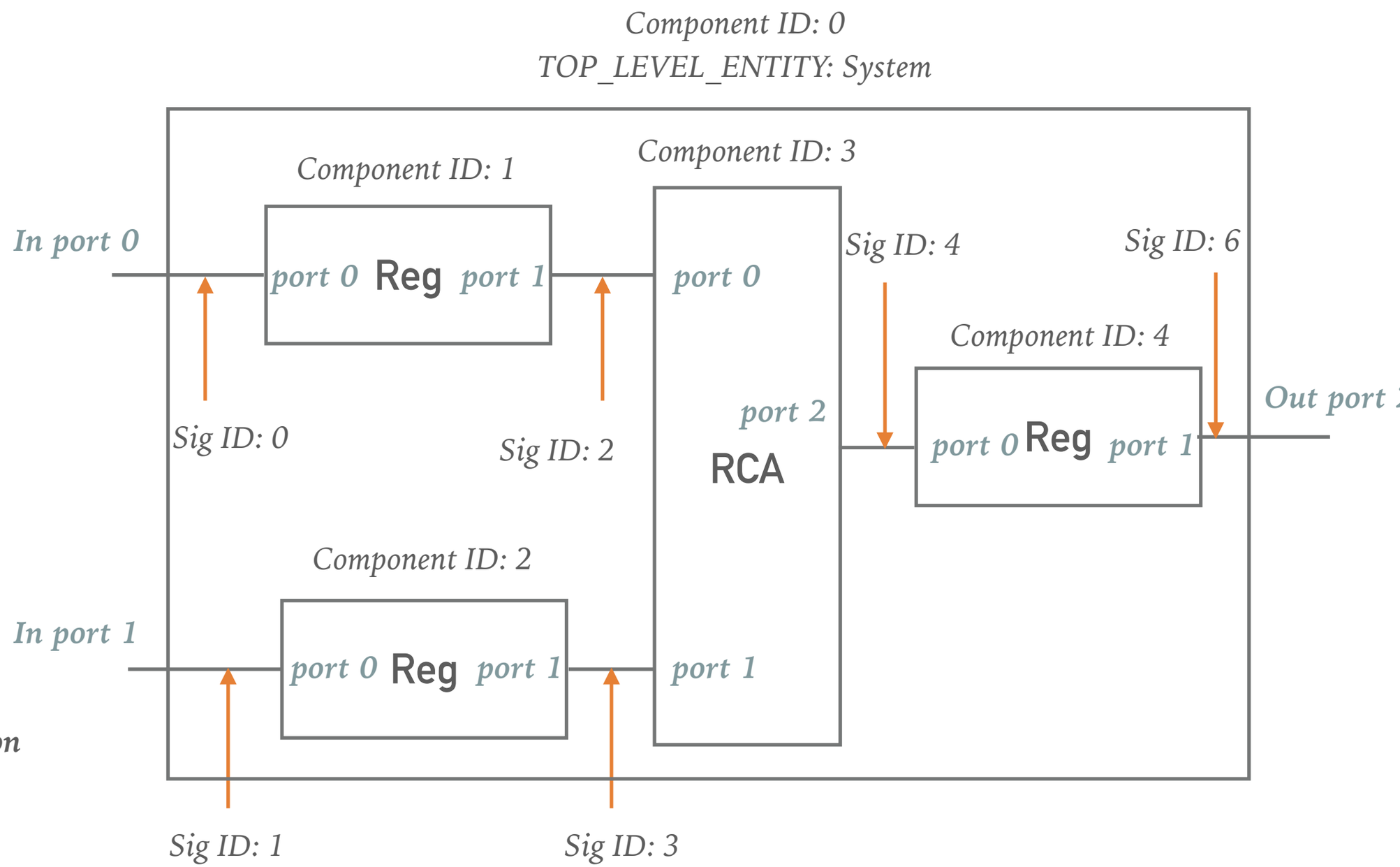

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