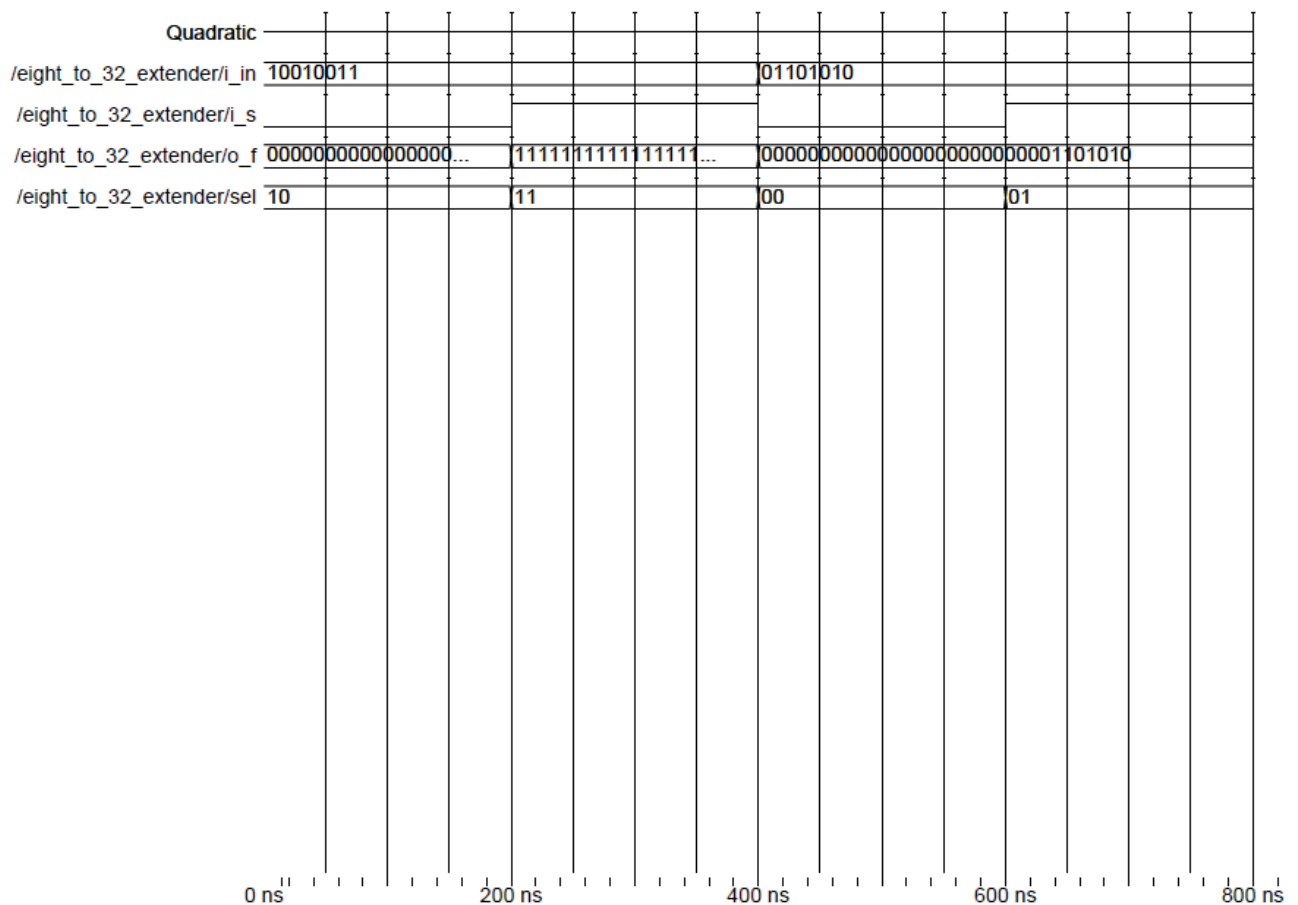


Prelab:

According to Figure 1, the value of **q** will get set on the rising clock to whatever is in memory at the address given by the address signal. As far as writing to memory goes, the write to memory happens on the falling edge of the clock. This can be seen visually by having the values in memory only change at a falling edge of the clock. Writing only happens when **wren** is high. Once **wren** turns high, the next rising edge the output **q** changes value, and the following falling edge is when the write happens to the memory location as specified by **address**.

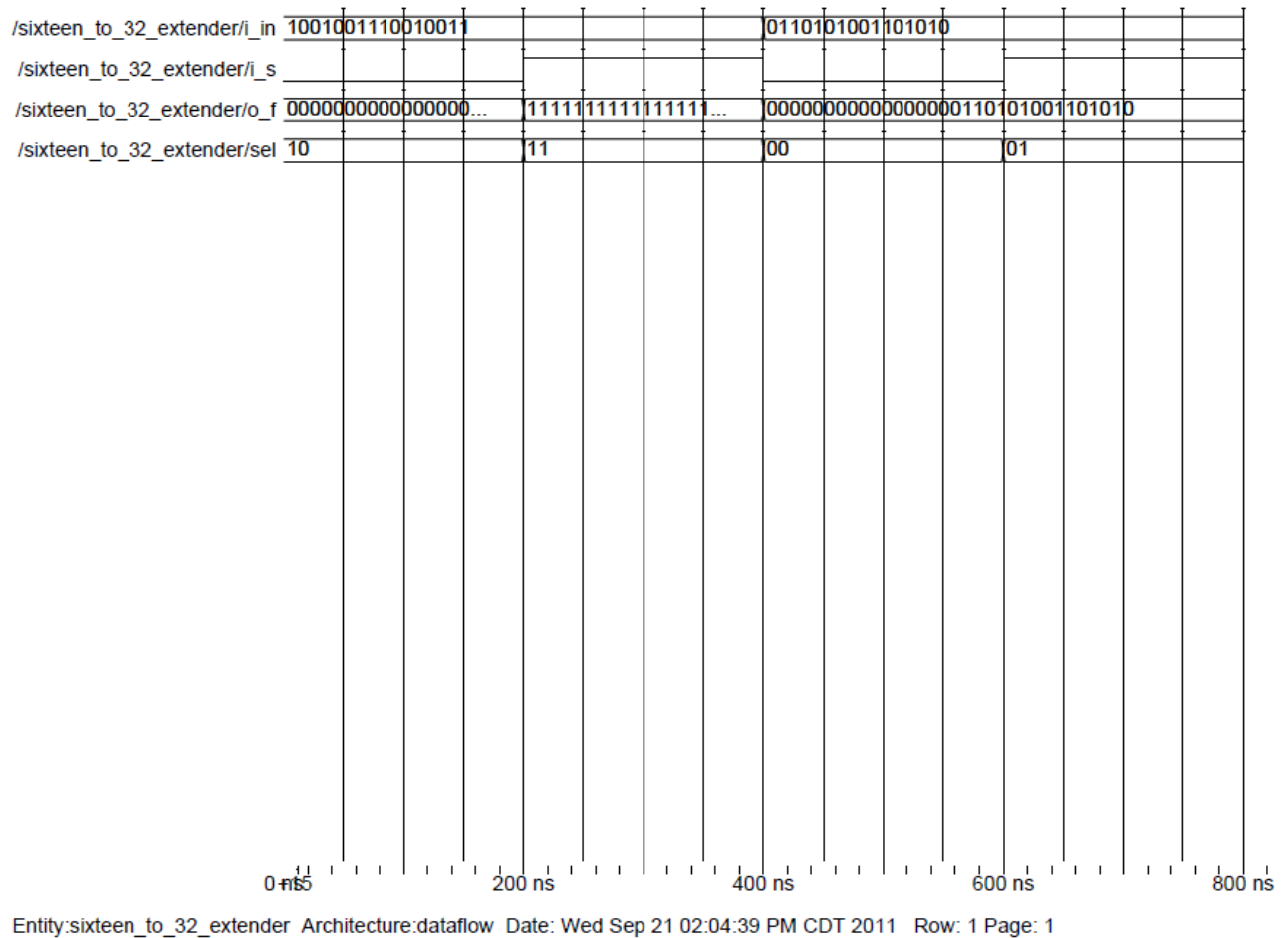
Part 1:

- a) Some instructions requiring sign extension include addi, bne. An instruction that requires zero extension would be jump.
- b) There are 4 different extenders – a signed extender and unsigned (zero) extender for both 8-bit and 16-bit inputs.
- c) No question for report



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d)



Part 2:

- No question for report
- mif_filename** - the generic name of the file containing the memory specification

address - the address to read from or write to

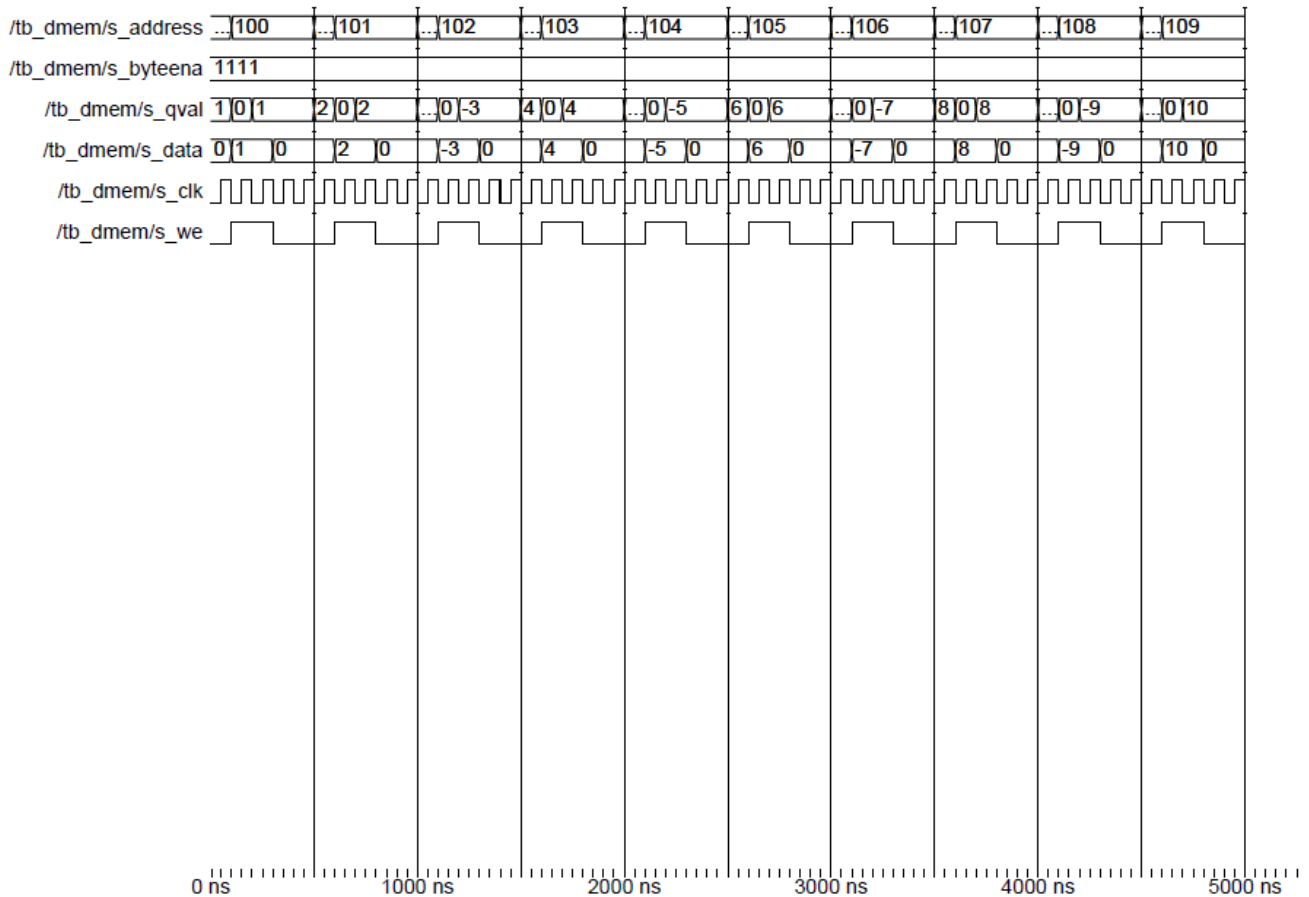
byteena - indicates which bytes will be overwritten in a write to the memory at location **address**

clock - the clock for the system. Keeps elements synchronized.

data - the data to write to the memory at address **address** if **wren** is enabled.

wren - whether we are able to write to memory or not

q - the output of a read from the memory module
- It is somewhat difficult to get the full range of time in a readable format, but here is what I could get.

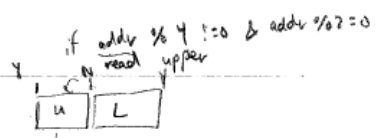


Entity:tb_dmem Architecture:behavior Date: Wed Sep 21 03:27:13 PM CDT 2011 Row: 1 Page: 1

- d) A difference between our waveforms and the given waveforms in the prelab is that ours has the waves changing exactly on a clock edge, whereas the prelab has some minor differences between the clock and the wave responses.

Part 3:

- a) For this new processor design I needed to add a couple new control signals. I added one to enable writing to memory, which corresponds to the write enable port on the memory module. I also added a selection signal to select whether we wanted to write the result from the adder/subtractor or the result from memory to the register file. I added a signal to define whether the operation was a signed operation or not, which corresponds to the selection signal on the extenders for the output from memory. I also added a selection signal for the size of the data coming from memory, which chooses which extended value to choose to go back to the register file.
- b) Schematic:



- c) The waveform for this section is pretty hard to gather as we have a bunch of register values, and a lot of memory values, which would make the image practically useless.