5_Quiz _L2

- Due Nov 18 at 2:15pm
- Points 10
- Questions 10
- Available until Nov 18 at 2:15pm
- Time Limit 15 Minutes

Instructions

This is a timed, closed book, closed notes quiz.
There are 10 questions.
Total time is 15 mins.
You can navigate front and back.
For code related questions, write the whole code in the area provided.
There should not be any other tab or window open on your laptop while you are attempting the quiz.
Offenders will get a 0.
You cannot use chatgpt or any other AI tool to obtain answers. Offenders will get a 0.
Good luck!!!

This quiz was locked Nov 18 at 2:15pm.

Attempt History

	Attempt	Time	Score
LATEST	Attempt 1	12 minutes	10 out of 10

ⓘ Correct answers are hidden.

Score for this quiz: 10 out of 10
Submitted Nov 18 at 2:12pm
This attempt took 12 minutes.

Question 1
1 / 1 pts

Assuming you have a 12 bit virtual address in which the first 4 most significant bits (MSB) are used for storing the VPN. How many offset values can be accommodated?

- 64
- 256
- 32
- Cannot be determined
- 128

Question 2
1 / 1 pts

Assume the following stream of accessed virtual pages. What is the Hit rate if FIFO policy is used.

0,1,2,0,1,3,0,3,1,2,1

- 36%
- 31%
- 42%

- 51%

Question 3
1 / 1 pts

Assume the following stream of accessed virtual pages. What is the Hit rate if Optimal policy is used.

0,1,2,0,1,3,0,3,1,2,1

- 60%
- 70%
- 55%
- 45%

Question 4
1 / 1 pts

Which of the following is a disadvantage of paging?

- Inefficient utilization of sparse address spaces
- Leads to external fragmentation
- Additional memory accesses slow down the system
- Requires complex segmentation tables

Question 5
1 / 1 pts

When a TLB miss occurs on a RISC processor, how is it typically handled?

- By replacing the page with the least-recently-used policy
- By hardware fetching the PFN and updating the TLB
- By software (OS) raising an exception and resolving the miss
- By flushing all TLB entries

Question 6
1 / 1 pts

How does the Address Space Identifier (ASID) help during context switches in a system with TLBs?

- By dynamically resizing the TLB for the current process
- By marking invalid entries in the page table
- By avoiding the need to flush the TLB entirely
- By increasing the page size for frequently used processes

Question 7
1 / 1 pts

What additional hardware is required for the hybrid approach to page tables?

- TLB entries for each virtual page
- Multi-level address mapping circuits
- Page table caches and inverted tables
- Base and bounds registers for each segment

Question 8
1 / 1 pts

In multi-level page tables, how is space saved compared to linear page tables?

- (selected) By dynamically allocating only valid page table fragments
- By using larger page sizes for translation
- By replacing the page directory with a hashed index
- By storing page tables in compressed format

Question 9
1 / 1 pts

How does an inverted page table differ from a linear or multi-level page table?

- (selected) It uses physical frame numbers (PFNs) as indices instead of virtual page numbers (VPNs).
- It requires page directories to store indices
- It is limited to 32-bit address spaces only
- It eliminates the need for a TLB

Question 10
1 / 1 pts

What is the major concern with linear page tables for systems with a 64-bit virtual address space?

- They lead to high levels of fragmentation.
- They cannot support multi-level address translation
- (selected) They require excessive memory when multiple processes are running
- They cannot handle large page sizes effectively

Quiz Score: 10 out of 10