



Habib University

EE-371/CS-330/CE-321 Computer Architecture – Spring 2023

Instructors: Dr. Tariq Kamal, Dr. Farhan Khan, Dr. Munzir Zafar, Dr. Sorath

Time = 40 minutes

Quiz 04

Max Points: 20

Instructions:

- i. **Smart watches, laptops, and similar electronics are strictly NOT allowed.**
- ii. **Answer sheets should contain all steps, working, explanations, and assumptions.**
- iii. Attempt the quiz on clean papers with black/blue ink.
- iv. Print your name and HU ID on all sheets.
- v. Turn in your question paper along with your answer sheets.
- vi. You are not allowed to ask/share your method or answer with your peers. The work submitted by you is solely your own work. Any violation of this will be the violation of HU Honor code and proper action will be taken as per university policy if found to be involved in such an activity.

CLO Assessment:

This assignment assesses students for the following course learning outcomes.

Course Learning Outcomes		CLO Assessed
CLO 1	Explain the role of ISA in modern processors and instruction encodings and assembly language programming	
CLO 2	Explain the architecture and working of a single cycle processor	
CLO 3	Design the architecture to mitigate issues of a pipelined processor	
CLO 4	Analyze the performance of cache operations	✓

Question 1 [8 points]:

A four-way set-associative cache with 256 sets has been proposed for your newly designed Fast-MATH embedded processor that uses RISC-V architecture. Each block holds one word.

The memory address space is 32 bits (4GB), and the cache is byte-addressable.

(Note: Each word contains 4 bytes)

- a) [4 points] How many bits from the main memory address will be allocated for tag, index(set), and block offset?

Tag	Index (Set)	Block Offset
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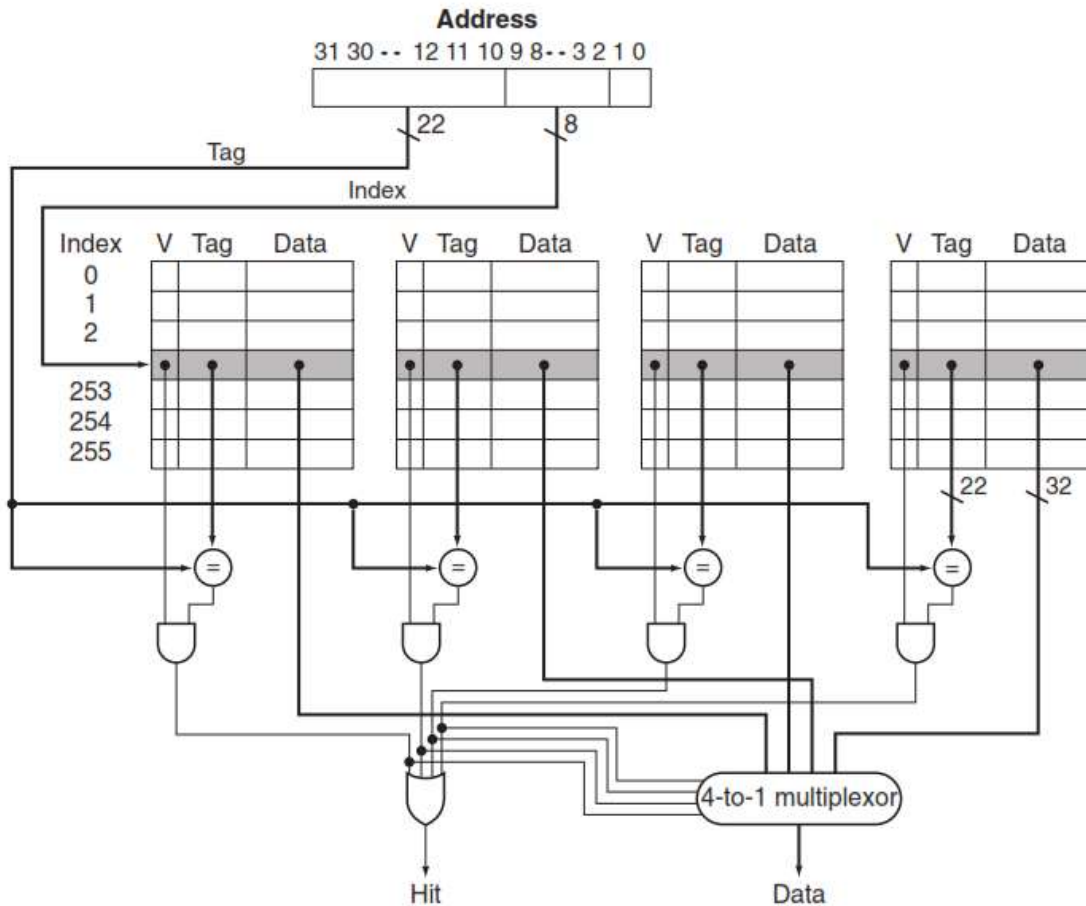
(Note: Block offset also includes byte offset in its least significant bits)

Answer:

- Each block holds 1 word = $1 \times 4 = 4$ bytes = 2^2 bytes, therefore, 2 bits are allocated for Block Offset.
- 256 sets in Cache = 2^8 sets in cache, therefore, 8 bits are allocated for index(set).
- Total bits in memory address are 32, therefore, remaining $32 - 8 - 2 = 22$ bits are allocated for tag.

- b) [4 points] Draw a diagram for the cache organization specifying the relevant multiplexor(s) and other logic.

Answer:



Question 2 [4 points]:

Assume the miss rate of an instruction cache is 2% and the miss rate of the data cache is 4%. If a processor has a CPI of 2 without any memory stalls, and the miss penalty is 110 cycles for all misses, determine how much faster a processor would run with a perfect cache that never missed.

Assume the frequency of all loads and stores is 40%.

Answer:

The number of memory miss cycles for instructions in terms of the Instruction count (I) is:

- Instruction miss cycles = $I \times 2\% \times 110 = 2.20 \times I$

As the frequency of all loads and stores is 25%, we can find the number of memory miss cycles for data references:

- Data miss cycles = $I \times 40\% \times 4\% \times 110 = 1.76 \times I$

- The total number of memory-stall cycles is $2.20 I + 1.76 I = 3.96 I$. This is three cycles of memory stall per instruction.
- Accordingly, the total CPI including memory stalls is $2.00 + 3.96 = 5.96$.

Since there is no change in instruction count or clock rate, the ratio of the CPU execution times is:

$$\frac{\text{CPU Time with stalls}}{\text{CPU time with perfect cache}} = \frac{I \times CPI_{\text{stall}} \times \text{Clock Cycle Time}}{I \times CPI_{\text{perfect}} \times \text{Clock Cycle Time}} = \frac{CPI_{\text{stall}}}{CPI_{\text{perfect}}} = \frac{5.96}{2} = 2.98$$

The performance with the perfect cache is better by 2.98.

Question 3 [8 points]:

Assume a fully-associative cache with four one-word blocks.

Consider the following word address sequence:

0, 2, 3, 7, 11, 13, 14, 7, 1.

Assuming an LRU replacement policy, which accesses are hits?

(Hint: Draw a table and specify each memory access as a Hit or a Miss.)

Answer:

Word Address	Hit/Miss	Block 0	Block 1	Block 2	Block 3
0	Miss	M[0]			
2	Miss	M[0]	M[2]		
3	Miss	M[0]	M[2]	M[3]	
7	Miss	M[0]	M[2]	M[3]	M[7]
11	Miss	M[11]	M[2]	M[3]	M[7]
13	Miss	M[11]	M[13]	M[3]	M[7]
14	Miss	M[11]	M[13]	M[14]	M[7]
7	Hit	M[11]	M[13]	M[14]	M[7]
1	Miss	M[1]	M[13]	M[14]	M[7]

There is 1 hit.