Student Name: **HU ID #:**

Habib University

EE-371/CS-330/CE-321 Computer Architecture – Spring 2024
Instructors: Dr. Tariq Kamal, Dr. Farhan Khan, Dr. Waseem Hassan

Time = 50 minutes **Quiz 03** **Max Points: 20**

Instructions:

i. ***Smart watches, laptops, and similar electronics are strictly NOT allowed.***
ii. ***Answer sheets should contain all steps, working, explanations, and assumptions.***
iii. Attempt the quiz on clean papers with black/blue ink.
iv. Print your name and HU ID on all sheets.
v. Turn in your question paper along with your answer sheets.
vi. You are not allowed to ask/share your method or answer with your peers. The work submitted by you is solely your own work. Any violation of this will be the violation of HU Honor code and proper action will be taken as per university policy if found to be involved in such an activity.

CLO Assessment:

This assignment assesses students for the following course learning outcomes.

Course Learning Outcomes		CLO Assessed
CLO 1	***Explain*** the role of ISA in modern processors and instruction encodings and assembly language programming	
CLO 2	***Explain*** the architecture and working of a single cycle processor	
CLO 3	***Design*** the architecture to mitigate issues of a pipelined processor	✓
CLO 4	***Analyze the*** performance of cache operations	

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Q1: Assume that the following sequence of instructions is executed on a five-stage pipelined RISC-V processor:

```
sub x1, x4, x5
add x2, x6, x7
or x3, x1, x2
```

a) [4 marks] If there is no forwarding uint insert NOP(s) to ensure correct execution. Re-write the code sequence with NOP(s) inserted[Hint: Draw timing diagram first]

Sol:

Instruction	CC0	CC1	CC2	CC3	CC4	CC5	CC6	CC7
sub	IF	ID	EXE	MEM	WB			
add		IF	ID	EXE	MEM	**WB**		
NOP			IF	ID	EXE	MEM	WB	
NOP				IF	ID	EXE	MEM	WB
or					IF	**ID**	EXE	MEM

```
sub x1, x4, x5
add x2, x6, x7
nop
nop
or x3, x1, x2
```

b) [6 marks] Assume the pipelined processor has hazard detection and forwarding units. Draw a timing diagram for the first seven cycles during the execution of this code and specify values of forwarding control signals in each cycle. Use **x** or don't care where forwarding is not needed.

Sol:

Instruction	CC0	CC1	CC2	CC3	CC4	CC5	CC6	CC7
sub	IF	ID	EXE	MEM	WB			
add		IF	ID	EXE	MEM	WB		
or			IF	ID	EXE	MEM	WB	IF
ForwardA	x	x	00	00	01	x	x	x
ForwardB	x	x	00	00	10	x	x	x

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Q2: Assume that the following sequence of instructions is executed on a five-stage pipelined RISC-V processor:

```
ld x2, 4(x1)
and x4, x2, x3
sll x5, x2,  x4
```

a) [5 marks] If there is no forwarding uint insert NOP(s) to ensure correct execution. Re-write the code sequence with NOP(s) inserted[Hint: Draw timing diagram first]

Sol:

Instruction	CC0	CC1	CC2	CC3	CC4	CC5	CC6	CC7
ld	IF	ID	EXE	MEM	WB			
NOP		IF	ID	EXE	MEM	WB		
NOP			IF	ID	EXE	MEM	WB	
and				IF	ID	EXE	MEM	WB
NOP					IF	ID	EXE	MEM
NOP						IF	ID	EXE
sll							IF	ID

```
ld x2, 4(x1)
nop
nop
and x4, x2, x3
nop
nop
sll x5, x2,  x4
```

b) [5 marks] Assume the pipelined processor has hazard detection and forwarding units. Draw again the multi-cycle timing diagram and show, if any NOP(s), will be inserted.

Sol:

Instruction	CC0	CC1	CC2	CC3	CC4	CC5	CC6	CC7
ld	IF	ID	EXE	MEM	WB			
NOP		NOP	NOP	NOP	NOP	NOP		
and			IF	ID	EXE	MEM	WB	
sll				IF	ID	EXE	MEM	WB