Lab Quiz – Worksheet

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Task 1.

Code: Design module & testbench

Provide appropriately commented code for designed module & its testbench, code should contain meaningful variable naming.

**Add snippet or Copy paste the code written in the Editor window. Make sure the irrelevant area of the snip is cropped.*

Design Module

```
module ALU8Bit(
    input [7:0] Din_A,
    input [7:0] Din_B,
    input [2:0] Opcode,
    output reg [7:0] DOut,
    output Zero_Flag
    );
    always @(*)
    begin
    case (Opcode)
    3'b011:
    DOut=(Din_A & Din_B); //AND OPERATION

    3'b100:
    DOut=(Din_A | Din_B); //OR OPERATION

    3'b000:
    DOut=(Din_A + Din_B); //ADD OPERATION

    3'b001:
    DOut=(Din_A - Din_B); //SUB OPERATION

    3'b010:
    DOut=~(Din_A | Din_B); //NOR OPERATION
```

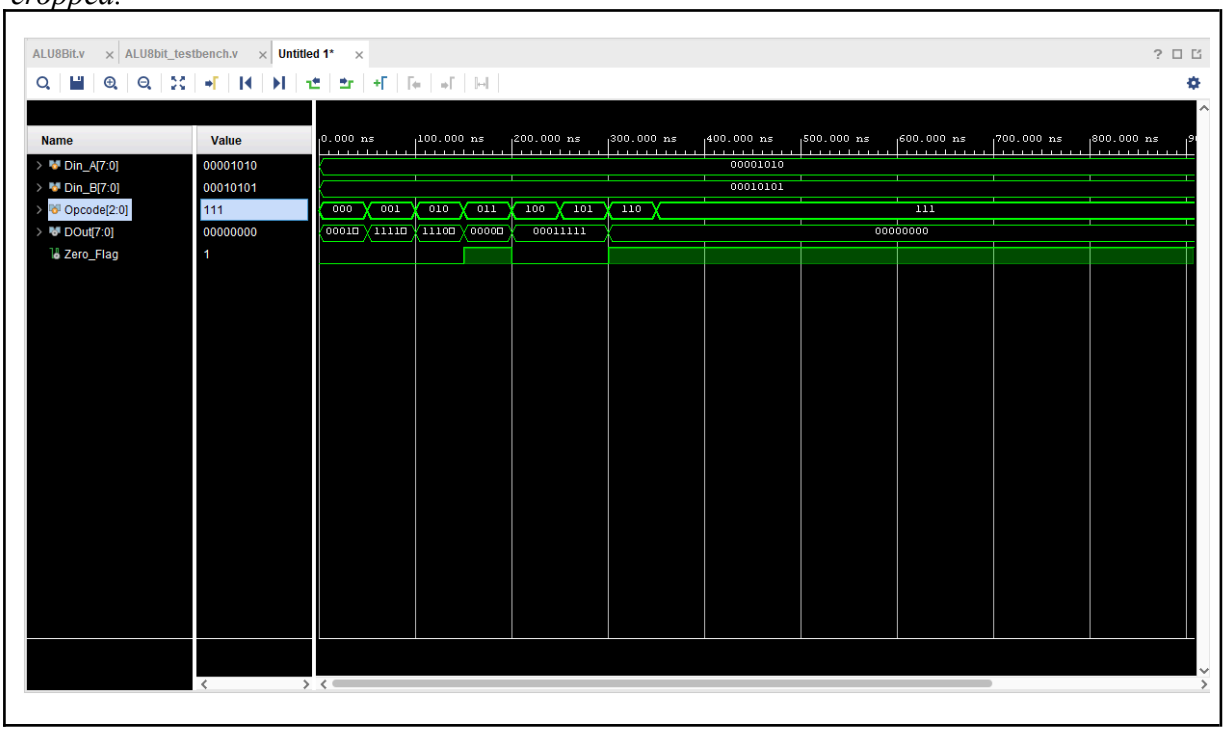
```
    3'b101:
    DOut= Din_A ^ Din_B ; //XOR OPERATION

    3'b110:
    DOut= Din_A << Din_B ; //SHIFT LEFT OPERATION

    3'b111:
    DOut= Din_A >> Din_B ; //SHIFT RIGHT OPERATION

    default:
    DOut=8'b00000000;

    endcase
    end
    assign Zero_Flag = DOut? 0:1;
endmodule
```

Test Bench

```
module ALU8bit_testbench(
    );
    reg [7:0] Din_A;
    reg [7:0] Din_B;
    reg [2:0] Opcode;
    wire [7:0] DOut;
    wire Zero_Flag;
    ALU8Bit alu(Din_A,Din_B,Opcode,DOut,Zero_Flag);
    initial
    begin
    Din_A=8'b00001010; //10
    Din_B=8'b00010101; //21

    Opcode=3'b000;

    #50
    Opcode=3'b001;

    #50
    Opcode=3'b010;

    #50
    Opcode=3'b011;

    #50
    Opcode=3'b100;

    #50
    Opcode=3'b101;

    #50
    Opcode=3'b110;

    #50
    Opcode=3'b111;

    end
endmodule
```

Results (Waveforms)

**Add snip of relevant signals' waveforms. Make sure the irrelevant area of the snip is cropped.*



Comments

**Observation/Comments on the obtained results/working of code.*

It performs various arithmetic and logic operations based on the input signals. The module has three inputs A and B for 8 bits and Opcode for 3 bits. The result is for 8 bits.

When Opcode is 000 we will perform add operation, basically whatever is the Opcode value we will perform the assigned ALU Operation for it.

Operations supported by this ALU include:

● ADD (ALUOp = 3'b000): Bitwise ADDof a and b which in my code will give output when a and b are added here it is Din_A + Din_B = 10 + 21 = 31 00011111

● OR (ALUOp = 3'b`100): Bitwise OR of a and b

● SUB (ALUOp = 3'b001): this will subtract the given values a-b is to give 11110101

● NOR (ALUOp = 3'b010): this will first OR them then invert it to give 11100000

● AND (ALUOp = 3'b011): this will AND the two values to give 00000000

● XOR (ALUOp = 3'b101): this will perform Bitwise XOR operation and give 00011111

● SHIFT LEFT (ALUOp = 3'b110): this will shift value of A to left by the value of B bits to give result 00000000

● SHIFT RIGHT (ALUOp = 3'b111): this will shift value of A to right by the value of B bits to give result 00000000

● Default: If none of the specified Opcode codes are matched, Result is set to 0.

Din_A	Din_B	Opcode	DOut	Zero_Flag
8’d10	8’d21	000	00011111	0
		001	11110101	0
		010	11100000	0
		011	00000000	1
		100	00011111	0
		101	00011111	0
		110	00000000	1
		111	00000000	1

Table: Testcases

Task 2.1

Value of a & b:

```
// a=2;
// b=3;
always
begin
a=b;
b=a;
end
```

a=_____ b=_____

```
// a=2;
// b=3;
always
begin
a<=b;
b<=a;
end
```

a=_____ b=_____

A)

a=3
b=3

B)

a=TRUE
b=FALSE

Task 2.2

MCQ: Write the correct answer

D

Lab Quiz

Assessment Rubrics

Marks Distribution:

Task No.	LR 2 Code	LR 5 Results	LR 10 Analysis
Task 1 - Design Module	/20	-	-
Task 1 - Testbench	/10	/15	/5
Task 2.1	-	-	/5
Task 2.2	-	-	/5
Total Points	/60 Points		
CLO Mapped	CLO 1		

For description of different levels of the mapped rubrics, please refer to the provided Lab Evaluation Assessment Rubrics.

#	Assessment Elements	Level 1: Unsatisfactory Points 0-1	Level 2: Developing Points 2	Level 3: Good Points 3	Level 4: Exemplary Points 4
LR2	**Program/Code/ Simulation Model/ Network Model**	Program/code/simulation model/network model does not implement the required functionality and has several errors. The student is not able to utilize even the basic tools of the software.	Program/code/simulation model/network model has some errors and does not produce completely accurate results. Student has limited command on the basic tools of the software.	Program/code/simulation model/network model gives correct output but not efficiently implemented or implemented by computationally complex routine.	Program/code/simulation /network model is efficiently implemented and gives correct output. Student has full command on the basic tools of the software.
LR5	**Results & Plots**	Figures/ graphs / tables are not developed or are poorly constructed with erroneous results. Titles, captions, units are not mentioned. Data is presented in an obscure manner.	Figures, graphs and tables are drawn but contain errors. Titles, captions, units are not accurate. Data presentation is not too clear.	All figures, graphs, tables are correctly drawn but contain minor errors or some of the details are missing.	Figures / graphs / tables are correctly drawn and appropriate titles/captions and proper units are mentioned. Data presentation is systematic.
LR10	**Analysis**	Results are not interpreted or are analyzed incorrectly.	Analysis of the obtained results is incomplete. Conclusions are not drawn.	Results are analyzed and concluded but are not well explained and justification is not provided with the help of reasoning.	Results are well analyzed and supported with reasons. A good comparison is made between the theoretical and experimental results with the correct and useful conclusion.