Habib University

EE-371/CS-330/CE-321 Computer Architecture – Spring 2023
Instructors: Dr. Tariq Kamal, Dr. Farhan Khan, Dr. Waseem Hassan

Time = 50 minutes **Quiz 04 SOL** **Max Points: 20**

Instructions:

i. ***Smart watches, laptops, and similar electronics are strictly NOT allowed.***
ii. ***Answer sheets should contain all steps, working, explanations, and assumptions.***
iii. Attempt the quiz on clean papers with black/blue ink.
iv. Print your name and HU ID on all sheets.
v. Turn in your question paper along with your answer sheets.
vi. You are not allowed to ask/share your method or answer with your peers. The work submitted by you is solely your own work. Any violation of this will be the violation of HU Honor code and proper action will be taken as per university policy if found to be involved in such an activity.

CLO Assessment:

This assignment assesses students for the following course learning outcomes.

Course Learning Outcomes		CLO Assessed
CLO 1	***Explain*** the role of ISA in modern processors and instruction encodings and assembly language programming	
CLO 2	***Explain*** the architecture and working of a single cycle processor	
CLO 3	***Design*** the architecture to mitigate issues of a pipelined processor	
CLO 4	***Analyze the*** performance of cache operations	✓

Question 1 [8 points]:

a) **[4 points]** Assume a fully- associative cache with eight one-word blocks.

Consider the following word address sequence:

0, 2, 3, 7, 11, 13, 14, 7, 1, 2, 3, 0

Assuming an LRU replacement policy, which accesses are hits?

b) **[4 points]** Assume a direct-mapped cache with eight one-word blocks.

Consider the following word address sequence:

0, 2, 3, 7, 11, 13, 14, 7, 1, 2, 3, 0

Assuming an LRU replacement policy, which accesses are hits?

(Hint: Draw a table and specify each memory access as a Hit or a Miss.)

Answer:

a)

Block Address	Hit/Miss	Cache content after access							
		Block 0	Block 1	Block 2	Block 3	Block 4	Block 5	Block 6	Block 7
0	Miss	M[0]							
2	Miss	M[0]	M[2]						
3	Miss	M[0]	M[2]	M[3]					
7	Miss	M[0]	M[2]	M[3]	M[7]				
11	Miss	M[0]	M[2]	M[3]	M[7]	M[11]			
13	Miss	M[0]	M[2]	M[3]	M[7]	M[11]	M[13]		
14	Miss	M[0]	M[2]	M[3]	M[7]	M[11]	M[13]	M[14]	
7	Hit	M[0]	M[2]	M[3]	M[7]	M[11]	M[13]	M[14]	
1	Miss	M[0]	M[2]	M[3]	M[7]	M[11]	M[13]	M[14]	M[1]
2	Hit	M[0]	M[2]	M[3]	M[7]	M[11]	M[13]	M[14]	M[1]
3	Hit	M[0]	M[2]	M[3]	M[7]	M[11]	M[13]	M[14]	M[1]
0	Hit	M[0]	M[2]	M[3]	M[7]	M[11]	M[13]	M[14]	M[1]

There are 4 hits.

b)

Block Address	Cache Index	Hit/ Miss	Cache content after access							
			Block 0	Block 1	Block 2	Block 3	Block 4	Block 5	Block 6	Block 7
0	0 mod 8 = 0	Miss	M[0]							
2	2 mod 8 = 2	Miss	M[0]		M[2]					
3	3 mod 8 = 3	Miss	M[0]		M[2]	M[3]				
7	7 mod 8 = 7	Miss	M[0]		M[2]	M[3]				M[7]
11	11 mod 8 = 3	Miss	M[0]		M[2]	M[11]				M[7]
13	13 mod 8 = 5	Miss	M[0]		M[2]	M[11]		M[13]		M[7]
14	14 mod 8 = 6	Miss	M[0]		M[2]	M[11]		M[13]	M[14]	M[7]
7	7 mod 8 = 7	Hit	M[0]		M[2]	M[11]		M[13]	M[14]	M[7]
1	1 mod 8 = 1	Miss	M[0]	M[1]	M[2]	M[11]		M[13]	M[14]	M[7]
2	2 mod 8 = 2	Hit	M[0]	M[1]	M[2]	M[11]		M[13]	M[14]	M[7]
3	3 mod 8 = 3	Miss	M[0]	M[1]	M[2]	M[3]		M[13]	M[14]	M[7]
0	0 mod 8 = 0	Hit	M[0]	M[1]	M[2]	M[3]		M[13]	M[14]	M[7]

There are 3 hits.

Question 2 [8 points]:

A four-way set-associative cache with 256 sets has been proposed for your newly designed Ubiquiti-MATH embedded processor that uses RISC-V architecture. Each block holds one word. The memory address space is 32 bits (4GB), and the cache is byte-addressable.

(Note: Each word contains 4 bytes)

a) **[4 points]** How many bits from the main memory address will be allocated for tag, index(set), and block offset?

Tag	Index (Set)	Block Offset

(Note: Block offset also includes byte offset in its least significant bits)

b) **[4 points]** Draw a diagram for the cache organization specifying the relevant multiplexer(s) and other logic.

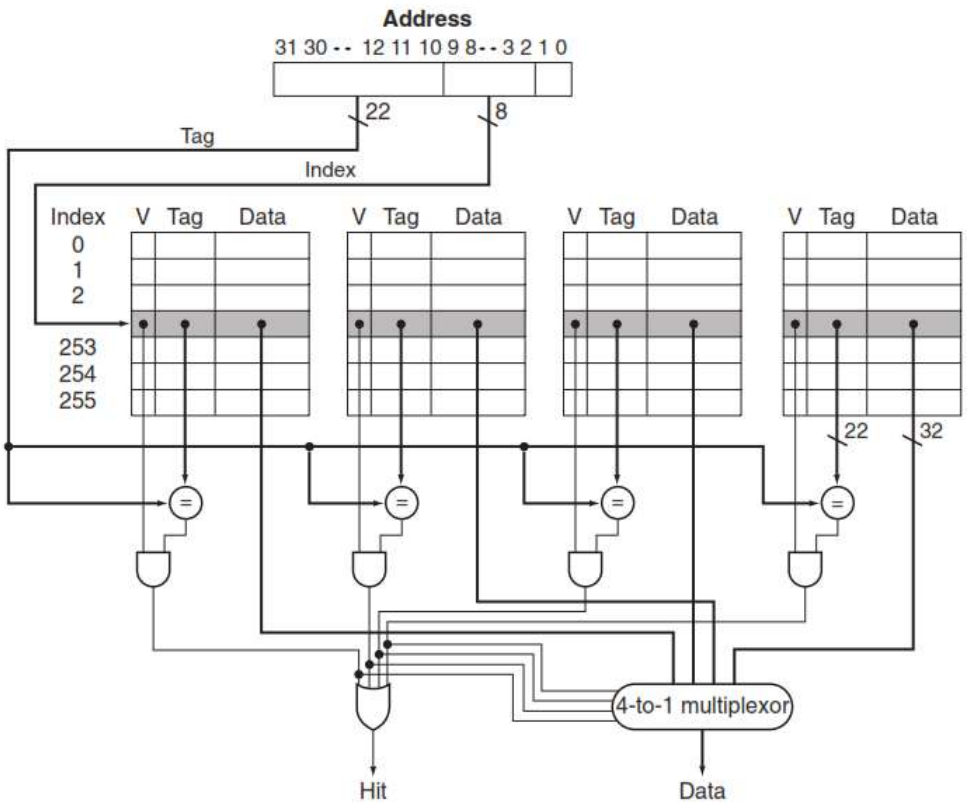
Answer:

a)

- Each block holds 1 word = 1 x 4 = 4 bytes = 2^2 bytes, therefore, 2 bits are allocated for Block Offset.
- 256 sets in Cache = 2^8 sets in cache, therefore, 8 bits are allocated for index(set).
- Total bits in memory address are 32, therefore, remaining 32 – 8 – 2 = 22 bits are allocated for tag.

Tag = 22	Index (Set) = 8	Block Offset = 2

b)



Question 3 [4 points]:

a) **[2 points]** Assume the miss rate of an instruction cache is 2% and the miss rate of the data cache is 4%. If a processor has a CPI of 2 without any memory stalls, and the miss penalty is 110 cycles for all misses, determine how much faster a processor would run with a perfect cache that never missed.
Assume the frequency of all loads and stores is 40%.

b) **[2 points]** Suppose that after heavily improving the pipeline of the processor in part (a), we have achieved a CPI of 1. Find out how much faster the same processor would run with a perfect cache that never missed?

Answer:

a)
The number of memory miss cycles for instructions in terms of the Instruction count (I) is:

- Instruction miss cycles = I × 2% × 110 = 2.20 × I

As the frequency of all loads and stores is 40%, we can find the number of memory miss cycles for data references:

- Data miss cycles = I × 40% × 4% × 110 = 1.76 × I
- The total number of memory-stall cycles is 2.20 I + 1.76 I = 3.96 I. This is four cycles of memory stall per instruction.
- Accordingly, the total CPI including memory stalls is 2.00 + 3.96 = 5.96.

Since there is no change in instruction count or clock rate, the ratio of the CPU execution times is:

$$\frac{CPU\ Time\ with\ stalls}{CPU\ time\ with\ perfect\ cache} = \frac{I\ \times CPIstall \times Clock\ Cycle\ Time}{I\ \times CPIperfect \times Clcok\ Cycle\ Time} = \frac{CPIstall}{CPIperfect}$$
$$= \frac{5.96}{2} = 2.98$$

The performance with the perfect cache is better by 2.98.

b)

The number of memory miss cycles for instructions in terms of the Instruction count (I) is:

- Instruction miss cycles = I × 2% × 110 = 2.20 × I

As the frequency of all loads and stores is 40%, we can find the number of memory miss cycles for data references:

- Data miss cycles = I × 40% × 4% × 110 = 1.76 × I
- The total number of memory-stall cycles is 2.20 I + 1.76 I = 3.96 I. This is four cycles of memory stall per instruction.
- Accordingly, the total CPI including memory stalls is $CPI_{stall} = CPI_{perfect} + CPI_{miss} = 1.00 + 3.96 = 4.96$.

Since there is no change in instruction count or clock rate, the ratio of the CPU execution times is:

$$\frac{CPU\ Time\ with\ stalls}{CPU\ time\ with\ perfect\ cache} = \frac{I\ \times CPIstall \times Clock\ Cycle\ Time}{I\ \times CPIperfect \times Clcok\ Cycle\ Time} = \frac{CPIstall}{CPIperfect}$$
$$= \frac{4.96}{1} = 4.96$$

The performance with the perfect cache is better by 4.96.