Fong

Read Cycle SRAM - CY7C1049G

Timing Reference	Explanation (CLK is T = 5 ns)	Value	Requirement	Margin
tRC	This is the minimum length of time th	10 ns	10 ns	0 ns
tAA	This is the maximum amount of time t	10 ns	10 ns	0 ns
tOHA	This is the minimum amount of time t	0 ns	3 ns	3 ns

Read to SRAM	Timing in ns
De-rating	3
CLK time to address	5
tSU	3.79
tAA	10
Total	**21.79**

Write Cycle SRAM - CY7C1049G

Timing Reference	Explanation (CLK is T = 5 ns)	Value	Requirement	Margin
tWC	This is the total width of the wavefo	10 ns	10 ns	0 ns
tSD	This is the setup time the data need	5 ns	5 ns	5 ns
tHD	This is the hold time the data needs	0 ns	0 ns	0 ns
tSCE	CE is low to 0, so it is always activ	5 ns	7 ns	2 ns
tAW	This is the setup time the address ne	5 ns	7 ns	2 ns
tHA	This is the hold time the address ne	0 ns	0 ns	0 ns
tLZWE	This is the length of time after WE	0 ns	3 ns	3 ns
tHZWE	This is the length of time after WE	0 ns	5 ns	0 ns
tLZOE	This is the length of time after OE g	5 ns	3 ns	2 ns

Write to SRAM	Timing in ns
De-rating	0
CLK time to address	5
tSU	3.79
tAW	7
Total	**15.79**

Read Cycle FLASH NOR - S29AL008J

Timing Reference	Explanation (CLK is T = 5 ns)	Value	Requirement	Margin
tRC	This is the minimum length of time th	70 ns	70 ns	0 ns
tACC	This is the setup time the address	70 ns	70 ns	0 ns
tCE	This is the maximum length for chip e	70 ns	70 ns	0 ns
tOE	This is the maximum length for outpu	30 ns	30 ns	0 ns
tDF	This is the maximum length for chip e	15 ns	16 ns	1 ns
tSR/W	This is the maximum length of latency	15 ns	20 ns	5 ns
tOEH	This is the minimum length of output	0 ns	0 ns	0 ns
tOH	This is the minimum length of output	0 ns	0 ns	0 ns

Read to NOR Flash	Timing in ns
De-rating	3
CLK time to address	5
tSU	3.79
tAA	70
Total	**81.79**

Write Cycle FLASH NOR - S29AL008J

Timing Reference	Explanation	Value	Requirement	Margin
tWC	This is the total width of the wavefo	70 ns	70 ns	0 ns
tAS	This is the minimum setup time the	0 ns	0 ns	0 ns
tAH	This is the minimum hold time the	45 ns	45 ns	0 ns
tCH	This is the minimum hold time in C	0 ns	0 ns	0 ns
tWP	This is the minimum Write Pulse W	22.5 ns	35 ns	12.5 ns
tWHWH1	This is the programming operation	5 ns	6 ns	1 ns
tCS	This is the setup time for Chip Enal	0 ns	0 ns	0 ns
tWPH	This is the minimum Write Pulse W	22.5 ns	25 ns	2.5 ns
tDS	This is the minimum data setup tim	N/A	35 ns	N/A
tDH	This is the minimum data hold time	N/A	0 ns	N/A
tBUSY	This is the maximum program/erase	N/A	90 ns	N/A
tRB	This is the minimum recovery time	0 ns	0 ns	0 ns
tVCS	This is the minimum VCC setup tir	N/A	50 ns	N/A

Write to NOR Flash	Timing in ns
De-rating	0
CLK time to address	5
tSU	3.79
tAH (tAW)	45
Total	**53.79**

Vivado Timing Report

Timing Reference	Setup Time	Hold Time	Pulse Width
Timing (ns)	3.79	0.201	4.5