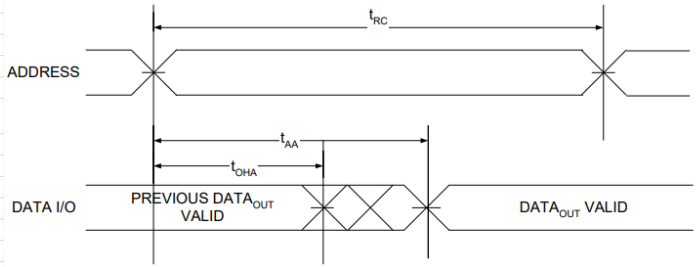
Fong

SRAM - CY7C1049G

Figure 6. Read Cycle No. 1 of CY7C1049G (Address Transition Controlled) [20, 21]



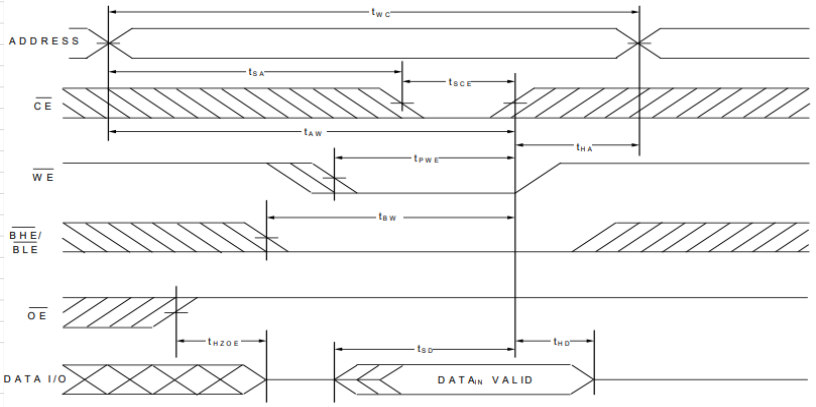
tRC = Read Cycle Time

tAA = 10ns = Address to data/EER valid

tOHA = Data / ERR hold from address change

20. The device is continuously selected, OE = VIL, CE = VIL.
21. WE is HIGH for the read cycle.

Figure 9. Write Cycle No. 1 ($\overline{CE}$ Controlled) [24, 25]



tWC = Write cycle time

tSCE = CE LOW to write end

tAW = Address setup to write end

tHA = Address hold from write end

tSA = Address setup to write start

tPWE = WE pulse width

tHZOE = OE HIGH to HI-Z

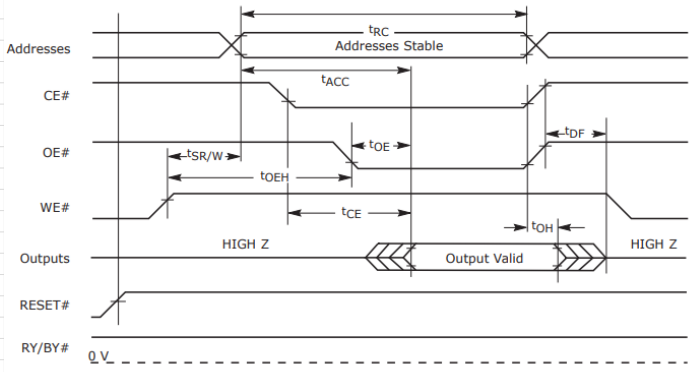
tSD = Data setup to write end

tHD = Data hold from write end

24. The internal write time of the memory is defined by the overlap of WE = VIL, CE = VIL. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
25. Data I/O is in HI-Z state if CE = VIH, or OE = VIH

FLASH NOR - S29AL008J

Figure 14. Read Operations Timings



tRC = Read Cycle Time

tACC = Address to Output Delay

tCE = Chip Enable to Output Delay

tOE = Output Enable to Output Delay

tDF = Chip or Output Enable to Output High Z

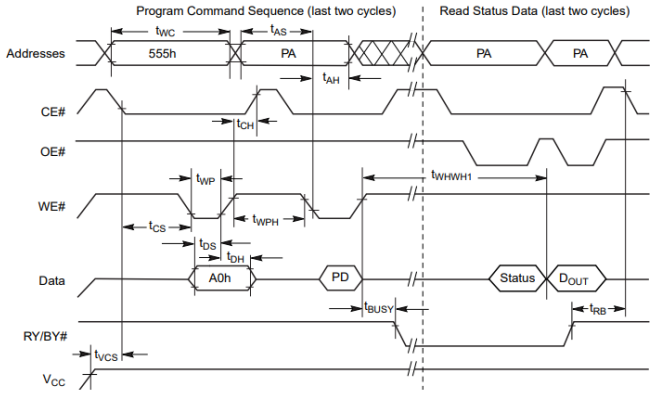
tSR/W = Latency Between Read and Write Operations

tOEH = Output Enable Hold Time

tOH = Output Hold Time From Addresses, CE# or OE#

FLASH NOR - S29AL008J

Figure 18. Program Operation Timings



tWC = Write Cycle Time

tAS = Address Setup Time

tAH = Address Hold Time

tCH = CE# Hold Time

tWP = Write Pulse Width

tWHWH1 = Programming Operation

tCS = CE# Setup Time

tWPH = Write Pulse Width High

tDS = Data Setup Time

tDH = Data Hold Time

tBUSY = Program/Erase Valid to Ry/By# Delay

tRB = Reovery Time from Ry/By#

tVCS = VCC Setup Time