Generating the Technology library related sdb files:

* Download all the files from the following link
  + “ <https://wustl.box.com/VCSsdb> ”
* Create a folder named VTVT\_TSMC180
* Run following commands in order.
* ***vhdlan -work vtvt\_tsmc180 vtvt\_tsmc180\_Vtables.vhd***
* ***vhdlan -work vtvt\_tsmc180 vtvt\_tsmc180\_Vcomponents.vhd***
* ***vhdlan -work vtvt\_tsmc180 vtvt\_tsmc180\_VITAL.vhd***
* You should find two .sdb in the VTVT\_TSMC180 directory created.
* Note: Remove the VTVT\_TSMC180 folder if you want to regenerate the .sdb files.

Process to simulate using VCS:

* Run following command to analyze all your design and test bench files written in Verilog
  + vlogan <filename.v>
* you should find a AN.DB folder created.
* Copy the already generated .sdb files in VTVT\_TSMC180 directory into the AN.DB folder.
* Run your vcs simulation by providing the **top module of your testbench**.
  + vcs –debug <topmodule> -o simv
  + eg: vcs –debug cortexm0ds\_tb –o simv