International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 2 Issue 4, April - 2013

Design And Simulation Of First Order Sigma Delta ADC In 0.13um CMOS Technology

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Abstract

This paper presents the design of a first order Sigma-Delta ADC which is realized using CMOS technology. In this paper, a first Order Sigma-Delta ADC is implemented in a standard 0.13um CMOS technology. The Design and Simulation of the Modulator is done using Mentor Graphics Tool. First order single bit Sigma Delta ADC Modulator is implemented using ±1.3 power supply. The SD ADC provides the advantage of low power, require no anti aliasing filters and immune to noise outside the ADC bandwidth. Further, design of 1-bit Sigma Delta ADC is to be proposed which consists of Op-amp as a key component in Sigma delta ADC. Op-amp at integrator stage is with Gain 46 dB, output resistance is 10KΩ, power dissipation is 0.928 mW, offset voltage is 0.065 V, and prorogation delay is 16.61 ns.

1. Introduction

Oversampled sigma-delta analog-to-digital converters(sigma-delta ADCs) are well known for their capability to achieve high-resolution in low-to-medium speed applications. However, extending these converters to broadband applications requires lowering the oversampling ratio (OSR) in order to implement the sigma-delta modulator within the technology limits and reasonable values of consumable power. Recently, ΔΣ modulation becomes suited for high resolution ADC. In addition, oversampling is employed to shape the quantization noise from a coarse quantizer outside the signal band. High-order modulator structures and multi-bit quantizers are often used to decrease the OSR requirements without lowering their performance.

A sigma-delta ADC comprises of an analog block of modulator and a digital block of decimator. One integrator and qauantizer in the forward path and a DAC in the feedback path of a single feedback loop system. The use of modulator is done in order to sample input signal at oversampling rate which generates output stream of 1 bit. For actual DSP decimator or down sampler is used as a digital filter. In sigma-delta ADC, a decimator is a important part of it.

In this work we are going to design of Op-amp, Comparator and DAC for Sigma-Delta Analog–to-Digital Converter (ADC) using Mentor Graphics tool. The paper is being divided into five sections. In section 2, Basic of ADCs and types of ADCs. In section 3, designing of the Op-amp, Comparator and DAC. In section 4, Simulation results are presented. Finally in section 5, Conclusion.

2. BASIC OF ADCs

2.1 Ideal Analog and Digital Converter

The Analog to digital converter (ADC or A/D converter) has the opposite function as that of Digital to Analog converter and converts an analog input signal to a digital output signal, as shown in Figure.1

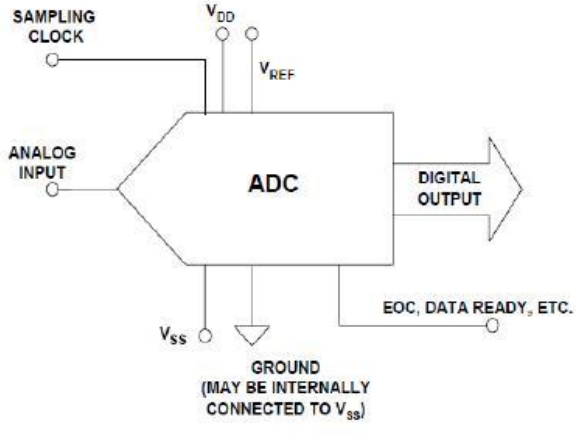
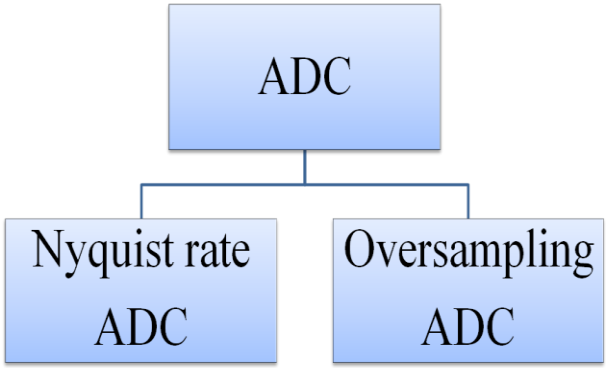


Figure.1 Ideal Block Diagram of Digital to Analog Converter [3]

where Bout is the digital output world while Analog Input and Vref are the analog input and reference signal

respectively. Also, we define VLSB to be the signal change corresponding to a signal LSB change in the D/A case.

2.2 Types of ADC's



A. Nyquist-Rate ADCs

- Flash ADCs
- Sub-Ranging ADCs
- Folding ADCs
- Pipelined ADCs
- Successive Approximation (Algorithmic) ADCs
- Integrating (Serial) ADCs

B. Oversampling ADCs

- Delta-Sigma based ADCs

2.3 Delta Sigma A/D Converter

This class of A/D converter stands out to be the most advanced, among all the Data converters discussed so far.

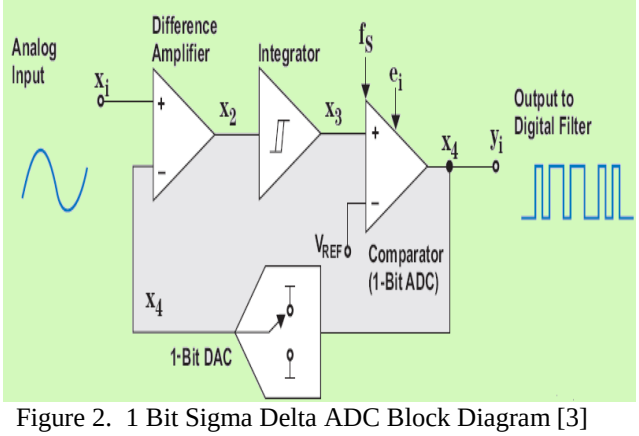


Figure 2. 1 Bit Sigma Delta ADC Block Diagram [3]

Figure shows the block diagram of first order Delta-sigma Converter (Σ-Δ ADC). It consists of Integrator, a comparator (1 bit ADC), 1-bit DAC. In above block diagram the output of an integrator is feed to a 1-bit ADC (which is known as a Comparator), and output of ADC is given to the DAC.

The type of A/D converters discussed so far are Nyquist converters where by sampling rate is twice the input signal frequency for error free signal approximation. Only way to decrease the Quantization noise or better signal representation is sampling the signal many more times. This is the fundamental theory in sigma delta data converters.

3. Design of Sigma Delta ADC

3.1 Op-Amp Design

Op-Amps are one of the basic and important circuits which have a wide application in several analog circuit. The 1st stage is a differential amplifier. It has two inputs which are the inverting and non-inverting voltage. It provides at the output a differential voltage or a differential current that, essentially, depends on the differential input only. The gain provided by the input stages is not sufficient and additional amplification is required. The intermediate stage is provide necessary gain, which is another differential amplifier, driven by the output of the first stage.

The bias circuit is provided to establish the proper operating point for each transistor in its saturation region. Finally, we have the output buffer stage. It provides the low output impedance and larger output current needed to drive the load of op-amp or improves the slew rate of the op –amp. The key thing to note to about the amplifier is the frequency compensation network which is used to push the high frequency zero out of the pass band of the op-amp[3].

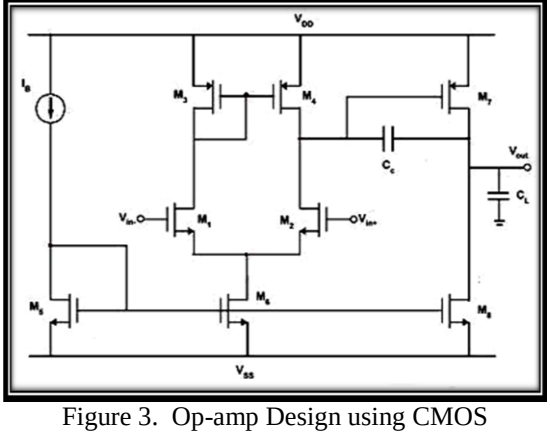


Figure 3. Op-amp Design using CMOS

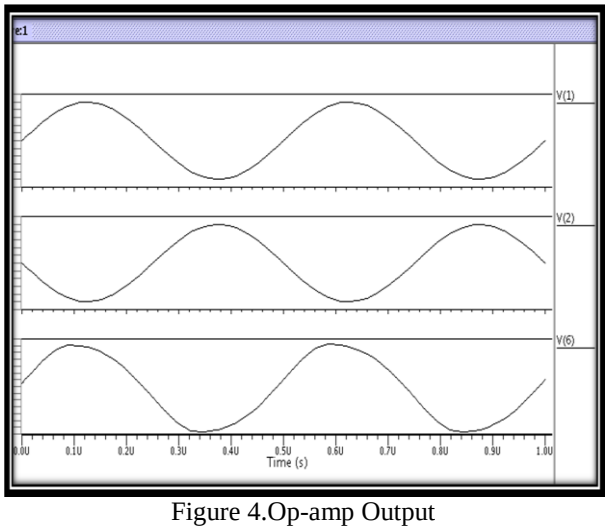


Figure 4.Op-amp Output

3.2 Design of Comparator

The comparator is generally used in the process of converting analog signal to digital signals. A comparator is a device which compares two voltages or currents and switches its output to indicate which is larger. A comparator is a circuit that has binary output. Ideally its output is defined as follows:

$$V_o = \begin{cases} V_{OH} \text{ if } V_{in+} - V_{in-} > 0 \\ V_{OL} \text{ if } V_{in+} - V_{in-} < 0 \end{cases}$$

In an analog-to-digital conversion process, it is necessary to first sample the input. The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. The comparator does not need the compensation network because its only function is to switch from rail to rail. Stability is not needed as it will only slow down the switching speed. When a sine wave is input to the circuit, the comparator switches from positive rail to negative rail [3].

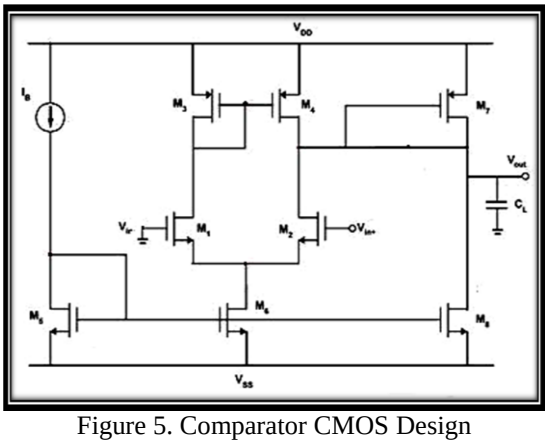


Figure 5. Comparator CMOS Design

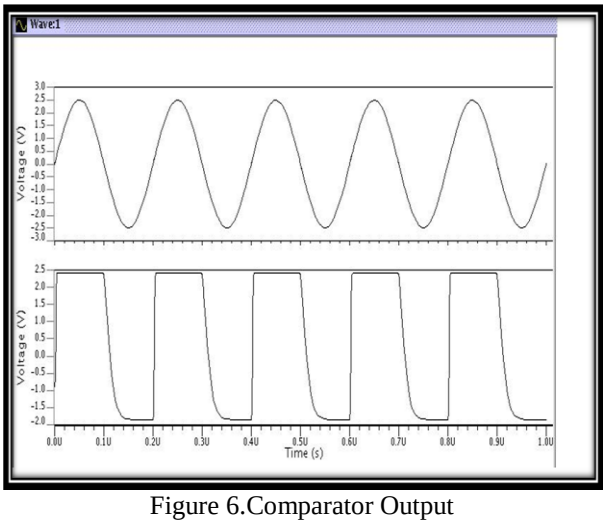


Figure 6.Comparator Output

3.3 Design of DAC

The most important component of feedback path is the 1 bit DAC that converts the output digital bit stream to analog value based on a reference voltage. The DAC is a simple multiplexer based design in which if the input(output of modulator) is logic 1 a voltage of +Vref is fed back and if the input is logic 0 a voltage of–Vref is fed back to the summer of first stage.

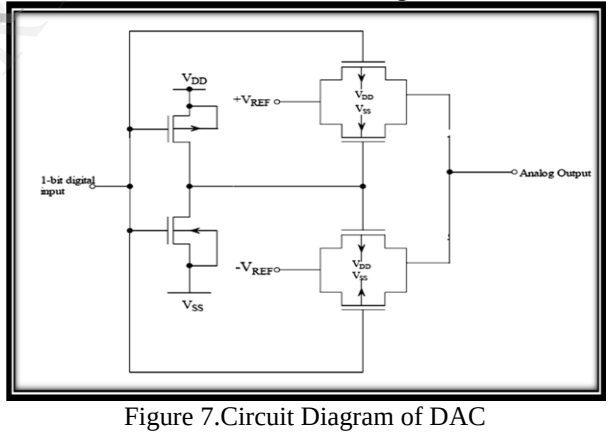


Figure 7.Circuit Diagram of DAC

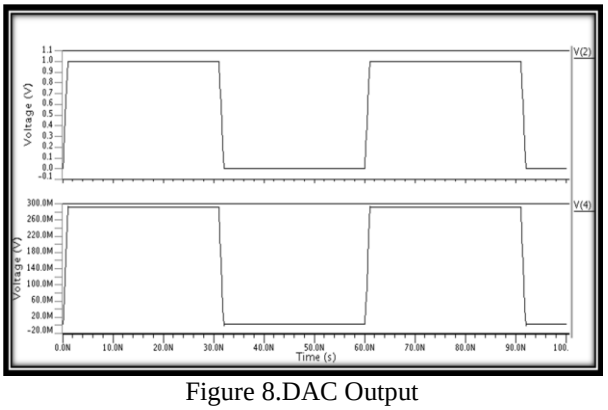


Figure 8.DAC Output

4. Simulation Results

The circuit design of Op-amp, Comparator and DAC for 1st order Sigma -Delta have been implemented by using 0.13um CMOS Technology.

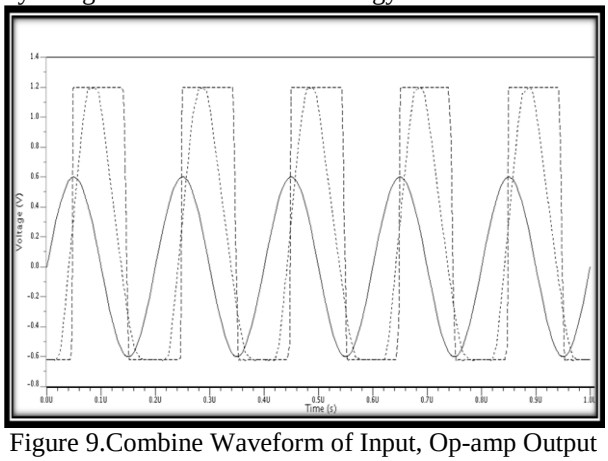


Figure 9.Combine Waveform of Input, Op-amp Output and Comparator Output

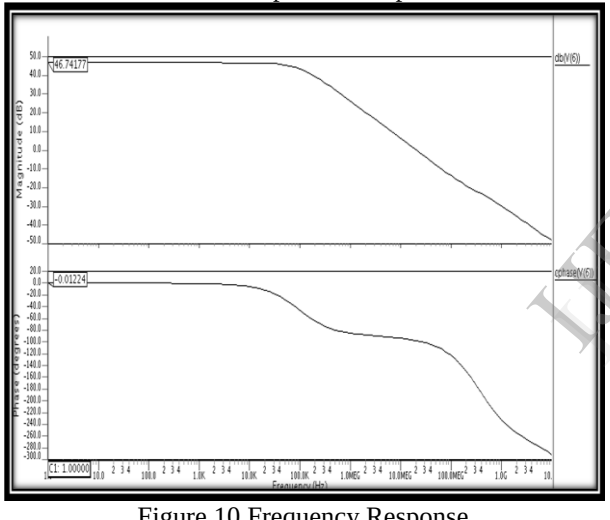


Figure 10.Frequency Response

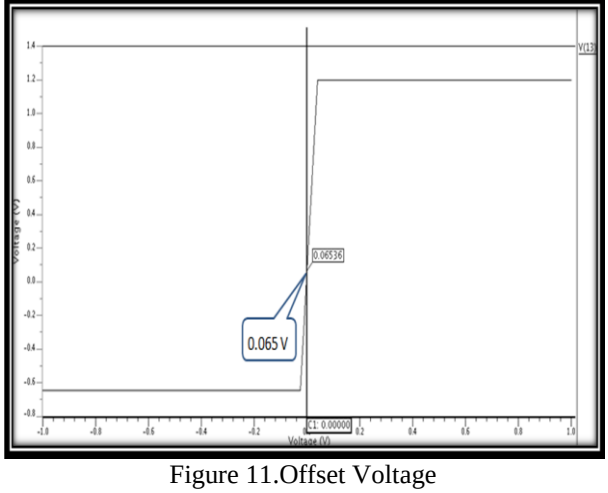


Figure 11.Offset Voltage

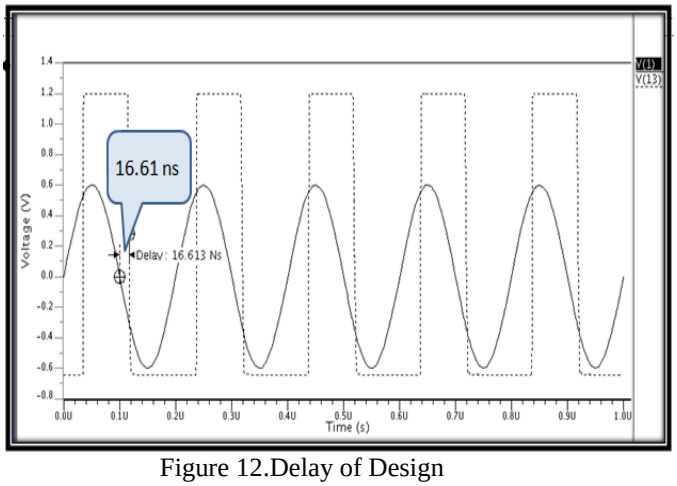


Figure 12.Delay of Design

Table 1 Resulted System Parameters

Parameter	Value
Power Supply	±1.3 V
Technology	0.13 um
Power Dissipation	0.928 mW
Delay	16.61 ns
Offset	0.065 V
Gain	46.74 dB

5. Conclusion

In present work, An 1-bit sigma-delta analog-to digital converter system has been designed and simulated in standard TSMC 0.13 um CMOS Technology. The circuits are simulated in SPICE with MOSIS Level-53 MOS model parameters. For simulation I used Power supply voltage is VDD=1.3v and resistance is 10KΩ and after simulation Gain of Op-Amp is 46 dB and Power dissipation s 0.928 mW.

6. References

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