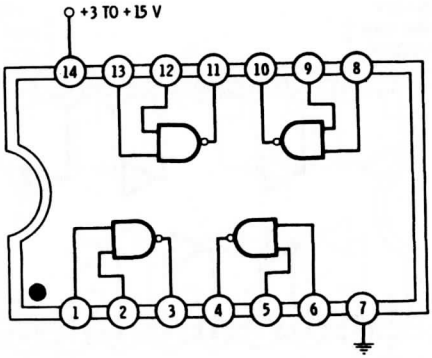
4011

QUAD 2-INPUT NAND GATE



TOP VIEW

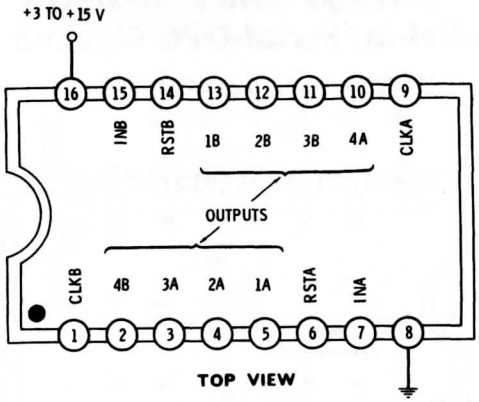
All four positive-logic NAND gates may be used independently.

On any one gate, with *either* or both inputs *low*, the output will be *high*; with both inputs *high*, the output will be *low*.

Propagation delay is 25 nanoseconds at 10 volts and 60 nanoseconds at 5 volts. Total package current at 1 megahertz is 0.4 milliampere at 5 volts and 0.8 milliampere at 10 volts.

Device is functionally equivalent to 7400 (TTL) and 74C00 (CMOS).

DUAL 4-STAGE SHIFT REGISTER (Serial-in/Parallel-Out)



This package contains two completely separate 4-stage shift registers that may be used in serial-in/serial-out or serial-in/parallel-out modes. Each register has its own clock and reset pins. Registers may be cascaded for longer lengths.

On either register, data entered on the IN pin appears at the 1 output on the positive edge (ground-to-positive transition) of the clock. A second clocking transfers the data to the 2 output, a third to the 3 output, and a fourth to the 4 output. The reset input must be *grounded* during normal operation. Making the reset input *positive* forces all outputs to ground and keeps them there until the reset input returns to ground.

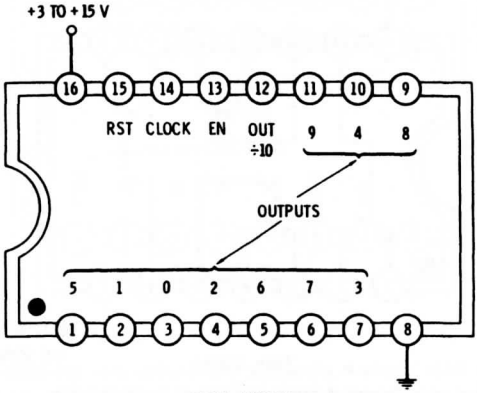
The clock must be noise free and have only one ground-to-positive transition per desired register clocking. The clock rise and fall times should be reasonably fast, preferably faster than 5 microseconds.

Maximum clock frequency is 5 megahertz at 10 volts and 2.5 megahertz at 5 volts. Total current per package at a 1-megahertz clocking rate is 2 milliamperes at 5 volts and 5 milliamperes at 10 volts.

Functionally equivalent to the 7491 and 74164 (TTL) and the 74HC4015 and 74C164 (CMOS) devices.

4017

DIVIDE-BY-10 COUNTER WITH 1-OF-10 OUTPUTS (Synchronous)



TOP VIEW

This is a fully synchronous decade, or divide-by-10, counter. It may be used to obtain a 1-of-10 decoded output or a square-wave output one-tenth the frequency of the input.

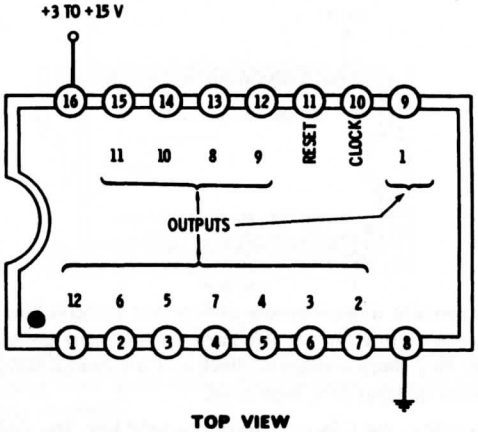
For normal operation, the clock enable and the reset should be at *ground*. The counter advances one count on the positive edge (ground-to-positive transition) of the clock. On any count, the decoded output goes *positive;* the others remain at ground. The OUT terminal is high for counts 0 through 4 and low for counts 5 through 9.

Making the reset input positive returns the counter to count zero. In this state, the "0" output and the OUT terminal are positive; the other outputs are at ground. The reset must be returned to ground to allow counting to continue. A positive voltage on the clock enable will inhibit (prevent count advance) clock operation.

The clock must be noiseless and have only one ground-to-positive transition per desired count. The clock rise time should be faster than 5 microseconds. An external gate will allow division by 1 through 10. Maximum clock frequency is 5 megahertz at 10 volts and 2.5 megahertz at 5 volts. Total package current at 1 megahertz is 0.4 milliampere at 5 volts and 0.8 milliampere at 10 volts, unloaded.

4040

12-STAGE (÷4096) BINARY RIPPLE COUNTER



TOP VIEW

This is a binary ripple counter that counts in the up direction using positive logic.

The reset input is normally held at ground. Every time the clock changes from positive to ground, the counter advances one count. The 1 output divides the input clock by $2^1 = 2$. The 2 output divides the input clock by $2^2 = 4$. The 3 output divides the input clock by $2^3 = 8$, up to the 12 output which divides by $2^{12} = 4096$.

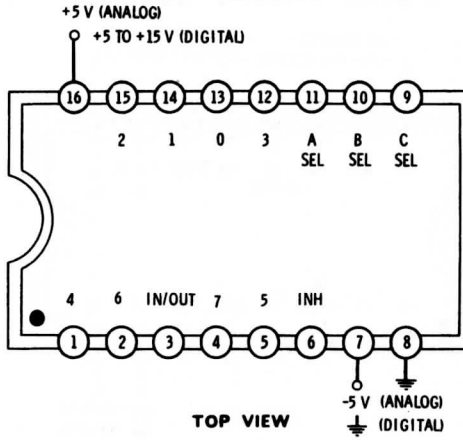
Making the reset input positive forces all outputs to ground and holds them there until the reset returns to ground.

The clock input must be conditioned to be noiseless and fall only once per desired count. Clock rise and fall times should be faster than 5 microseconds.

Since this is a ripple counter, the outputs change in sequential order and incorrect counts will briefly result during the settling time. Device is functionally and pin-for-pin equivalent to 74HC4040 for LS TTL levels.

Maximum input frequency is 6 megahertz at 10 volts and 2 megahertz at 5 volts. Total package current at a 1-megahertz clock rate is 0.4 milliampere at 5 volts and 0.8-milliampere at 10 volts. Consult the manufacturer's data sheet for propagation times.

1-OF-8 SWITCH



This package may be used as a 1-of-8 analog data multiplexer or demultiplexer, or as a 1-of-8 digital selector or distributor.

In the analog mode, −5 volts is applied to pin 7, and digital-control signals of low = ground and high = +5 are applied to the A, B, C, and INH inputs. If INH is high, no channel is selected. If INH is low, the channel selected is determined by the binary word input to A = 1, B = 2, and C = 4. Analog signals may be any value between +5 and −5 volts.

In the digital mode, pin 7 is grounded, and digital-control signals of low = ground and high = pin-16 voltage are applied to the A, B, C, and INH inputs. If INH is high, no channel is selected. If INH is low, the channel selected is determined by the binary word input to the A = 1, B = 2, and C = 4 inputs. Digital signals controlled may be any value between the pin-16 voltage and ground.

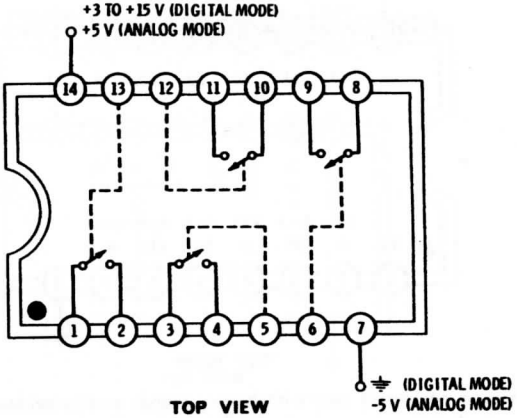
In either mode, the OFF state is an open circuit and the ON state is a 120-ohm resistor. Pin 3 may be used as an input or an output, depending on whether information is to be gathered from eight possible sources or distributed to eight possible locations. For digital signals only, device is functionally equivalent to the 74151 (TTL) and the 74C151 (CMOS) devices.

The minimum permissible load resistance is 100 ohms, and not more than 25 milliamperes can be routed through the circuit.

Total package current at a 1-megahertz clock rate is 0.5 milliampere at 5 volts and 1 milliampere at 10 volts, open circuited. Propagation delay is 200 nanoseconds for the supply connections shown. See Chapter 7 for more information.

4066

QUAD DIGITAL OR ANALOG BILATERAL SWITCH



TOP VIEW

All four switches may be used separately or in combination.

On any single switch, when the control voltage equals the pin-7 voltage, the switch remains OFF and behaves as a very high impedance. When the control voltage equals the pin-14 voltage, the switch turns ON and behaves as a nearly linear, bilateral, 90-ohm resistor.

Signals routed through the switch may be digital or analog, but they must never exceed the pin-14 voltage nor go below the pin-7 voltage.

Switches may be shorted together in any pattern, and there is no difference between the input and output terminals of any switch.

For instance, if all four switches are connected with one common terminal, the package may be used as a 1-of-4 data selector, a 1-of-4 data distributor, a 1-of-4 analog commutator, or a 1-of-4 analog multiplexer.

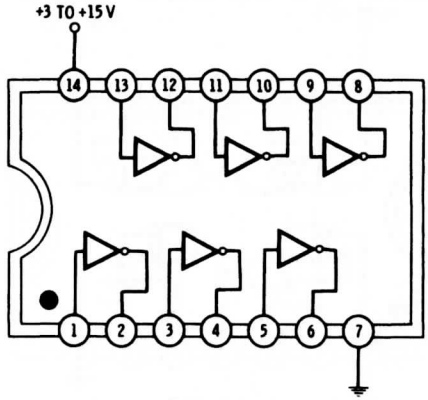
If more than one switch is connected to a common point, external logic usually must guarantee that only one switch is turned on at a time.

Maximum switching frequency is 10 megahertz at 10 volts and 5 megahertz at 5 volts. Package dissipation depends on the loading. Dissipation should be kept under 100 milliwatts total.

This is an improved version of the 4016, having a lower ON resistance. However, the 4016 remains a better choice for ultralow-leakage applications, such as sample-hold circuits.

See Chapter 7 for more information.

HEX INVERTER



TOP VIEW

All six inverters may be used independently. On any inverter, a *low* input provides a *high* output, and vice versa.

Device is functionally equivalent to the 7404 (TTL) and 74C04 (CMOS) devices.

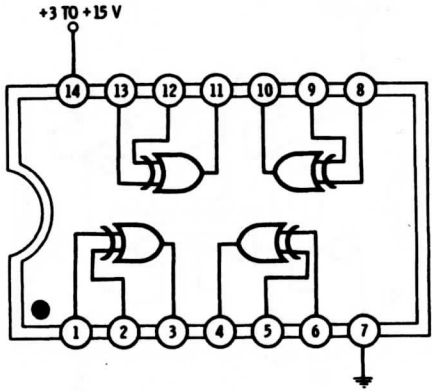
This is a "low-power" version of the 4049. It will not directly drive regular TTL, nor can it be used for voltage translation.

In addition, this device is only singly buffered, which means *the 4069B will perform no better in astable and pulse circuits than ordinary A-series devices.* Thus, while the 4069B has the output drive typical of other B-series devices, it has far less internal gain.

Propagation delay is 25 nanoseconds at 10 volts and 50 nanoseconds at 5 volts. Total package current at 1 megahertz is 0.5 milliampere at 5 volts and 1 milliampere at 10 volts.

4070

QUAD EXCLUSIVE-OR GATE



TOP VIEW

All four EXCLUSIVE-OR gates may be used independently.

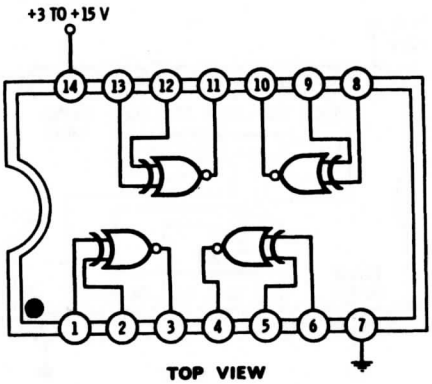
On any one gate, if one input is high but not both, the output will be *high*. If both inputs are *high* or both inputs are *low*, the output will be *low*.

The gate can be used as a comparator by noting that identical inputs give a low output, and different inputs, a high output. It can also be used as a controllable inverter by noting that a low on one input passes on whatever is on the other input; while a high complements whatever is on the other input.

Propagation delay is 70 nanoseconds at 10 volts and 175 nanoseconds at 5 volts. Supply current at a 1-megahertz data rate is 0.2 milliampere at 5 volts and 0.4 milliampere at 10 volts.

This device is identical to the 4508 and replaces the obsolete 4030. It is functionally equivalent to the 7486 (TTL) and the 74C86 (CMOS).

QUAD EXCLUSIVE-NOR GATE



TOP VIEW

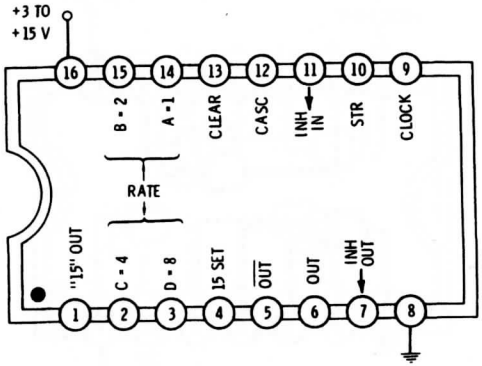
All four EXCLUSIVE-NOR gates may be used independently. On any one gate, if one input is high, but not both, the output will be low. If both inputs are high or both inputs are low, the output will be high.

The gate can be used as a comparator by noting that identical inputs give a high output and different inputs give a low output. It can also be used as a controllable inverter by noting that a high on one input will pass on whatever is on the other input, while a low complements it.

Propagation delay is 70 nanoseconds at 10 volts and 175 nanoseconds at 5 volts. Supply current at a 1-megahertz data rate is 0.2 milliampere at 5 volts and 0.4 milliampere at 10 volts.

4089

BINARY RATE MULTIPLIER



TOP VIEW

This is a special-purpose logic block that may be used to multiply an output pulse rate by a selected amount.

In normal use, pins 4, 10, 11, 12, and 13 are grounded. A clock is routed to pin 9. An input "rate" word, weighted A=1, B=2, C=4, and D=8, is applied to the rate inputs.

An output is provided at pin 6 and its complement is at pin 5. This output will be *one-sixteenth* the clock input multiplied by the input rate word. For instance, with a 16-kHz clock input, a rate word of 0000 produces zero output. A rate word of 0001 produces 1 kHz, 0010 produces 2 kHz, 1011 produces 11 kHz, and so on.

The output pulse rate is an average, and the pulses are usually unevenly spaced. Jitter is inherent in any rate-multiplier circuit. Rate multipliers can be used only where a certain total or a long-term average is all that is needed.

The 15-Set and Clear inputs (pins 4 and 13, respectively) are used to synchronize the start of operation to the zero or maximum count. The Inhibit input stops output pulses if it is high.

Rate multipliers are cascaded by connecting the Inhibit output of the first package to the Inhibit input and strobe of the second package, and the Output of the first package to the Cascade input of the second package. Clock inputs are connected together.

Operating current at a 1-megahertz clock rate is 0.5 milliampere at 5 volts and 1 milliampere at 10 volts. Maximum clock frequency is 4.5 megahertz at 10 volts and 2 megahertz at 5 volts.

The 4527 is a similar decimal unit.