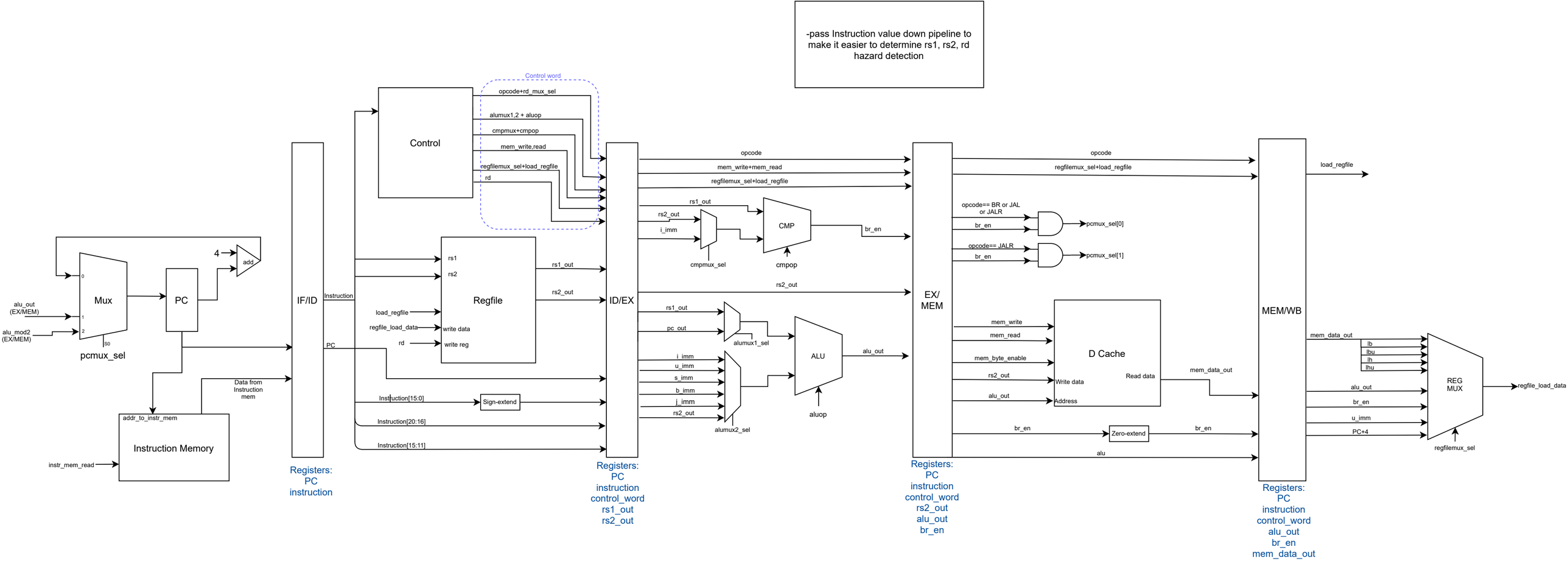
-pass Instruction value down pipeline to make it easier to determine rs1, rs2, rd hazard detection
Control word
Control
opcode+rd_mux_sel
alumux1,2 + aluop
cmpmux+cmpop
mem_write,read
regfilemux_sel+load_regfile
rd
Mux
PC
4
add
0
1
2
s0
alu_out (EX/MEM)
alu_mod2 (EX/MEM)
pcmux_sel
IF/ID
Instruction
PC
Data from Instruction mem
addr_to_instr_mem
Instruction Memory
instr_mem_read
Registers: PC instruction
rs1
rs2
load_regfile
regfile_load_data
rd
write data
write reg
Regfile
rs1_out
rs2_out
Instruction[15:0]
Sign-extend
Instruction[20:16]
Instruction[15:11]
ID/EX
opcode
mem_write+mem_read
regfilemux_sel+load_regfile
rs1_out
rs2_out
i_imm
cmpmux_sel
CMP
cmpop
br_en
rs1_out
pc_out
alumux1_sel
rs2_out
i_imm
u_imm
s_imm
b_imm
j_imm
rs2_out
alumux2_sel
ALU
aluop
alu_out
Registers: PC instruction control_word rs1_out rs2_out
EX/ MEM
opcode
regfilemux_sel+load_regfile
opcode== BR or JAL or JALR
br_en
pcmux_sel[0]
opcode== JALR
br_en
pcmux_sel[1]
mem_write
mem_read
mem_byte_enable
rs2_out
alu_out
D Cache
Write data
Address
Read data
mem_data_out
br_en
Zero-extend
br_en
alu
Registers: PC instruction control_word rs2_out alu_out br_en
MEM/WB
load_regfile
mem_data_out
lb
lbu
lh
lhu
alu_out
br_en
u_imm
PC+4
REG MUX
regfilemux_sel
regfile_load_data
Registers: PC instruction control_word alu_out br_en mem_data_out