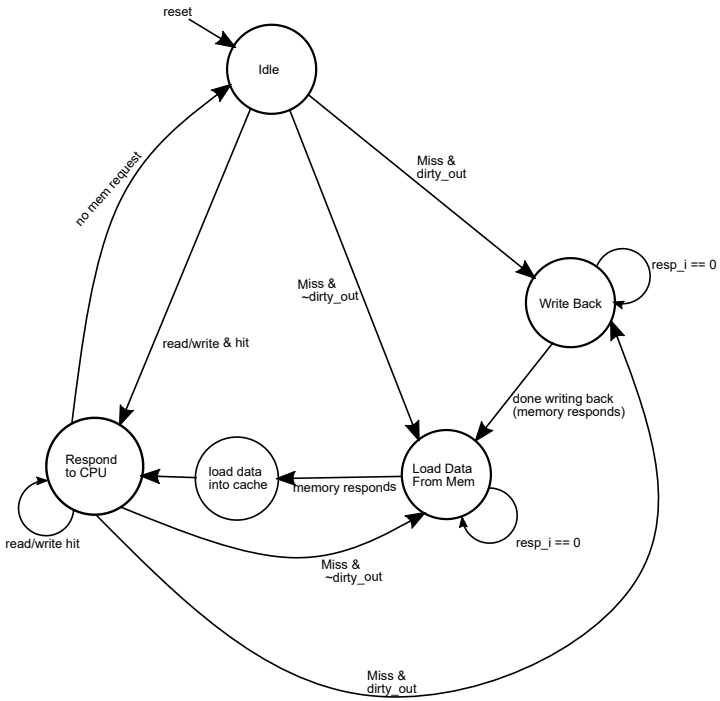

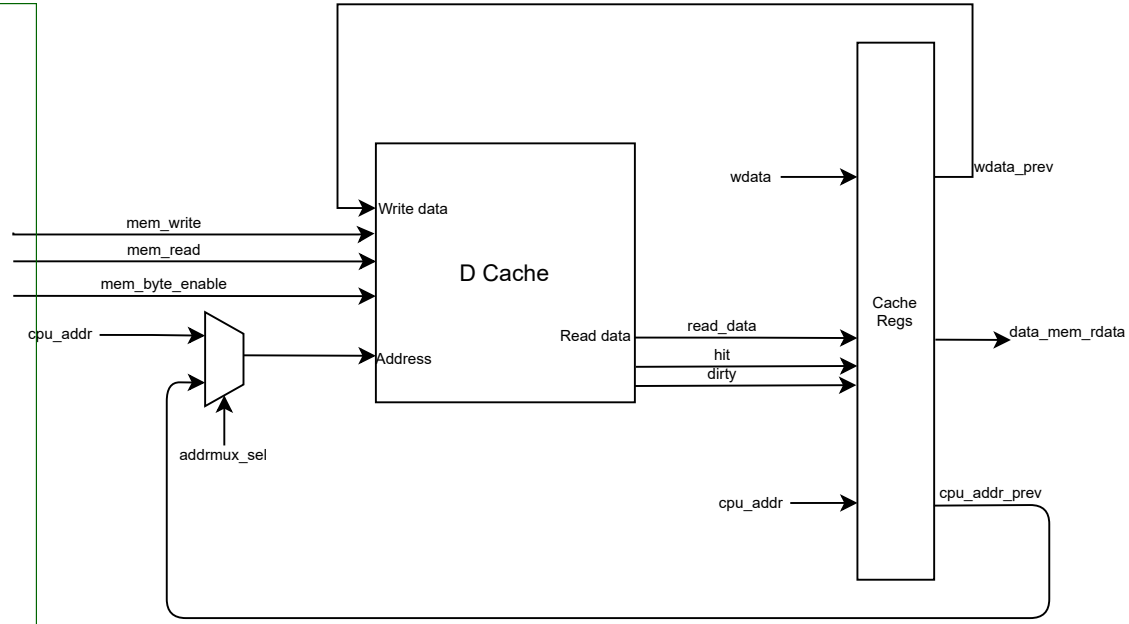

Idle:
-Used for nothing (no read or write)
default signals:

way_sel = hit1
tag_sel = 0
read_from_mem = 0
write_to_mem = 0
load_cache = 0
load_lru = 0
source_sel = 0
read_cache_data = 1

Write_back
-Used when cache is full and data must be written to mem (dirty=1) before getting new data block from memory

write_to_mem = 1
way_sel = lru_out
tag_sel = 0
addrmux_sel = cpu_addr_prev

Respond_to_CPU
-Once we know we have a hit, write to cache if needed, and respond to cpu

mem_resp = 1
way_sel = hit_1
load_lru = 1
load_cache = mem_write
source_sel = 0 (cpu)
addrmux_sel = cpu_addr

Load_Data_From_Mem
-If we have a miss, we need to load a block of memory into the cache

read_from_mem = 1
way_sel = lru_out
tag_sel = 1
addrmux_sel = cpu_addr_prev

Load_Data_Into_Cache
-Need a cycle to put memory into cache

load_cache = 1
source_sel = 1 (memory)
way_sel = lru_out
addrmux_sel = cpu_addr_prev