Team PCB

RISC-V Pipelined Processor

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Checkpoints

Checkpoint 1

- Base RISC-V Pipelined Processor

Checkpoint 2

- L1 Cache
- Hazard & Branch Prediction

Checkpoint 3

- L2 Cache
- Eviction Write Buffer
- M-Extension
- OBL Prefetcher

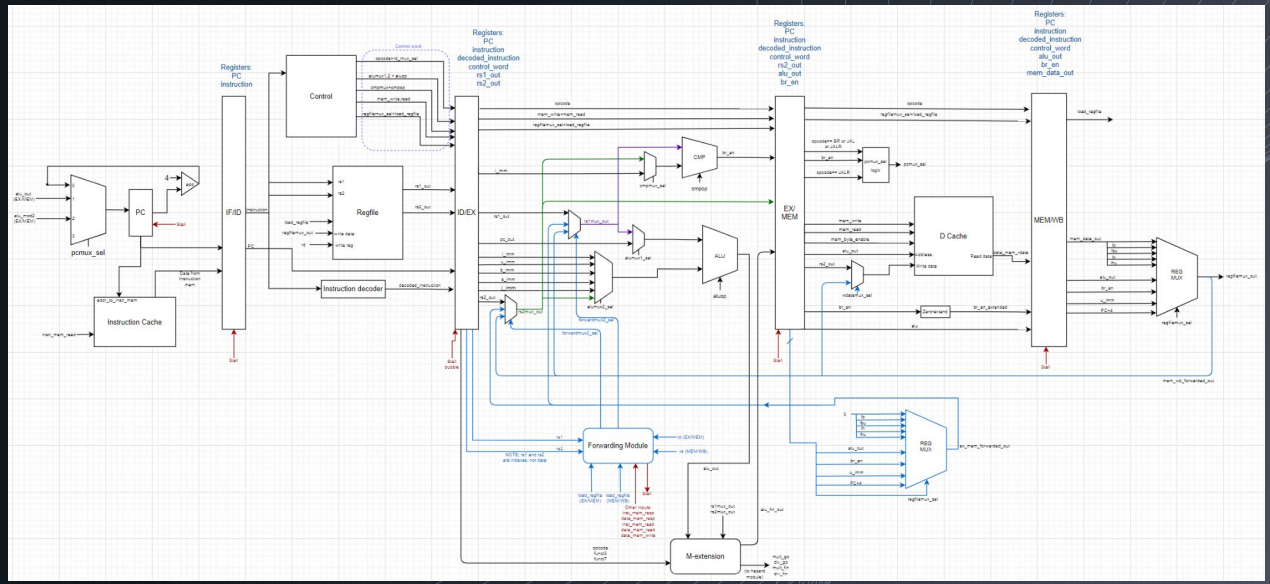
Checkpoint 4

- BRAM
- Improving Fmax
- Optimizing Advanced Features

RISC-V 5-stage Pipeline Processor

Advanced Features:

- L2 Cache, 8-way
- Eviction Write Buffer
- OBL Prefetcher
- M-Extension



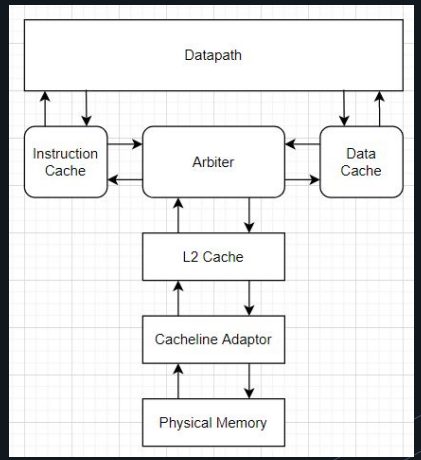
L2 Cache

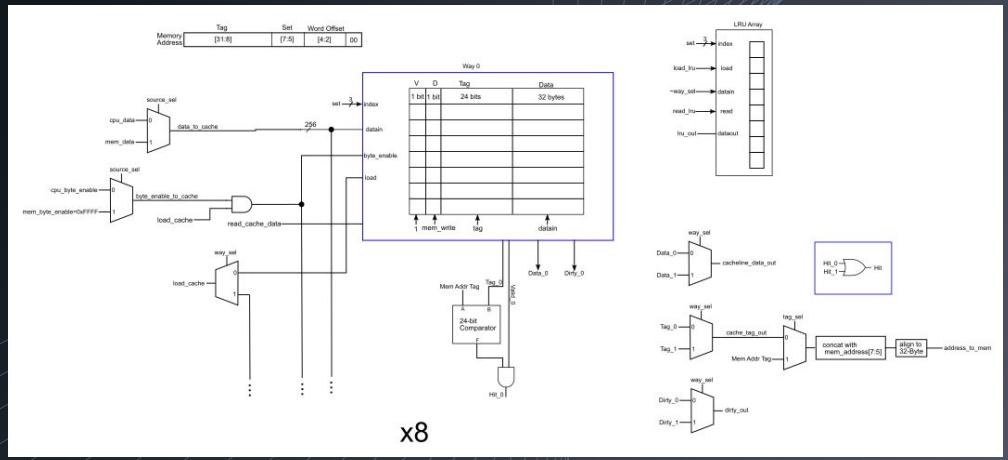
Overview

- 8-way Set Associative
- 2-cycle
- BRAM
- Bit-pLRU

Performance Metrics

- 70% Hit Rate average
- Comp2: 4772 hits, 1131 misses, 15 writebacks
- Reduced comp1 and comp2 times by about 50%, comp1 time by 10%

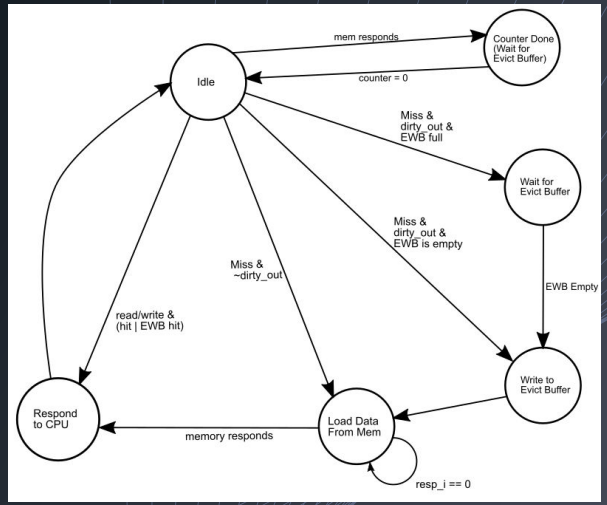


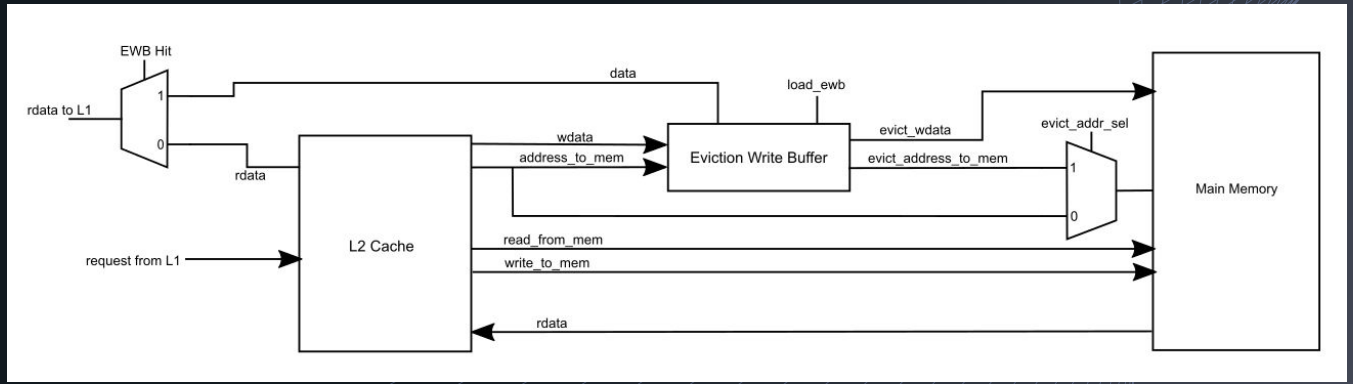


Eviction Write Buffer

Overview
- Small buffer to hold evicted data
- Allows L2 to write back and service misses much faster

Performance Metrics
- 655 writebacks total for competition code
- 31,385 cycles saved
- 24 hits
- Underwhelming performance- relatively few writebacks





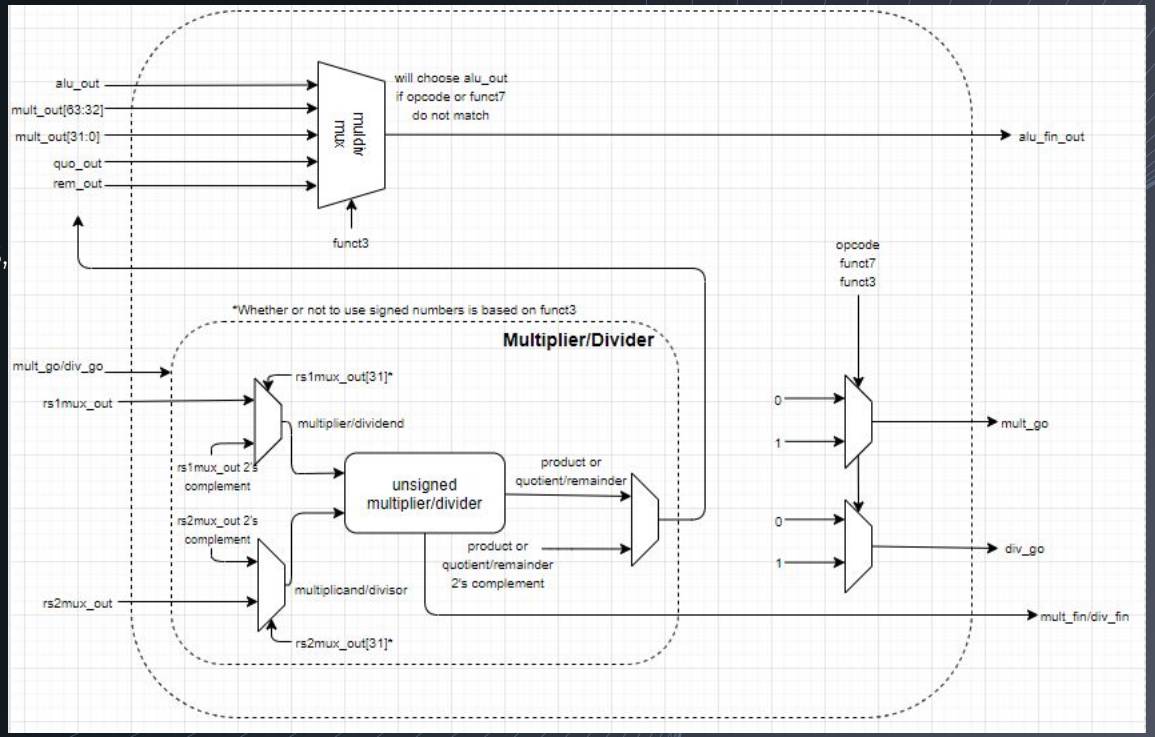
M-Extension

Overview

- Multiplication uses add-shift algorithm
- Division uses shift-subtract algorithm
- Unit testing yielded all correct values, but we couldn't get correct responses with comp2_m.s

Performance Metrics

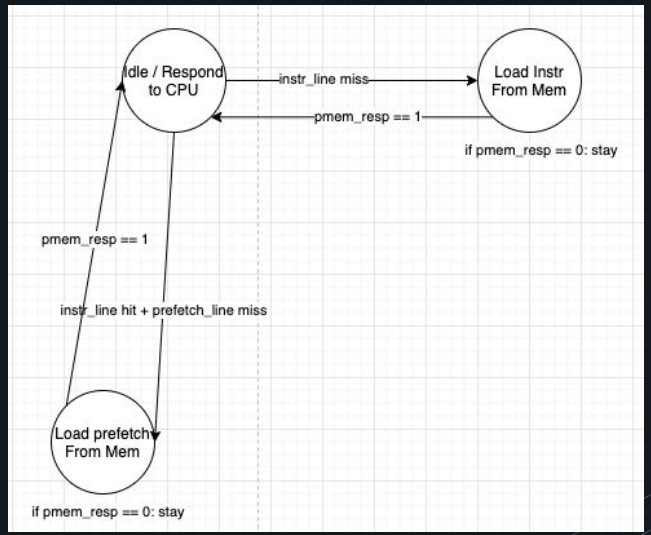
- Two variations of a factorial program, one using only adds and one using our new multiplication operation
- On running these both on the test input 12!:
  - fact_add took 8085 ns
  - fact_mult took 6685 ns
- 17% speedup using mul



OBL Prefetcher

Overview

- Implemented One Block Lookahead Prefetching on Instruction Cache (read-only)
- First responds to original instruction (cache line i), then fetches the block ahead (i+1) from memory if it does not exist in cache
- While waiting on i+1 block from physical memory:
  - Respond to Instruction Requests if it's a Cache Hit
  - Doesn't stall pipeline (unless there is also a data request)



	% of hits	% of hits prefetched	Execution time % diff
comp1	99.64%	83.59%	139.14%
comp2_i	98.39%	72.61%	112.08%
comp3	98.42%	82.04%	131.42%

Overall Performance

	Comp Time	Comp Power	Score
comp1	656,146 ns	884 mW	2.497e-10
comp2_i	2,363,225 ns	867 mW	1.144e-8
comp3	1,867,665 ns	836 mW	5.446e-9

FMax: 96 MHz

Total Score: 2.497e-9

What we wish we had done differently

- EWB did not provide good performance increase
- Difficulties with pipelined cache
- Wallace Tree Multiplier, starting earlier on testing
- Work to reduce power
- OBL Prefetching: Modified Cache Arbiter to override prefetch requests with data requests

Questions?