Modified Cache FSM with Basic OLB Prefetching

Default Signals:

way_sel = 0
tag_sel = 0
read_from_mem = 0
write_to_mem = 0
load_cache = 0
load_lru = 0
source_sel = 0
read_cache_data = 1

Idle

-Used for nothing (no read or write)

Read_cache_data

-After receiving a request to read/write, we must read from the cache to have tag/data/dirty/valid available

read_cache_data = 1
read_lru = 1

Write_back (same for prefetch + regular)

-Used when cache is full and data must be written to mem (dirty=1) before getting new data block from memory

write_to_mem = 1
way_sel = lru_out
tag_sel = 0

Respond_to_CPU

-Once we know we have a hit, write to cache if needed, and respond to cpu

mem_resp = 1

way_sel = hit_0

load_lru = 1

load_cache = mem_write
source_sel = 0 (cpu)

Load_Data_From_Mem (same for prefetch + regular)

-If we have a miss, we need to load a block of memory into the cache

read_from_mem = 1
way_sel = lru_out
tag_sel = 1

Load_Data_Into_Cache (same for prefetch + regular)

-Need a cycle to put memory into cache

load_cache = 1
source_sel = 1 (memory)

Check Cache for Prefetch Data

-As title. Uses default signals like Idle