Brendan Hall

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# Professional Experience

2001 – Present **Technology Fellow**, *Honeywell Aerospace, Advanced Technology*, Golden Valley MN.

Crew Interface and Platform Systems (CIPS) Advanced Technology Group at Honeywell. I am responsible for executing internally and externally funded technology programs. My research areas include fault-tolerant distributed system architectures, model-based-system and safety engineering, system verification, integrated design assurance, and the industrial application of formal methods.

**Successful Record of Funded Research Wins and Execution**

*A primary goal of Advanced Technology is to attract research funding. To support this goal, I have established strong collaborative research partnerships and successfully led several funded research programs. Selected ongoing and past projects are highlighted below:*

2013 – ongoing  **FAA Complex Systems**. Principal Investigator for FAA funded research on the mitigation of complex systems. Research partners include MIT, NDSU, and Certification Services**.**

2013 - ongoing **NASA – AFFIRM**. *Partnering with Galois Inc., I am Co-PI on this program that is developing a Domain Specific Language (DSL) and related syntheses technologies to analyze and implement provably correct distributed systems*.

2013 – 2016 **NASA – Certware**. *Partnering with Kestrel Technology, this program is developing an eclipse based certification workbench, integrating safety and assurance case notations, natural language with formal assurance case reasoning*.

2010 - 2013 **NASA – AFCS**. *Partnering with SRI and WWTechnology, I led this research program targeting the application of formal methods, formal architectural modeling and test generation for distributed fault-tolerant architectures*.

2011 - 2013 **FAA - CRC/Checksum**. *Partnering with Carnegie Mellon University, this research worked to identify aviation best practices for the Selection of Cyclic Redundancy Codes*.

2007 - 2009 **FAA - Data Bus Handbook**, *Co-Author of FAA Handbook for Data Bus Evaluation*.

**Proven Record of Technology Development Leadership**

*Development has focused on distributed platforms systems, and model-based system engineering and analysis tooling. Select projects are highlighted below:*

Current Activities  **Model-Development**

* Championed and deployed formal methods training course
* Championing and pioneering deployment of property based requirements specification methods, supporting the transparent insertion of formal methods technologies, and constrained natural language based test automation
* Pioneering the application of new technologies to support Integrated for Model-Based System Engineering across heterogeneous tooling environments
* Developing new techniques for integrated model-driven safety analysis

2006-2012 **TTEthernet**, I led the Honeywell team for the joint Honeywell, TTTech development of TTEthernet (SAE-AS802), developing the technology from conception through Technology Readiness Level (TRL) 6. Following the selection TT-GbE as the by-wire backbone for the NASA Orion program, I championed and led the development of the Network Integration Lab (NIL) to formally retire the technology risks.

2002 -2015 **Other Developments**, Minimalist TTP-HUB (DO254), Low-cost FlexRay Dependability Augmentation and Gateway, a Low-complexity Partitioned Barrel Processor, and the Braided Ring Availability Integrity Network (BRAIN).

**Proven Track Record of Innovation**

Patents Over 40 patents awarded.

Publications Over 20 papers and 2 book chapters published.

# Prior Professional Experience

2001 – 2002 **Master Software Engineer**, *Hamilton Sundstrand, Electric Power Systems*.

Generic duties included the development of aircraft utility control software for the secondary power distribution cabinet architecture. SW developed in accordance with DO178B, utilizing the Shlaer/Mellor development methodology. Target platform was a MPC750 processor using DiabData C and a proprietary time and space partitioned OS.

Championed and led a pilot study to use COTS tools (MATLAB, Beacon-for-Simulink, DOORS) with in-house scripts for the automatic code generation of avionics utility control software demonstrating significant productivity gain.

Produced influential internal white paper on the application of TTP to secondary power distribution architecture

1998 – 2001 **Principal Software Engineer**, *Honeywell Engines and Systems*, Tucson, AZ.

Generic responsibilities included the design and development of embedded C++ APU Engine Control Software to DO178B. Development tools include Microtec/Diab C++ under UNIX/NT and Rational Rose UML. Platforms include single and dual6833x, MPC509, using in house simple schedulers and COTS RTOS (VRTX). CVS and Clear Case used for CM. One of the prime architects of Tucson’s **Modular Aerospace Control (MAC)** a modular FADEC architecture based upon a TTP/C based fault-tolerant backbone. MAC was awarded research funding from NASA and has been successful in winning significant new business for the Tucson site.

**Honeywell Data Monitor (HDM)**. I led the development of a Windows based tool for target based software monitoring and qualification testing. HDM comprised a win32 (Microsoft Visual C++, MFC, COM) based automation server hosting the script language Python. The tool was successfully deployed (100+ users) to support AS900 engine (D0-178B) certification.

I also initiated and supported the deployment of National Instrument’s Lab Windows CVI and Test Stand to the Tucson production environment

1993 - 1998 **Software Engineer**, *Motorola, AIEG*, Stotfold, UK.

Responsibilities included the strategic planning of test methods and the design of test platforms for new products (automotive power-train ECUs) under development in the department. The work included the design of ATP and environmental stress screening (ESS) systems, in C, C++ and Assembler (68xxxx). Test hardware included ISA, GPIB and VXI instrumentation; the software platforms in use were Microtec, Borland 4.5, Lab-Windows CVI, SourceSafe (for CM).

Championed new modular test development SW architecture that reduced test development time by 8X. Pioneered BDM based test techniques that enabled increased coverage for *Chip-On-Board* based products, and enabled analog in-circuit test systems to achieve digital component test coverage. Traveled to partner companies and sites in Europe to consult and train people in new test techniques.

1993 – 1995 **Test Development Engineer**, *Motorola, AIEG*, Stotfold, UK.

Responsibilities included the design and continuous improvement of test systems for an ISDN PC based video conferencing system. Test systems developed included PC GPIB, and VXI based functional and parametric quality audit systems. Tests implemented to meet BABT manufacturing approval. Activities also included the proving and validation of test equipment; specifying GR&R campaigns and the training of production line and analysis personnel.

1991 – 1993 **Test Package Design Engineer**, *British Aerospace*, Stevenage, UK.

This position incorporated both design and post design support roles. The main responsibilities comprised the design and development of automatic test system software working in C and Pascal on both DOS VxWorks, using GPIB and VXI instrumentation. Post design support of Z80/6502 assembler.

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|  | Education |
| 1989 - 1991 | **BEng.**, *University of Reading*, United Kingdom. Electronic Engineering 2:1 (Hos) |
| 1993 – 1997 | **PGDip.**, *University of Hertfordshire*, United Kingdom. Computer Science |
| 2012 - 2013 | **Honeywell Technical Leadership Development Program**.  Merit based course participation |
| 2014 | SCRUM Master Certification.  Computer Languages and Skills |
| Proficient | C/C++, Python, Prolog, VHDL, VHDL-AMS, AADL, UML, SysML, PSL, MS-Office, Latex |
| Learning | Haskell, nodejs, HTML-5, PVS |
| Tools | SCADE, SCADE-SYSTEM, OSATE, Altera-Quartus and NIOS, ModelSim, SAL |
| Processes | Aerospace Certification (DO-178 B/C, DO-254, DO-297, ARP-4754A, 4761, 5107).  Awards and Recognition |
| 2010 | **NASA Space Flight Awareness Team Award**.  For work relating to TT-GbE Development and Technology Maturation |
| 2010 | **Technical Achievement Award**, *Honeywell - Aerospace Wide*.  For work relating to fault-tolerant networking. |
| 2008, 2010 | **Outstanding Engineer Award**, *Honeywell*. Peer nominated (1% of Honeywell population). |
| 2003 | **Technical Achievement Award**, *Honeywell*.  For work fault-tolerant field-bus development. |
| 1991 | **Apprentice Award Winner**, *British Aerospace Dynamics (UK)*.  Interests |
| Memberships | Member of IEEE, INCOSE, SAE. Active on SAE AS-2C and AS-2D committees. |
| Community | First League Lego Coach 2012, 2013, 201,2016 |
| Hobbies | Robotics, 3D printing, swimming, Music (Used to play a in Celtic Rock Band). |

# Publications

1. Devesh Bhatt, Brendan Hall, Samar Dajani-Brown, Steve Hickman, and Michael Paulitsch. Model-based development and the implications to design assurance and certification. In *Digital*

*Avionics Systems Conference, 2005. DASC 2005. The 24th*, volume 2, pages 13–pp. IEEE, 2005.

1. Linda Briesemeister, Grit Denker, Daniel Elenius, Ian Mason, Srivatsan Varadarajan, Devesh Bhatt, Brendan Hall, Gabor Madl, and Wilfried Steiner. Quantitative fault propagation analysis for networked cyber-physical systems. *2nd analytic virtual integration of cyber-physical systems workshop (AVICPS)*, 2011.
2. Kevin Driscoll, Brendan Hall, Philip Koopman, Justin Ray, and Mike DeWalt. Data network evaluation criteria handbook. 2009.
3. Kevin Driscoll, Brendan Hall, Håkan Sivencrona, and Phil Zumsteg. Byzantine fault tolerance, from theory to reality. In *Computer Safety, Reliability, and Security*, pages 235–248. Springer Berlin Heidelberg, 2003.
4. Kevin Driscoll, Brendan Hall, Håkan Sivencrona, and Phil Zumsteg. Paper h. *On the Design and Validation of Fault Containment Regions in Distributed Communication Systems*, page 163, 2004.
5. Kevin Driscoll, Brendan Hall, and Srivatsan Varadarajan. Maximizing fault tolerance in a low-swap data network. In *Digital Avionics Systems Conference (DASC), 2012 IEEE/AIAA 31st*, pages 7A2–1. IEEE, 2012.
6. Kevin R Driscoll, Madl Gabor, and Brendan Hall. Modeling and analysis of mixed synchronous/asynchronous systems. 2012.
7. Kevin R Driscoll, Brendan Hall, and Kevin Schweiker. Application agreement and integration services. 2013.
8. Bruno Dutertre, Arvind Easwaran, Brendan Hall, and Wilfried Steiner. Model-based analysis of Timed-Triggered Ethernet. In *Digital Avionics Systems Conference (DASC), 2012 IEEE/AIAA 31st*, pages 9D2–1. IEEE, 2012.
9. Arvind Easwaran, Brendan Hall, and Kevin Schleicher. Model-driven test generation of distributed systems. 2012.
10. B Hall, M Paulitsch, and K Driscoll. 2007-01-1492 Flex ray brain fusion a Flexray-based braided ring availability integrity network. *SAE SP*, 2121:73, 2007.
11. Brendan Hall, Kevin Driscoll, Michael Paulitsch, and Samar Dajani-Brown. Ringing out fault tolerance. a new ring network for superior low-cost dependability. In *Dependable Systems and Networks, 2005. DSN 2005. Proceedings. International Conference on*, pages 298–307. IEEE, 2005.
12. Brendan Hall, Kevin Driscoll, and Kevin Schweiker. Verification and validation of flight critical systems (VVFCS). In *Digital Avionics Systems Conference (DASC), 2012 IEEE/AIAA 31st*, pages 1–18. IEEE, 2012.
13. Brendan Hall, Kevin R Driscoll, and Gabor Madl. Investigating system dependability modeling using aadl. 2013.
14. Brendan Hall, Michael Paulitsch, Dewey Benson, and Alireza Behbahani. Jet engine control using Ethernet with a brain. *AIAA*, 5291, 2008.
15. Brendan Hall, Michael Paulitsch, and Kevin Driscoll. Flexray brain fusion a Flexray-based braided ring availability integrity network. *Training*, 2013:10–02, 2007.
16. Brendan Hall, Michael Paulitsch, Kevin Driscoll, et al. Port driven authentication in a network, February 23 2010. US Patent 7,668,204.
17. Brendan Hall, Michael Paulitsch, and Kevin R Driscoll. Escape CAN limitations. 2007.
18. Brendan HALL, Brian Sellner, and Reinhard MAIER. Automated safety critical software development for distributed control systems: A cots approach. *SAE transactions*, 110(7):293– 302, 2001.
19. Brendan Hall, Brian Sellner, and Reinhard Maier. Modular aerospace controls. *Aerospace Engineering*, 21(8):37–39, 2001.
20. Roman Obermaisser. *Time-Triggered Communication*. CRC Press, Inc., 2011. Contributed two chapters. One on BRAIN one TTEThernet.
21. Michael Paulitsch and Brendan Hall. Insights into the sensitivity of the brain (braided ring availability integrity network)–on platform robustness in extended operation. In *Dependable Systems and Networks, 2007. DSN’07. 37th Annual IEEE/IFIP International Conference on*, pages 154–163. IEEE, 2007.
22. Michael Paulitsch and Brendan Hall. Flexray in aerospace and safety-sensitive systems. *Aerospace and Electronic Systems Magazine, IEEE*, 23(9):4–13, 2008.
23. Michael Paulitsch and Brendan Hall. Starting and resolving a partitioned brain. In *Object Oriented Real-Time Distributed Computing (ISORC), 2008 11th IEEE International Symposium on*, pages 415–421. IEEE, 2008.
24. Michael Paulitsch, Jennifer Morris, Brendan Hall, Kevin Driscoll, Elizabeth Latronico, and Philip Koopman. Coverage and the use of cyclic redundancy codes in ultra-dependable systems. In *Dependable Systems and Networks, 2005. DSN 2005. Proceedings. International Conference on*, pages 346–355. IEEE, 2005.
25. Stefan Poledna, Martin Schwarz, Guenther Bauer, Wilfred Steiner, Brendan Hall, and Michael Paulitsch. Autocratic low complexity gateway/guardian strategy and/or simple local guardian strategy for Flexray or other distributed time-triggered protocol, April 29 2009. EP Patent 2,053,830.
26. William Todd Smithgall, Brendan Hall, and Srivatsan Varadarajan. Time triggered Ethernet system testing means and method, March 7 2013. US Patent 20,130,058,217.
27. Wilfried Steiner, Günther Bauer, Brendan Hall, Michael Paulitsch, and Srivatsan Varadarajan. TTEthernet dataflow concept. In *Network Computing and Applications, 2009. NCA 2009. Eighth IEEE International Symposium on*, pages 319–322. IEEE, 2009.
28. Wilfried Steiner, Günther Bauer, Matthias Wächter, Michael Paulitsch, and Brendan Hall. Method for synchronizing local clocks in a distributed computer network, March 23 2011. EP Patent 2,297,886.