

Thermoelectric modeling of the ATLAS ITk Strip Detector

Kurt Brendlinger¹, Georg Viehhauser¹, Graham Beck¹, Yu-Heng Chen¹

Abstract

Here is the abstract.

Keywords: Silicon detector, Thermal runaway, Thermal management, Cooling

1. Introduction

The temperatures in silicon detector systems are critically important for the performance of these systems. The leakage current shows a pronounced temperature dependence

$$I \propto T_S^2 e^{-T_A/T_S}, \quad (1)$$

where T_S is the sensor temperature and $T_A \simeq 7000$ K. Leakage currents can become particularly significant after irradiation of the silicon material. The heat generated by these leakage currents in the silicon sensor, together with the heat from front-end electronic components on the detector, needs to be removed by cooling systems. Due to the strong growth of leakage power with temperature there is a critical temperature T_{crit} above which the heat cannot be removed quickly enough, and the detector becomes thermally unstable ('thermal runaway')¹. The capability of the cooling system to remove this heat is limited by the temperature of the local cold sink (typically the coolant temperature) and the thermal impedance of the heat path between the source (electronics and sensor) and the sink.

In addition, there can be aspects of the front-end electronics that are temperature-dependent. For example, in the strip system for the ATLAS Phase-II upgrade [1] there are two additional temperature-dependent heat sources. The first is a radiation damage effect in the digital part of the readout electronics (the ABC130 and HCC chips), which is manufactured in 130 nm technology by the CMOS 8RF process (ref). This effect leads to an increase of the digital power in the chip depending on the received dose rate (TID) and the temperature of the chip (ref). This has been first observed in the ATLAS IBL [2]. The other temperature dependence of the power generated by the front-end electronics stems from the converter chip (FEAST (ref)) used in the on-detector DC-DC converter system supplying power to the front-end electronics.

Even before the limit of thermal stability is reached, knowledge of temperatures in silicon detector systems is important, as they define system parameters like power supply capacity and cable dimensions.

In principle the temperatures in the system for a given set of operational parameters (power density, thermal conductivities, etc.) can be predicted by FEA to an accuracy that is limited only by the quality of the input parameters. However, this is a time-consuming process and can be prohibitively difficult if a number of local heat sources depend non-linearly on the temperature. A simplification to this problem that allows for an analytical solution in the case of a simple heat source topology has been developed in [3]. Here we develop this method further to include several temperature-dependent non-linear heat sources in the front-end electronics. The resulting set of equations cannot be solved analytically anymore, but with little effort using numerical problem solvers. This enables us to predict with some confidence the temperatures and power requirements in the ATLAS strip system throughout Phase-II operation. The results from this prediction have been used throughout the project to consistently dimension the different systems (cooling, power, services, etc.) also with some robustness due to the inclusion of a common set of safety factors. This method can be easily adapted to any other system by adjusting to the system-specific geometries and parameters.

¹In a real detector system the resulting growth of sensor temperature would be arrested by overcurrent limits in the power supplies, resulting in a reduction of the bias voltage, which in turn will degrade the S/N performance of the system.

1.1. The ATLAS strip system

The strip system for the ATLAS Phase-II upgrade [1] consists of two parts: the barrel system comprises four concentric cylindrical barrels, and the two endcaps, which consist of six disks each.

In the barrel, the detector modules are made of square sensors ($96.85 \times 96.72 \text{ mm}^2$) with a hybrid on top, which hosts the front-end chips (ABC130 and HCC), but also circuitry to convert the supply voltage of larger than 10 V to the chip voltage of 1.5 V. This circuitry is controlled by the FEAST chip. The modules are glued onto both sides of a composite sandwich that contains two parallel thin-wall titanium cooling pipes embedded in carbon foam (Allcomp K9 - ref) between two facesheets of UHM carbon fibre (3 layers of K13C2U/EX1515) with a co-cured Kapton/copper low-mass tape. A model of this geometry is shown in Fig. 1. During final operation, cooling will be achieved by evaporating CO₂ in the cooling pipes with a final target temperature no higher than -35°C anywhere on the stave. The geometry of the stave is uniform along its length, with the exception of the end region of the stave, where an End-Of-Structure (EOS) card is mounted on both surfaces, which shares part of the heat path from the module, and where the thermal path is degraded by the presence of electrically-insulating ceramic pipe sections.

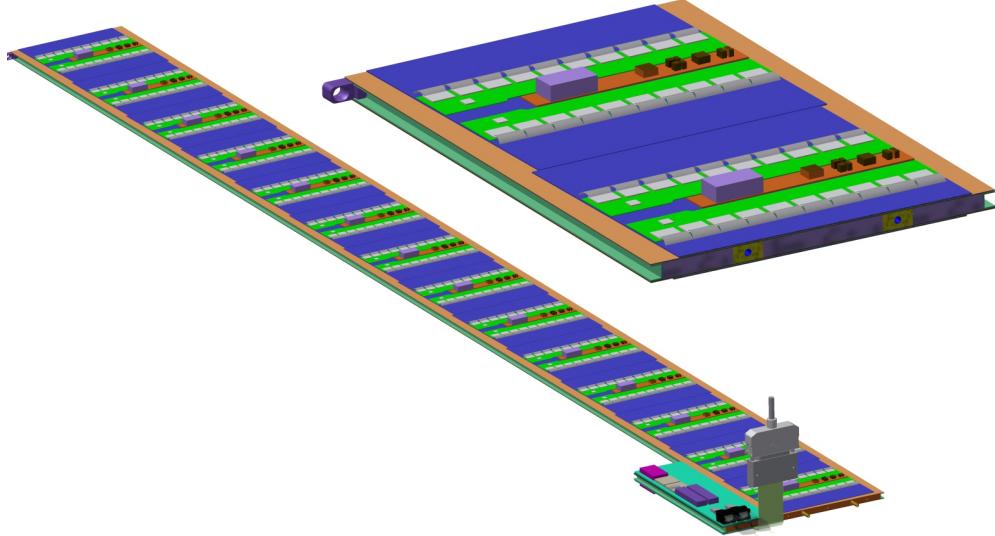


Figure 1: Strip barrel local support geometry. On the left, a complete stave is shown (EOS card in the foreground). The right picture shows a cross-section of the stave with the two cooling pipes visible inside the core.

The endcap detector consists of six disks, each containing 32 ‘petals’ loaded on both sides with six silicon modules (twelve in total). The endcap detector modules consist of six distinct designs located at increasing radius from the beam pipe and labeled R0 through R5 (where ‘R’ stands for ring). Each endcap module consists of one or two irregularly-shaped silicon sensors, and a varying number of front-end chips on each module (between 12 and 28 ABCs, and 2 to 4 HCCs). The EOS card is located adjacent to the R5 module, but the cooling pipes (without electrical breaks) run directly underneath it without a shared heat path, in contrast to the barrel EOS. The remaining module and petal core design details are largely identical to the barrel module description above. Fig. 2 depicts the geometry of the endcap petal.

Figure 2: Endcap strip geometry

1.2. Radiation environment

A key input to the calculation is the radiation environment of the strip system, as several inputs depend on radiation damage effects. The sensor leakage current can be parametrized as a function of the fluence

expressed in 1 MeV neutron-equivalents, and the TID effect on the digital chip current will be described as a function of the total ionizing dose rate (more details on its dependencies can be found in Section 6).

Predictions for both of these parameters for each point in the ITk are available which have been generated using the FLUKA particle transport code and the PYTHIA8 event generator (Fig. 3) [ref]. Both of these distributions display a weak dependence on z in the barrel, whereas they vary significantly along r and z over the length of the endcap petals. Because of this, and the linear uniformity of the stave compared to the more complex geometry along a petal, we modelled only two types of modules for the barrel (a generic module along the linear part of the stave and the module next to the end-of-structure card), but six different types of modules in a petal.

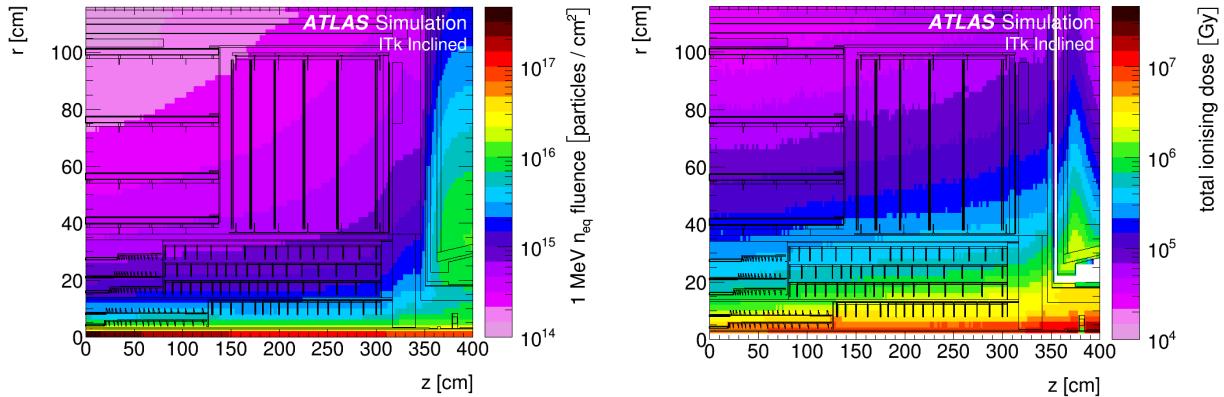


Figure 3: ATLAS ITk radiation environment. 1 MeV neutron equivalent fluence (left) and total ionizing dose (right). Both plots are for an integrated luminosity of 4000 fb^{-1} [1].

2. The electrical model

The electrical model consists of low-voltage (LV) and high-voltage (HV) circuits, depicted in Fig. 4. The LV current is used to power the hybrid controller chips (HCCs), ATLAS Binary Chips (ABCs) and Autonomous Monitoring and Control chip (AMAC) located on PCBs that are glued directly onto the surface of the sensor. The number of chips vary according to the design of each different module type (barrel short-strip and long-strip modules, and six different endcap module designs).

The ABCs and HCCs are all powered at 1.5 V using a DCDC converter (the FEAST) to step the voltage down from 11 V (linPOL12V and bPOL12V in Fig. 4). Typically one FEAST per module is used to power the chips; however, due to the large number of ABCs on endcap module R3, the load is split across two FEAST converters on the module.

The AMAC contains a component powered at 1.5 V and one powered at 3 V; both are delivered from the 11V source by an LDO regulator with a 1.9 mA quiescent current. Again, the endcap module R3 differs from other modules, containing two AMACs each powered by its own LDO.

The bus tape, which carries both LV and HV currents, has a small wire resistance, which impacts the module in two ways. First, the tape itself will radiate some heat according to the amount of current passing through it; this source of heat is accounted for in the model, however the contribution to the total module power is negligible. Second, the voltage supplied to the module will be affected by the small ΔV in the bus tape. This effect is largest for modules on the non-EOS end of the barrel stave or endcap petal, where the current has traveled a longer distance. The treatment of this effect is slightly different in the barrel and endcap models: in the barrel, the voltage delivered to every module is set at 10.5 V; in the endcap, the ΔV is estimated based on the calculated expected power loss along the tape for each module. In both cases, the impact of using a different treatment is small.

The low-voltage current is also delivered to the EOS card to power various data transfer components, which require 2.5 V and 1.2 V supplies. On the EOS, a FEAST identical to the one used on the module is used to step the voltage down from 11 V to 2.5 V; an additional LDO regulator brings the 2.5 V down to

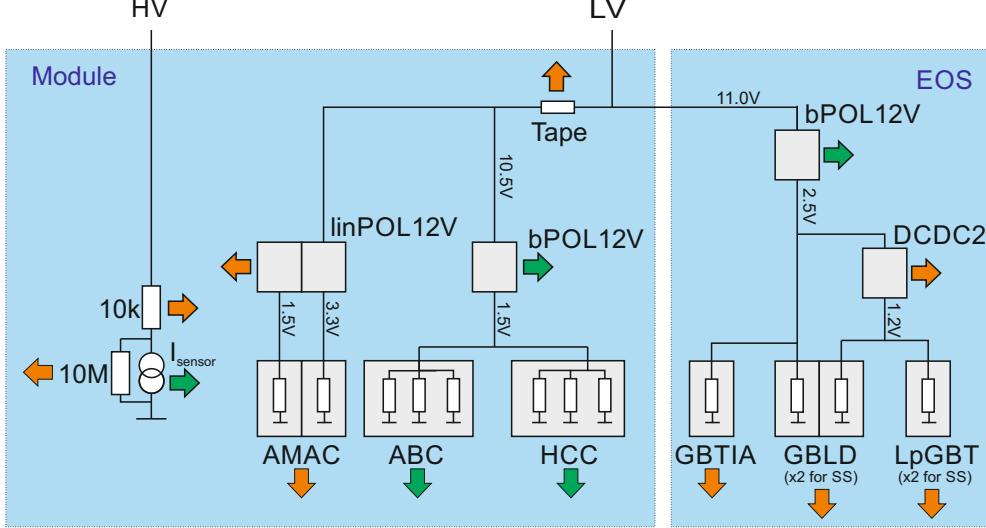


Figure 4: The electrical model of the ITk Strip barrel and endcap modules. Green arrows represent temperature-dependent heat sources, while orange arrows are temperature-independent. Grey squares are chips. Chip counts per module are linPOL12V/bPOL12V/AMAC: 1 each (2 each for EC R3); HCC: 1 for barrel LS, 2 for barrel SS and EC R0-R2 and R4-R5, 4 for EC R3; ABC: barrel: 10, 20 (LS, SS), EC: 17, 21, 21, 28, 16, 18 (R0-R5).

1.2 V for some components. The EOS cards on the endcap petals and the long-strip staves have one GBLD and one LpGBT; EOS cards on the short-strip staves contain two of each. All EOS cards contain one GBTIA.

Finally, the HV current provides the voltage bias on the silicon sensors. An HV multiplexer switch (HVMUX) is placed in parallel to the sensor, which can be used to disconnect the sensor from the bias line. Two HV filters with an effective resistance of $10\text{ k}\Omega$ are placed in series with the sensor. The nominal operating voltage of the sensor is expected to be 500V, but the system is designed to operate with a voltage bias of up to 700V.

3. The thermal model

The thermal network consists of heat sources (some of which are temperature dependent) and thermal resistances. The latter are given by the properties of the mechanical design (heat conductivities of the materials) and the geometry of the heat path. The geometry is generally 3-dimensional, but it is the strategy of the simple network models to lump the 3-dimensional behaviour into one thermal resistance parameter. In the models discussed here we have used a granularity corresponding to single detector modules for which the thermal resistance has been modelled. The temperatures in the model are then given for the nodes in the network in analogy to the potentials in an electrical network.

The complexity of the thermal network used in this study (see Fig. 5) is given by the variety of different temperature-dependent heat sources in the ATLAS strip system. These sources consist of the digital power for each type of chip, the heat generated by the FEAST chip providing the on-detector DC-DC conversion, and the sensor leakage currents. In the ATLAS ITk strip modules all of these components are located on top of the sensors, such that the heat generated in them flows through the sensor into the support structure, the stave (barrel) or petal (endcap) core with the embedded cooling pipe. In the network model, the heat flow from these sources is combined and flowing through a common impedance R_M to the sink at a temperature T_C . For each of the temperature-dependent heat sources (ABC, HCC, FEAST and the sensor) we have added a resistance from the common temperature T_{mod} to allow for a finite and different heat path for each of them. Finally, the End-of-substructure (EOS) card adjacent to the last module on the barrel stave (endcap petal) is modeled as an additional source of heat with an independent impedance for its unique thermal path.

This is a more complex thermal network than the one studied in Ref. [3], where an analytical solution for the determination of thermal stability was given. In particular, because of the non-linear temperature

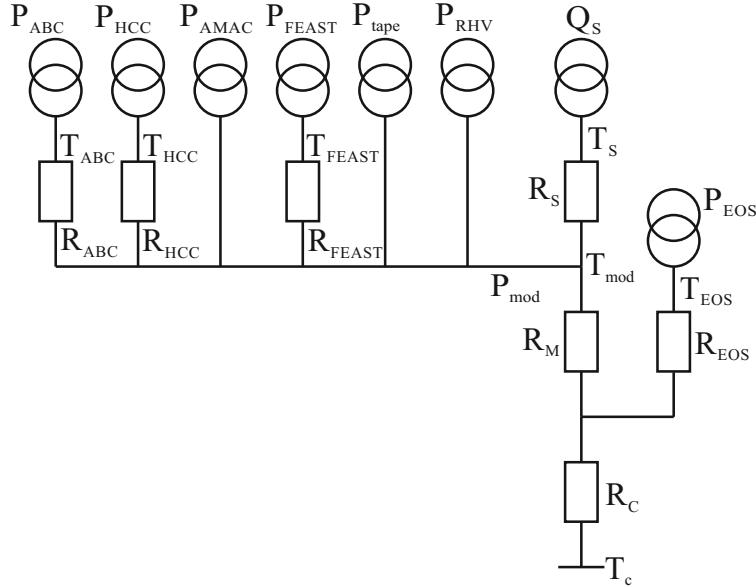


Figure 5: Thermal network model.

dependence of some of the heat sources, it is not possible in this case to solve the set of equations describing the model analytically. However, the set of equations is still sufficiently small to solve numerically using functional programming languages such as Mathematica (used in the barrel model) or Python (used in the endcap system).

4. Obtaining thermal impedances using FEA

Explain the method of extracting impedances of thermal pathways using FEA.

5. Other model inputs

The two temperature-dependent elements of the thermoelectric model—the radiation-induced digital current increase in the front-end chips, and the efficiency of the FEAST DCDC converter—are described in this section. Both effects are studied experimentally and fit with functional forms in order to accurately represent them in the model. The uncertainty in the experimental data, and in our modeling assumptions, are estimated here and considered in the evaluation of safety factors, described in detail in Section 7.2.

5.0.1. DCDC converter

The DCDC converter (FEAST) supplies a low-voltage (1.5 V) current to the ABC130 and HCC front-end chips on the module. The efficiency of the FEAST depends on its temperature as well as the output (load) current load delivered to the front-end chips. To correctly model the FEAST efficiency, experimental measurements have been performed to characterize the dependence and fitted with a functional form.

To measure the FEAST efficiency, the FEAST power board was glued to an aluminum cold plate, cooled with CO₂, and powered with the nominal working input and output voltages (11 V input, 1.5 V output). The temperature of the FEAST was measured with an NTC thermistor and PTAT sensor residing on the FEAST, for a range of load currents up to the maximum design current of 4A².

The data was then fit with a function with sufficient parameters to ensure reasonable agreement; the choice of functional form has no physical interpretation. Figure 6 depicts the FEAST efficiency data and

² FEAST data spreadsheet: http://project-dcdc.web.cern.ch/project-dcdc/public/Documents/FEASTMod_Datasheet.pdf. Cite?

the parameterized fit used in the model. The parameterization fits the data with an accuracy below 1%; this uncertainty in the FEAST efficiency modeling is small compared to other uncertainty sources, and is therefore neglected in our model.

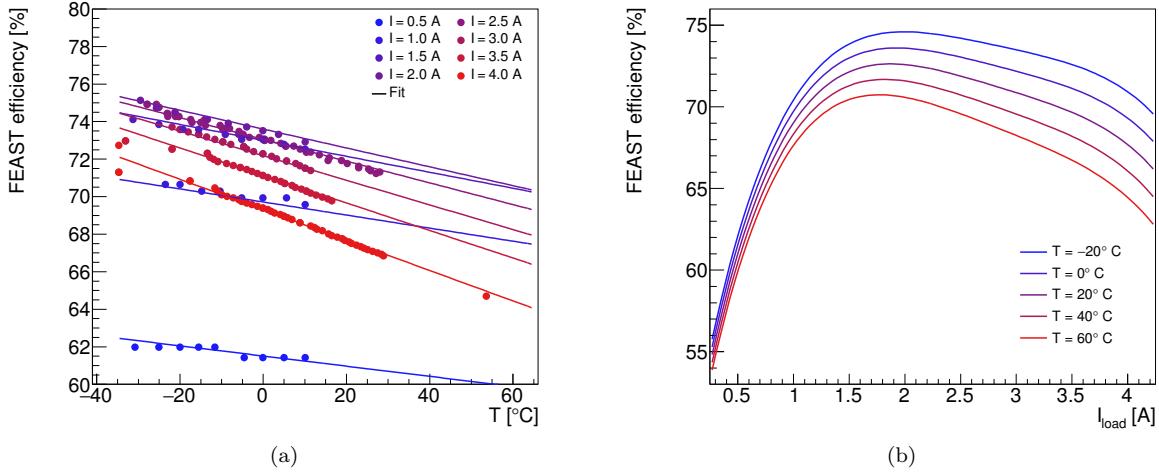


Figure 6: The FEAST efficiency model based on experimental data. (a) The experimental data points characterizing the FEAST efficiency are plotted as dots and color coded for load current. The data is compared to the analytic fit, evaluated in curves of equal current. (b) The same analytic fit, presented as a function of current load for curves of equal temperature.

5.0.2. Digital current increase of chips using 130 nm CMOS technology

The ABC and HCC chips, designed using IBM 130 nm CMOS8RF technology, are known to suffer from an increase in digital current when subjected to a high-radiation environment [1]. This phenomenon, known as the “TID bump,” is well-studied [4, 5] and has a characteristic shape whereby the effect reaches a maximum as a function of the accumulated dose and then gradually diminishes (see Fig. 7).

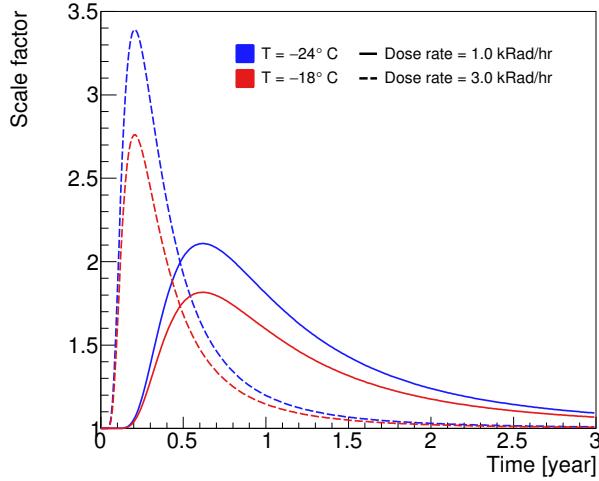


Figure 7: Parametrization of the impact of the total ionizing dose on the magnitude of the front-end chip digital current (the TID bump), presented as a function of time. The current is multiplied by a scale factor that is modeled as a function of total ionizing dose, dose rate, and temperature, based on experimental data.

In an effort to characterize the nature of the TID bump in the ABC and HCC chips empirically, many irradiation campaigns have been conducted using a variety of radiation sources, testing the effect at different

temperatures and dose rates. The data collected from these studies was used to develop a model of the TID bump that estimates the digital current increase given the total ionizing dose, the dose rate, and the operating temperature of the chip. This parameterization, which is depicted in Fig 7, is used as an input to the thermoelectric model in order to correctly model the ABC and HCC currents. The TID bump is assumed to fully apply to the HCC digital current, and apply to 69% of the ABC digital current (according to our understanding of its digital circuitry).

The TID bump displays certain key features, which are reflected in the parameterization: first, the effect is larger at colder temperatures and higher dose rates. This means it can be mitigated by operating the chips at higher temperature (note that the dose rate is fixed by the LHC conditions). Second, the figure also illustrates how chips receiving different dose rates will reach their maximum digital current increase at different times. This feature is particularly important when modeling the total power consumed by the barrel and endcap systems. In both systems, the dose rate varies significantly depending on the position of the module in the detector. The effect means that the maximum system power will be smaller than the sum of the maximum power of each module, as each chip reaches its maximum at a different point in time.

The TID bump is an important source of uncertainty in our model. The experimental data suggests a relatively large variation in the TID bump effect, in particular between different batches of the same type of chip delivered by the manufacturer, suggesting an unknown effect in the fabrication process. To estimate the uncertainty in the TID bump, the parameterized function is fit again using only the worst-performing data (defined as having the largest TID bump effect). This “pessimistic” parameterization is used as a safety factor to estimate the detector performance in worst-case scenarios.

The irradiations of individual chips have typically been performed at constant dose rate and temperature. In our model calculations both of these parameters vary throughout the evaluation. In our parametrization we use only the instantaneous value of these two parameters, thus neglecting any possible history of the TID effect. We also ignore any short-time effects due to variations in the dose rate on the scale of hours or days. This approach is mandated by the lack of more varied experimental data and the absence of a good theoretical model for this effect. This probably constitutes the largest source of unknown errors for our model.

5.0.3. Radiation-dependent leakage current

The radiation-induced leakage current can be parametrized as a function of the hadron fluence expressed in 1 MeV equivalent neutrons. The parametrizations we have used for the evaluation of our model are shown in Fig. 8 [ref Marcella Mikestikova]. The currents given there are at a sensor temperature of -15°C and are scaled in our model to the specific sensor temperature using eq. 1.

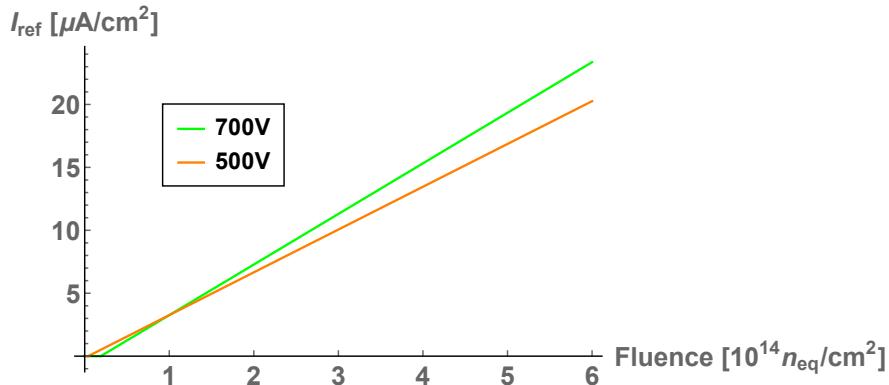


Figure 8: Parametrization used for the leakage current at -15°C as a function of the fluence for two different sensor bias voltages.

6. Running the model

The thermoelectric model constructs a profile of the sensor module operation conditions over the lifetime of the detector in the following manner. First, assuming a reasonable set of initial component temperatures,

the module total power (including all components, but excluding the sensor leakage power) and the sensor temperature without leakage current (T_0) is calculated assuming these initial temperatures. The initial value for the module power is used to solve for the sensor power and temperature accounting for leakage current, using the thermal balance equation and the relationship from Eq. 1. Using this calculated sensor leakage current and temperature, the power and temperature of the module components are updated given the initial (year 0, month 0) startup parameters.

Next, the module conditions of the following month (year 0, month 1) are calculated. Using the component temperatures calculated from the previous month and the operational parameters (ionizing dose and dose rates) from month 1, the module total power (excluding sensor leakage) is again calculated, and subsequently the sensor temperature and leakage current are computed. Following this, the module component temperatures and power values are derived for this month. This process is repeated in one-month steps until the final year of operation, or until a real solution for the sensor temperature does not exist, indicating that thermal runaway conditions have been reached.

In the barrel subsystem, the above procedure is performed four separate times to represent the radiation conditions of the four barrel layers located at different radii from the beam axis³ for both, a module next to the EOS card (hereafter referred to as ‘EOS module’) and a module along the length of the stave away from the EOS card (‘normal module’). Thus in total, 8 modules are simulated for the barrel (4 layers \times normal/EOS), and they are combined in their proper proportion to simulate the entire barrel system.

In the endcap subsystem, the total ionizing dose and dose rates vary significantly depending on the position of the module; furthermore, the design of each module on a petal differs significantly. Therefore, all 36 module types (6 rings \times 6 disks) are simulated independently, and combined to represent the full endcap.

We have implemented this algorithm in Mathematica (barrel) and Python (endcaps). In both cases the calculation for a set of operating conditions over the full lifetime of the LHC takes between 5 and 10 minutes on a standard PC, thus enabling a quick turn-around for systematic studies of the parameter space.

7. Outputs of the thermoelectric model

7.1. Operational scenarios

To study the different aspects of our predictions for the operation of the ITk strip system throughout its lifetime, we performed the calculation of the system parameters over the expected 14 years of operation in monthly steps as outlined in section 6. Time-dependent inputs to the calculations were given from the expected performance of the LHC (Fig. 9a) and different profiles for the cooling temperature. We studied flat cooling temperature scenarios at different temperatures starting at -35°C , the lowest evaporation temperature achievable with the ITk evaporative CO_2 cooling system, and a ‘ramp’ scenario in which the cooling temperature starts at 0°C and gradually is lowered down to -35°C over the course of 10 years (Fig. 9b).

7.2. Safety factors

To ensure the robustness of the system design against errors in the assumptions used in the model, we also evaluate the model using a set of input parameters with some key inputs degraded. The set of safety factors used is given in Table 1. Each safety factor has been estimated individually based on experience, the complexity of the system aspect described by the parameter, and from available data or the absence of such data. Note that the model can be evaluated with all the safety factors listed in Table 1 used together, a situation which is unlikely to occur in the real system, to provide a worst-case estimate for the performance of the ITk strip system. The individual effects of the different safety factors are demonstrated in figure 10.

7.3. Results

The thermo-electrical model provides a large range of predictions for the operation of the strip system. A detailed discussion of all results would only be of interest to ITk strip system experts and is beyond the scope of this article. Instead we will present here a subset of results to demonstrate the capabilities and use of the thermo-electrical model for the design of the detector system.

³The correct module type, short-strip in the inner two layers and long-strip for the outer two layers, is used for each layer.

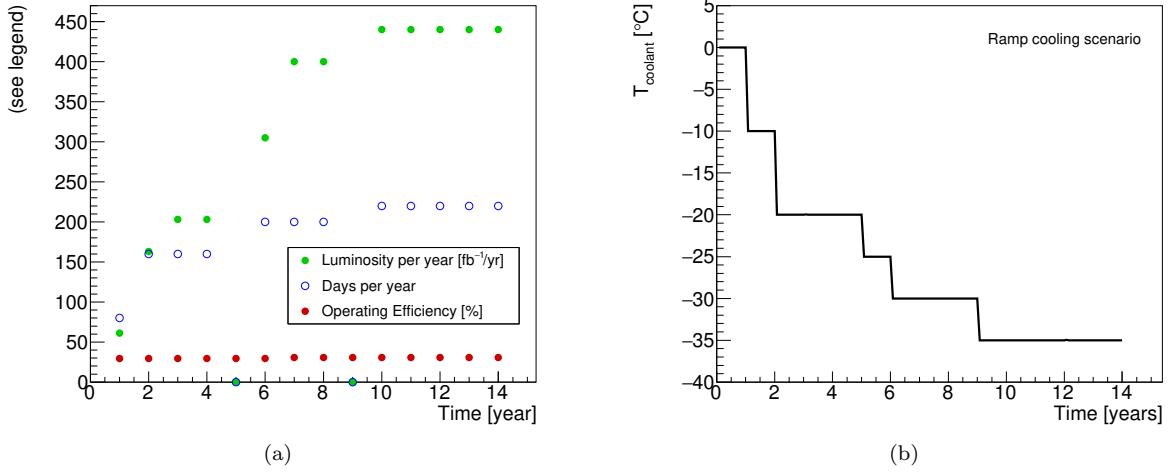


Figure 9: (a) Expected LHC performance and (b) ‘cooling ramp’ scenario for the coolant temperature. Year-long shutdowns of the LHC are anticipated in years 5 and 9.

Table 1: Safety factors.

Safety factor on	Value	Reason
Fluence	50%	Accuracy of fluence calculations and uncertainties in material distributions
Thermal impedance	10% endcap, 20% petal	Local support build tolerances, thermal network assumptions
Digital current	20%	Final chip performance and parametrization of TID effect
Analog current	5%	Final chip performance
Tape electrical impedance	10%	Electrical tape manufacturing tolerances
Bias voltage	700 V	Increased bias voltage from nominal 500 V to maintain S/N
TID parametrization	Nominal/Pessimistic	Different data sets for fit of TID bump

7.3.1. Module properties

Example output plots for module properties from the thermo-electrical modules are shown in Figures 11 and 12. The different radiation-dependent effects occur on different times scales. The maximum in the digital chip power due to the TID effect occurs relatively early (in year 1 to 4), although the bump has a long tail, particularly in the outer layers of the barrel. The sensor leakage power on the other hand grows towards the end of the lifetime of the ITk. If the leakage current would continue to increase in the case of further irradiation, or if the cooling temperature would be higher, this growth would ultimately lead to thermal runaway. Due to the radial dependence of the radiation environment, the radiation-induced effects are most pronounced in the innermost layers.

7.3.2. System properties

One of the key concerns for the design of the strip system is thermal stability of the system. If the cooling temperature is too high to limit the leakage power from the radiation-damaged sensors to a level where it can still be removed the system is unstable (it goes into ‘thermal runaway’). In this case there is no solution to the set of equations in the thermo-electrical model any more and the numerical search for a solution fails. In the barrel strip system this happens in the last year of operation at a cooling temperature of -15°C under nominal conditions, and at -25°C (in year 13) with safety factors applied. As the design cooling temperature of the ITk cooling system is -35°C we have confidence that the ITk strip system has sufficient margin for thermal stability.

Beyond the issue of stability, the thermo-electrical model delivers predictions for the development of

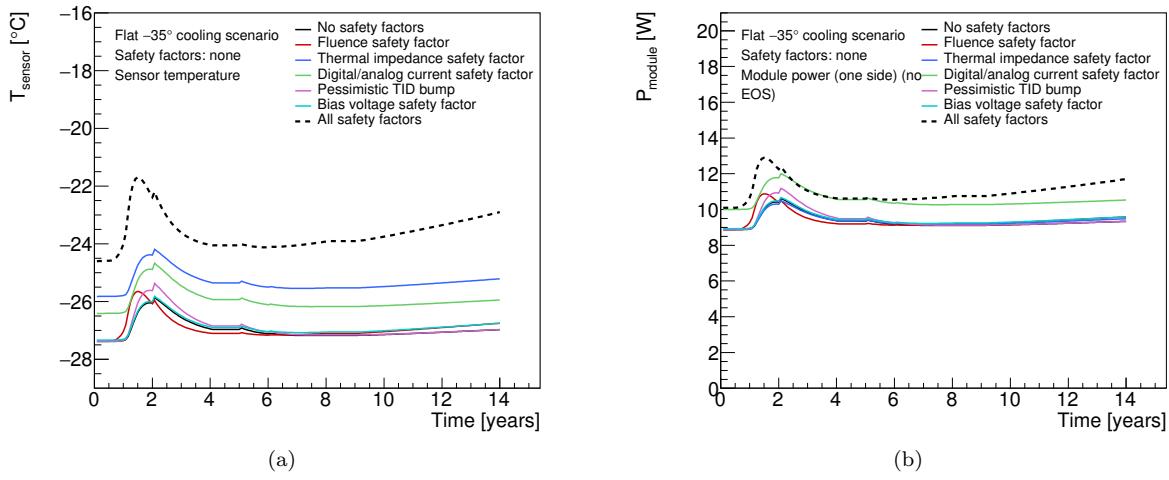


Figure 10: Comparing the impact of different safety factors on (a) the sensor temperature and (b) the module power for the R3 endcap module. The dotted line depicts the effect of all safety factors applied at once.

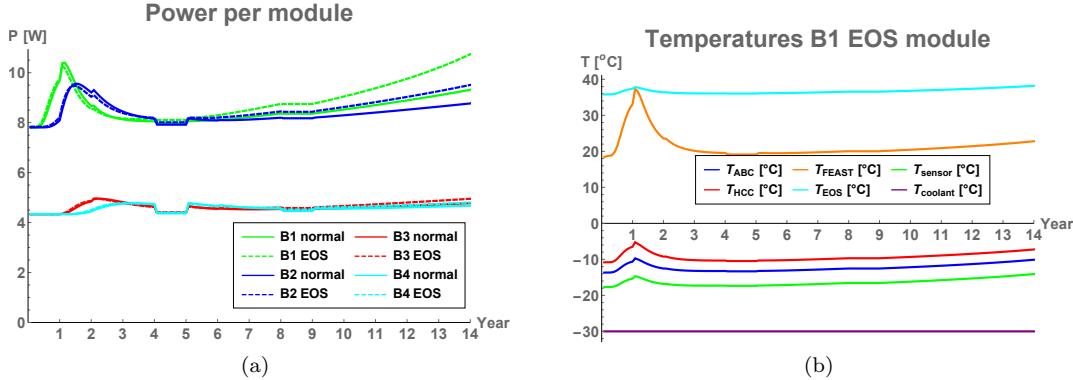


Figure 11: Examples of barrel module performance predictions for a flat cooling scenario (-30°) including safety factors. (a) Power per module. (b) Temperatures for different nodes of an end-of-stave barrel module in the innermost barrel.

current and power requirements for the overall system. Some of the predictions are shown in figure 13. Again, the different timescales of the various radiation-induced effects are visible. Ignoring this time dependence could lead to overspecification of some system aspects like the total cooling power.

These predictions are now used throughout the strip project to consistently size power supply and cooling systems. Including safety factors in the predictions gives us some confidence that the designs are robust and by using commonly agreed safety factors we ensure a consistent use of safety factors throughout the project and prevent safety factor creep.

Because of the different timescales for the peak power due to the TID effect and the sensor leakage due to radiation there is room for the optimization of the cooling temperature profile for minimal power. The thermo-electrical model is a powerful tool to plan such an optimized cooling profile. In fact, the cooling ‘ramp’ scenario introduced in Section 7.1 is the result of such an optimization (Fig. 14).

8. Model performance verification

The quality of the predictions of the thermo-electrical model is affected by two major factors: First, there is the quality of the input parameters, and second there are errors introduced by reducing the complex 3D geometry into a linear thermal impedance network. The former have been discussed throughout this paper

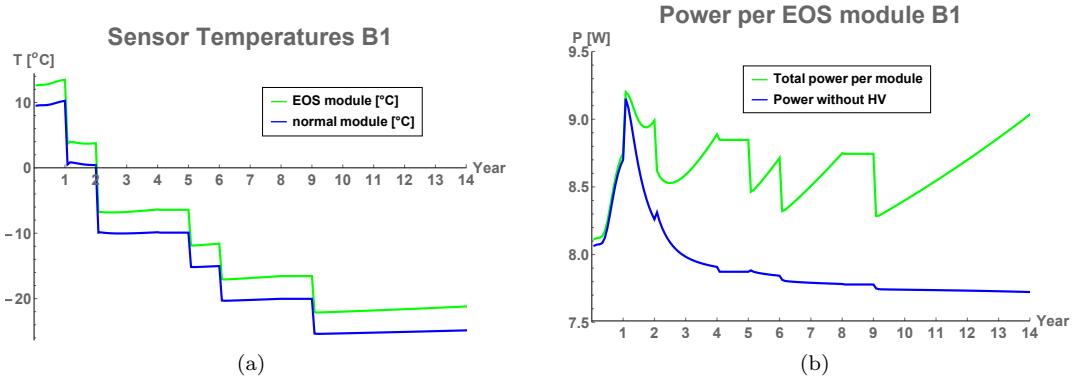


Figure 12: Examples of barrel module performance predictions for the ramp cooling scenario including safety factors. (a) Sensor temperature in the innermost barrel modules. (b) Power in an end-of-stave barrel module in the innermost layer.

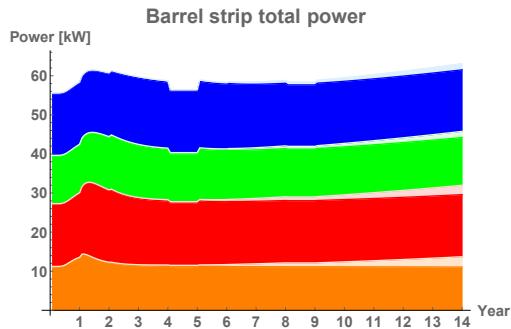


Figure 13: Examples for system performance predictions. Barrel total power requirements for flat -30° cooling including safety factors (left): The plot shows the stacked power requirements for the four barrels (orange: innermost barrel, blue: outermost barrel). Full colour indicates power from the front-end electronics, greyed parts are contributions from HV power for the four barrels.

where the different inputs have been presented. For the latter we have studied the agreement of predictions from the network model with the more accurate results obtained from FEA for selected states of the system.

For the verification of this agreement we have calculated the sensor temperature curve for a barrel end-of-stave module up to thermal runaway. For this we do not vary any of the input parameters in the model other than the sensor leakage power. We therefore can reduce the complex thermal network to its Thevenin equivalent, which is identical to the network studied in Ref. [3] and we can use the analytical expressions given there. The comparison of this prediction is shown in Fig. 15. Despite a large temperature variation of about 15°C across the sensor, which is caused by heat flux from the end-of-structure card and degraded thermal impedance at the end of the stave due to ceramic sections in the cooling pipe, the network model predicts the runaway within 1°C of the result from the FEA⁴. This agreement gives us confidence that the use of a thermal network model is not likely to significantly degrade the predictions beyond the errors introduced by other inputs to the model.

⁴Ref. [3] is not clear about the exact definition of the sensor temperature to be used for the calculation of the thermal impedance. In fact, at the time we were still using the maximum sensor temperature for this. Since then we have acquired more experience with thermal network models and found that the best agreement can be achieved if the average sensor temperature is used.

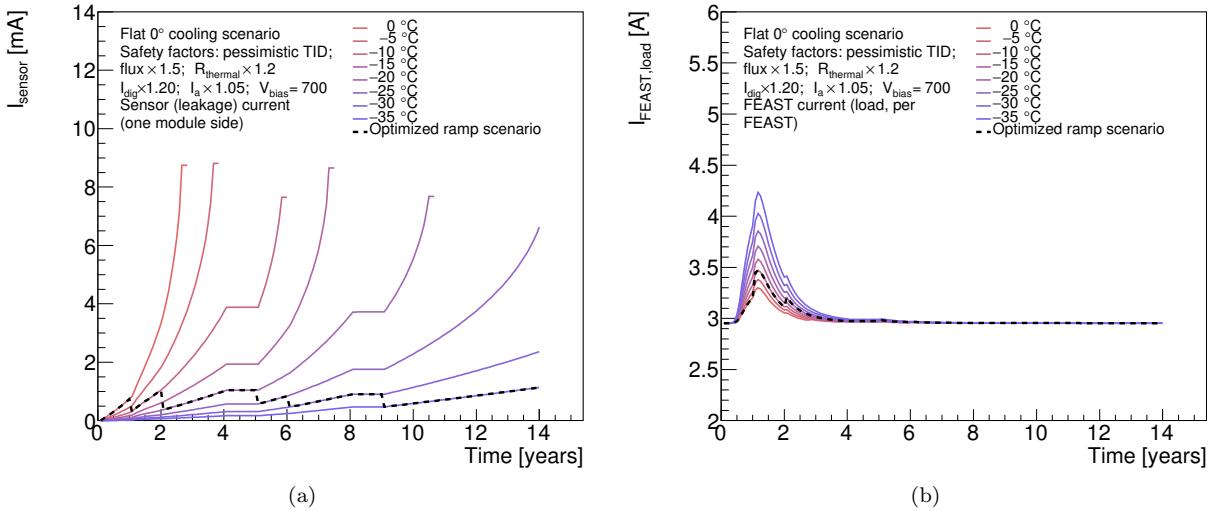


Figure 14: Performance of the cooling ‘ramp’ scenario specified in Fig. 9b. The dashed lines represent the ramp scenario, which has been selected so that the sensor leakage current (a) is stable throughout the lifetime of the ITk. A higher coolant temperature in the first few years reduces the TID effect, keeping the current load on the FEAST (b) well below its specified maximum of 4 A.

9. Conclusions

We have developed a model of the ATLAS ITk strip system which is based on the interplay between a thermal and an electrical network model. The set of equations in the model can be numerically solved using standard data analysis software in short time, allowing for a quick turn-around for systematic studies of the system performance. The complexity of these networks is given by the number of interconnected components between the networks which have a non-linear dependence on the temperature or electrical power. This approach could easily be adopted for any other silicon detector system.

In the case of the ATLAS strip system several temperature-dependent heat sources had to be included. In addition to the sensor leakage current these are the radiation-induced increase of the digital front-end power (‘TID bump’) and the efficiency of the DC/DC conversion system. The outputs of the model give us confidence that the ITk strip system will be thermally stable until the end of LHC phase II operation even if safety factors on key inputs are included. The model furthermore provides information for benchmark system parameters like cooling and supply power and currents in power cables, which is used in the specification of these systems. The use of the model outputs throughout the strip project ensures consistent specifications, including a common strategy on safety factors. Using the thermo-electrical model we can also propose an optimized cooling temperature ‘ramp’ scenario, which equalizes leakage power throughout the lifetime of the experiment while minimizing the TID bump.

We have verified the performance of the thermal network model compared to full FEA and are confident that the agreement is sufficient that the overall accuracy of the model is dominated by other inputs to the model, of which the most likely source of unknown error are limitations in the parametrization of the TID effect available for the model.

10. Acknowledgements

The evaluation of the termo-electrical model depends critically on the input parameters to the model. To capture the whole of the system these need to distill all what is known of the system, and we are therefore indebted to the whole of the ITk strip community. In particular we would like to thank Tony Affolder, Kyle Cormier, Ian Dawson, Sergio Diez Cornell, Laura Gonella, Ashley Greenall, Alex Grillo, Paul Keener, Steve McMahon, Paul Miyagawa, Craig Sawyer, Francis Ward and Tony Weidberg for all their inputs to this work.

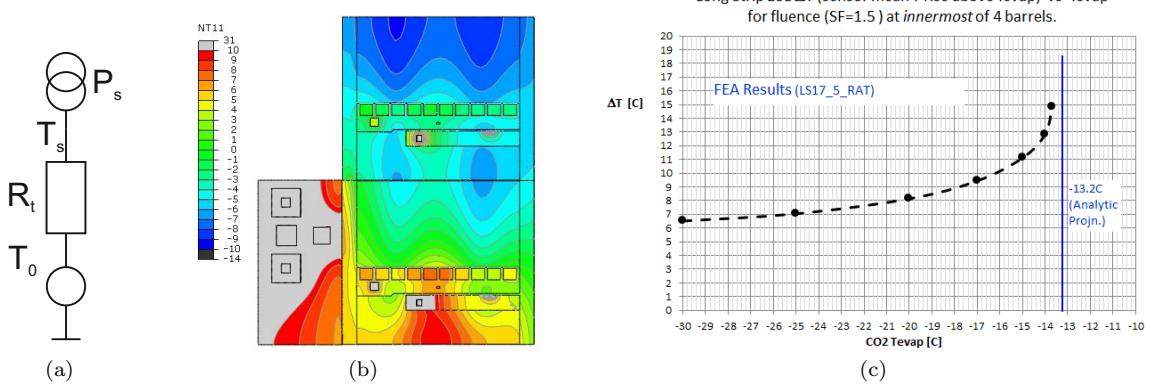


Figure 15: (a) Thevenin equivalent of the thermal network. (b) Result of surface temperature calculations using FEA. (c) Average temperature above cooling, comparing FEA (dots) and the network model prediction (dotted line).

References

- [1] ATLAS Collaboration, Technical Design Report for the ATLAS Inner Tracker Strip Detector.
- [2] Radiation induced effects in the ATLAS Insertable B-Layer readout chip, Tech. Rep. ATL-INDET-PUB-2017-001, CERN, Geneva (Nov 2017).
URL <https://cds.cern.ch/record/2291800>
- [3] G. Beck, G. Viehhauser, Analytic model of thermal runaway in silicon detectors, Nucl. Instrum. Meth. A618 (2010) 131–138. doi:[10.1016/j.nima.2010.02.264](https://doi.org/10.1016/j.nima.2010.02.264).
- [4] F. Faccio, G. Cervelli, Radiation-induced edge effects in deep submicron cmos transistors, IEEE Transactions on Nuclear Science 52 (6) (2005) 2413–2420. doi:[10.1109/TNS.2005.860698](https://doi.org/10.1109/TNS.2005.860698).
- [5] F. Faccio, H. J. Barnaby, X. J. Chen, D. M. Fleetwood, L. Gonella, M. McLain, R. D. Schrimpf, Total ionizing dose effects in shallow trench isolation oxides, Microelectronics Reliability 48 (7) (2008) 1000 – 1007, 2007 Reliability of Compound Semiconductors (ROCS) Workshop. doi:<https://doi.org/10.1016/j.microrel.2008.04.004>.
URL <http://www.sciencedirect.com/science/article/pii/S0026271408000826>