

Thermo-electrical modelling of the ATLAS ITk Strip Detector

Graham Beck^a, Kurt Brendlinger^b, Yu-Heng Chen^b, Georg Viehhauser^c

^a*Queen Mary University of London, Mile End Road, London E1 4NS, UK*

^b*Deutsches Elektronen-Synchrotron DESY, Notkestraße 85, 22607 Hamburg*

^c*University of Oxford, Keble Rd, Oxford OX1 3RH, UK*

Abstract

In this paper we discuss the use of linked thermal and electrical network models to predict the behaviour of a complex silicon detector system. We use the silicon strip detector for the ATLAS Phase-II upgrade to demonstrate the application of such a model and its performance. With this example, a thermo-electrical model is used to test design choices, validate specifications, predict key operational parameters such as cooling system requirements, and optimize operational aspects like the temperature profile over the lifetime of the experiment. The model can reveal insights into the interplay of conditions and components in the silicon module, and it is a valuable tool for estimating the headroom to thermal runaway, all with very moderate computational effort.

Keywords: Silicon detector, Thermal runaway, Thermal management, Cooling

1. Introduction

The temperatures in silicon detector systems are critically important to their performance. Fundamentally, the leakage current of a silicon sensor has a pronounced temperature dependence

$$I \propto T_S^2 e^{-T_A/T_S}, \quad (1)$$

where T_S is the sensor temperature and $T_A \simeq 7000$ K [1]. Leakage currents in the silicon sensor can become particularly significant after irradiation, and the heat generated by these leakage currents, together with the heat from front-end electronic components on the detector, needs to be removed by a cooling system. The capability of the cooling system to remove this heat is limited by the temperature of the local cold sink (typically a circulated fluid) and the thermal impedance of the heat path between the source (electronics and sensor) and the sink. Due to the strong growth of leakage power with temperature, there is a critical temperature T_{crit} above which the heat cannot be removed quickly enough, and the detector becomes thermally unstable ('thermal runaway')¹. Understanding the thermal behaviour and the headroom to thermal runaway is crucial for the design of a silicon detector system. Even before the limit of thermal stability is reached, temperatures in silicon detector systems have a major impact on key system parameters such as power supply capacity and cable dimensions, necessitating an accurate estimate.

In addition to the silicon, there can be aspects of the front-end electronics that have a temperature dependence. In the strip system for the ATLAS Phase-II upgrade [2], which is the subject of this case study, there are two additional temperature-dependent heat sources. The first is a radiation damage effect in the readout electronics, which leads to an increase in the digital power of the chip whose magnitude depends on the total ionisation dose (TID) and the temperature of the chip [2]. This phenomenon was first observed in the ATLAS IBL [3]. The other temperature dependence of a power source stems from the converter chip (FEAST [4]) used in the on-detector DC-DC converter system supplying power to the front-end electronics. The FEAST chip has an efficiency that decreases at higher temperatures; its efficiency also depends on the magnitude of the load current.

¹In a real detector system, the resulting growth of sensor temperature would be arrested by overcurrent limits in the power supplies, resulting in a reduction of the bias voltage. At the same time, the increased current leads to an increase of the noise, such that the overall result is a degradation of the S/N performance of the system.

In principle, the temperatures in the system for a given set of operational parameters (power density, thermal conductivities, etc.) can be predicted using finite element analysis (FEA) to an accuracy that is limited only by the quality of the input parameters. However, this is a time-consuming process and can be prohibitively difficult if a number of local heat sources depend non-linearly on temperature. A simplification to this problem that allows for an analytical solution in the case of a simple heat source topology has been developed in [5]. Here we develop this method further to include several temperature-dependent non-linear heat sources in the front-end electronics. The resulting set of equations cannot be solved analytically anymore, but the solution can be found with little effort using numerical problem solvers. This enables us to predict with some confidence the temperatures and power requirements in the ATLAS strip system throughout Phase-II operation. The results from this prediction have been used throughout the ATLAS strip project to consistently dimension the different systems (cooling, power, services, etc.), including an appropriate margin due to the inclusion of a common set of safety factors. This method can be easily adapted to any other system by adjusting the model to the system-specific geometries and parameters.

1.1. The ATLAS strip system

The strip system for the ATLAS Phase-II upgrade consists of two parts: the barrel system, comprised of four concentric cylindrical barrels, and two endcaps consisting of six disks each.

In the barrel, the detector modules are made of square sensors ($96.85 \times 96.72 \text{ mm}^2$) with hybrids on top, which host the front-end chips (ABC130 [6] and HCC [2]) as well as circuitry to convert the supply voltage of larger than 10 V to the chip voltage of 1.5 V, controlled by the FEAST chip. The modules are glued onto both sides of a composite sandwich (local support) that contains two parallel thin-wall titanium cooling pipes embedded in carbon foam (Allcomp K9) between two facesheets of ultra-high-modulus carbon fibre (3 layers of K13C2U/EX1515) co-cured together with a Kapton/copper low-mass tape. A model of this geometry is shown in Fig. 1. During final operation, cooling will be achieved by evaporating CO₂ in the cooling pipes with a final target temperature no higher than -35°C anywhere along the stave.

The geometry of the stave is uniform along its length, with the exception of the end region of the stave, where an End-Of-Substructure (EOS) card is mounted on both surfaces. The EOS card shares part of its heat path with the adjacent module; underneath this module (hereafter referred to as an ‘EOS module’), the thermal path is degraded by the presence of electrically-insulating ceramic pipe sections. The thermal and electrical properties of an EOS module are sufficiently different from other modules along the length of the stave (‘normal modules’) to warrant separate treatment in the thermo-electrical model of the barrel.

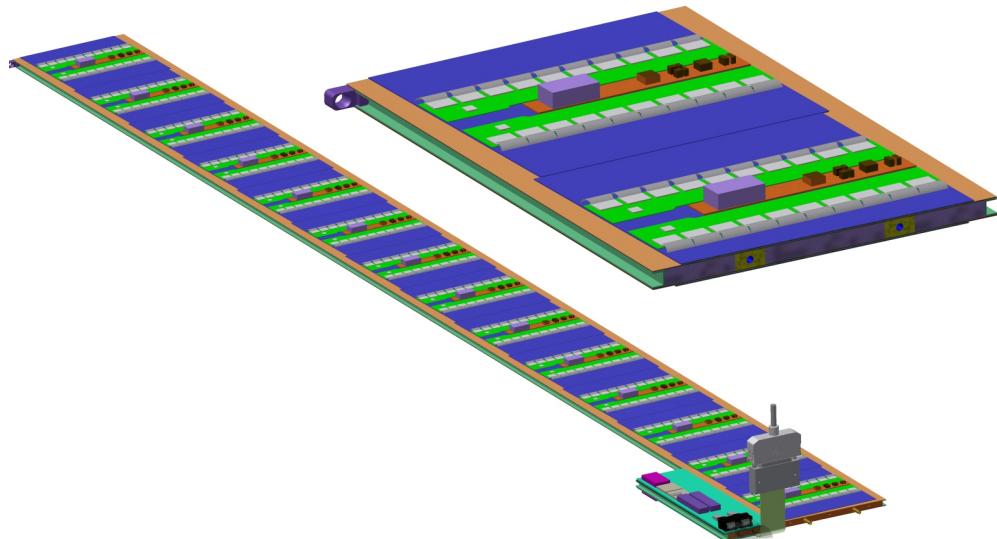


Figure 1: Strip barrel local support geometry. On the left, a complete stave is shown (EOS card in the foreground). The right picture shows a cross-section of the stave with the two cooling pipes visible inside the core.

61 The endcap system consists of two endcaps composed of 6 disks each. Each disk contains 32 ‘petals,’
 62 the local substructure depicted in Fig. 2. Both sides of the petal are loaded with 6 silicon modules, each
 63 with a distinct design, located at increasing radius from the beam pipe and labeled R0 through R5 (where
 64 ‘R’ stands for ring). Each endcap module consists of one or two wedge-shaped silicon sensors and a varying
 65 number of front-end chips and DC-DC converters. The EOS card is located adjacent to the R5 module, but
 66 the cooling pipes run directly underneath it without a shared heat path, in contrast to the barrel EOS card.
 67 The remaining module and petal core design details are largely identical to the barrel module description
 68 above. Because of the unique geometry of each module in a petal, each of the six different types of module
 69 is modelled separately in the thermo-electrical model.

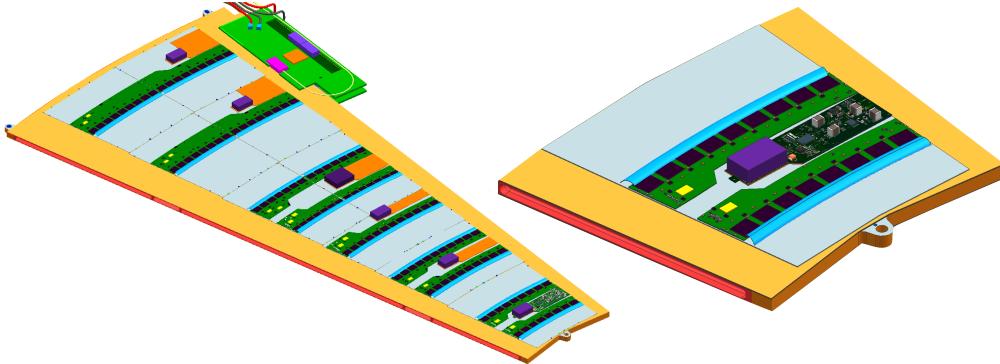


Figure 2: The geometry of the endcap strip petal, featuring 6 distinct module designs. A close-up of the R0 module is shown on the right.

70 1.2. Radiation environment

71 A key input to the thermo-electrical calculation is the radiation environment of the strip system, as several
 72 inputs depend on radiation damage effects. The sensor leakage current can be parametrized as a function
 73 of the fluence expressed in 1 MeV neutron-equivalents, and the TID effect on the digital chip current will
 74 be described as a function of the total ionizing dose rate (more details on its dependencies can be found in
 75 Section 7).

76 Predictions for both of these quantities have been generated for each point in the ITk using the FLUKA
 77 particle transport code and the PYTHIA8 event generator (Fig. 3) [7]. In the barrel system, both of these
 78 distributions display a strong dependence on r but a weak z -dependence. Accordingly, we make the simplifying
 79 assumption that modules within the same barrel layer have identical fluence and TID, and model four
 80 different radiation profiles (one for each barrel layer). In the endcaps, the radiation levels vary significantly
 81 over the length of the petals and from disk to disk; therefore, we model each disk and ring position separately
 82 (36 in total).

83 2. The electrical model

84 The electrical model consists of low-voltage (LV) and high-voltage (HV) circuits, depicted in Fig. 4. The
 85 LV current (supplied at 11 V) is used to power the hybrid controller chips (HCCs), ATLAS Binary Chips
 86 (ABCs) and Autonomous Monitoring and Control chip (AMAC) located on PCBs that are glued directly onto
 87 the surface of the sensor. These chips require between 1.5 and 3.3 V, which are provided by the temperature-
 88 dependent FEAST DC-DC converter (labeled bPOL12V in Fig. 4) and an LDO (low-dropout) regulator
 89 (labeled bPOL12). The number of chips and converters on each module vary according to the design of each
 90 different module type (barrel short-strip and long-strip modules, and six different endcap module designs).
 91 A barrel or endcap module contains 10–28 ABC chips, 1–4 HCCs, and 1–2 of each of the other components
 92 (linPOL12V/bPOL12V/AMAC).

93 The LV current is also delivered to the EOS card to power various data transfer components: the Gigabit
 94 Laser Driver (GBLD), low power GigaBit Transceiver (LpGBT) and Gigabit Trans-impedance Amplifier
 95 (GBTIA) chips. A FEAST identical to the one used on the module is used to step the voltage down from

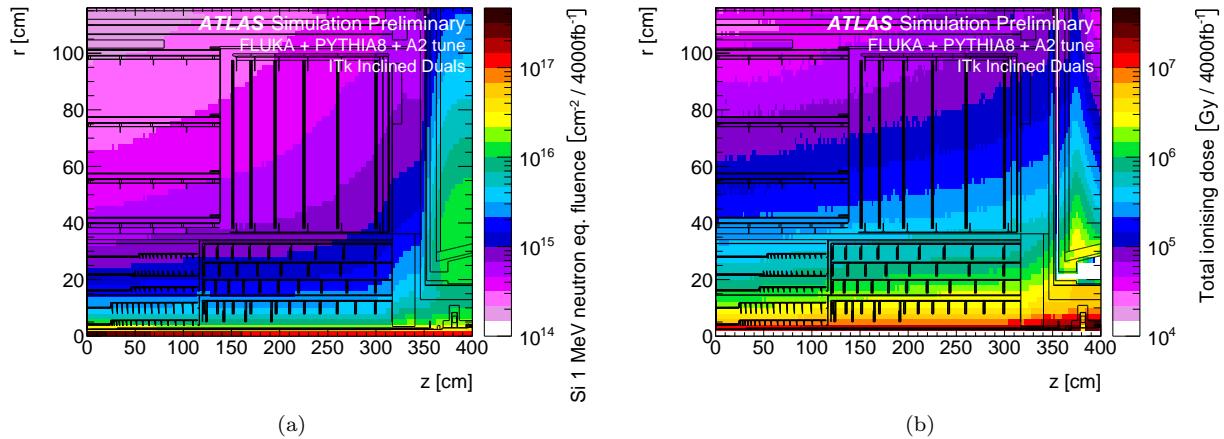


Figure 3: The ATLAS ITk radiation environment. (a) 1 MeV neutron equivalent fluence and (b) total ionizing dose. Both plots are for an integrated luminosity of 4000 fb^{-1} [7].

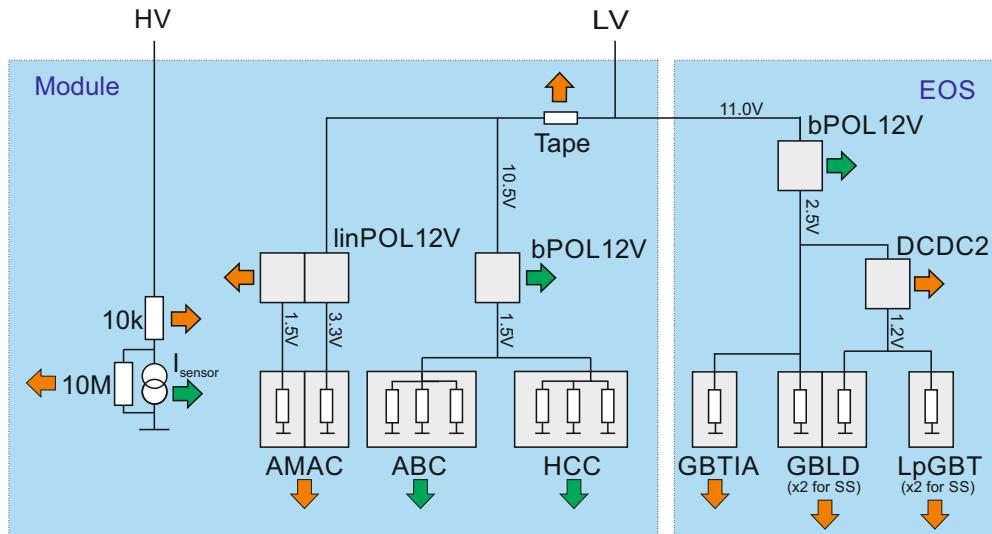


Figure 4: The electrical model of the ITk Strip barrel and endcap modules. Green arrows represent temperature-dependent heat sources, while orange arrows are temperature-independent. Grey squares are chips.

96 11 V to 2.5 V, and an additional LDO regulator brings the voltage down further for some components. The
97 short-strip barrel staves contain two GBLD and LpGBT chips.

The bus tape, which carries both LV and HV currents, has a small ohmic resistance, which impacts the module in two ways. First, the tape itself will generate some heat according to the amount of current passing through it; this source of heat is accounted for in the model, however the contribution to the total module power is negligible. Second, due to the voltage loss along the traces, there is a slight reduction in voltage supplied to successive modules along the substructure. The treatment of this effect is slightly different in the barrel and endcap models: in the barrel, the voltage delivered to every module is averaged to 10.5 V; in the endcap, the ΔV is estimated based on the calculated expected power loss along the tape for each module. In both cases, the impact of using a different treatment is small.

Finally, the HV current provides the bias voltage on the silicon sensors. An HV multiplexer switch (HVMUX) can be used to disconnect the sensor from the bias line (it requires a $10\text{ M}\Omega$ resistor parallel to the sensor in order to function). Two HV filters with an effective resistance of $10\text{ k}\Omega$ are situated in series

109 with the sensor. The nominal operating voltage of the sensor is expected to be 500V, but the system is
 110 designed to handle a bias voltage of up to 700V.

111 **3. The thermal model**

112 The thermal network consists of heat sources (some of which are temperature-dependent) and thermal
 113 resistances. The latter are given by the properties of the mechanical design (heat conductivities of the
 114 materials) and the geometry of the heat path. The geometry is generally 3-dimensional, but it is the strategy
 115 of the simple network models to lump the 3D behaviour into one thermal resistance parameter. In the models
 116 discussed here, we have used a granularity corresponding to single detector modules for which the thermal
 117 resistance has been modelled. The temperatures in the model are then given for the nodes in the network in
 118 analogy to the potentials in an electrical network.

119 The complexity of the thermal network used in this study, depicted in Fig. 5, is given by the variety of
 120 temperature-dependent heat sources in the ATLAS strip system: the digital power for each type of chip, the
 121 FEAST chip providing the on-detector DC-DC conversion, and the sensor leakage power. In the ATLAS
 122 ITk strip modules, all of these components are located on top of the sensors, such that the heat generated
 123 in them flows through the sensor into the support structure, the stave (barrel) or petal (endcap) core with
 124 the embedded cooling pipe. In the network model, the heat flow from these sources combines and travels
 125 through a common impedance R_M to the sink at a temperature T_C . For each of the temperature-dependent
 126 heat sources (ABC, HCC, FEAST and the sensor) we have added a resistance from the common temperature
 127 T_{mod} to allow for a finite and different heat path for each of them. Finally, the EOS card adjacent to the last
 128 module on the barrel stave or endcap petal is modeled as an additional source of heat with an independent
 129 impedance for its unique thermal path.

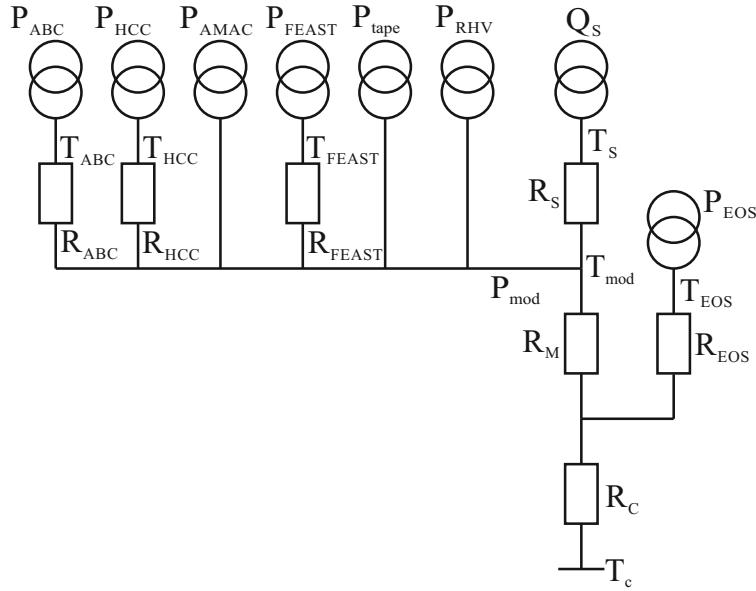


Figure 5: Thermal network model.

130 This is a more complex thermal network than the one studied in Ref. [5], for which an analytical solution
 131 for the determination of thermal stability is given. In particular, because of the non-linear temperature
 132 dependence of some of the heat sources, it is not possible in the present case to solve the set of equations
 133 describing the model analytically. However, the set of equations is still sufficiently small to solve numerically
 134 using functional programming languages such as Mathematica (used in the barrel model) or Python (used
 135 in the endcap system).

¹³⁶ 4. Obtaining thermal impedances using FEA

¹³⁷ The cooling path between the sources dissipating electrical power and the cooling fluid is 3-dimensional
¹³⁸ and includes components with orthotropic thermal conductivity. Hence the prediction of temperature at any
¹³⁹ node of the model requires a 3D thermal FEA [8, 9]. However, the thermal conductivities of the components
¹⁴⁰ along the path are approximately constant, so that the temperature rise ΔT_i above the coolant temperature
¹⁴¹ of any node i ($i = \text{ABC, HCC, AMAC, FEAST, tape, RHV, or sensor}$) in the thermal network model is
¹⁴² adequately described by a linear sum of contributions from individual sources, i.e:

$$\Delta T_i \equiv T_i - T_C = R_i P_i + (R_C + R_M) \sum_j P_j, \quad (2)$$

¹⁴³ where the index j runs over all powered nodes. (We have momentarily ignored the contribution from the
¹⁴⁴ EOS card.)

¹⁴⁵ In order to extract the thermal impedances for the thermal network model, the finite element model is run
¹⁴⁶ multiple times, with each heat source (or group of similar sources) switched on in turn with a representative
¹⁴⁷ amount of heat. In each of these cases, the temperature is calculated for all nodes in the thermal network
¹⁴⁸ model (Fig. 5). The temperature of a node is here taken as the average of the temperatures for all the
¹⁴⁹ grid points in the FEA model within the volume of the object corresponding to the node². The thermal
¹⁵⁰ impedances are then obtained from a fit of Eq. 2 using the temperature data for all nodes for all cases of
¹⁵¹ heat injection.

¹⁵² Because of the nature of the network, the fitted value for the common impedance $R_{CM} = R_C + R_M$ is
¹⁵³ determined by the observed temperature rises of components where no heat is injected. The linearity of
¹⁵⁴ this relationship is illustrated in Fig. 6. The value of each component-specific impedance is determined from
¹⁵⁵ the temperature rise observed when heat is injected into that component. The linear approximation of the
¹⁵⁶ model reasonably describes the FEA simulation, and the level of disagreement, discussed below, is taken as
¹⁵⁷ an uncertainty that is assessed as a safety factor as described in Section 7.2.

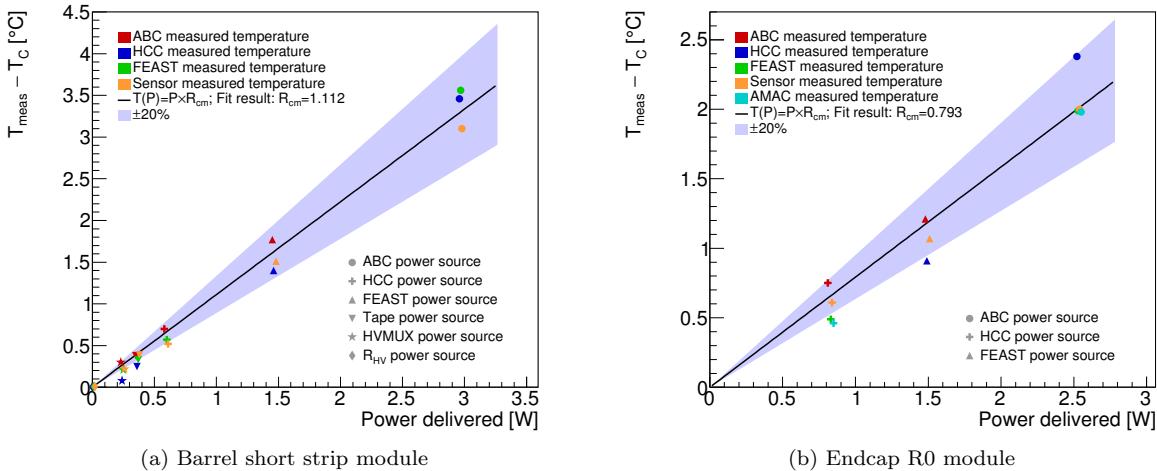


Figure 6: The relationship between the temperature rise observed in the FEA for a specific component and the heat injected in another component. The slope of the fitted line is the estimate for R_{CM} . (a) The fit for a short-strip barrel module adjacent to the EOS card. (b) The fit for the endcap R0 module. For each data point marker, the source of power is indicated by the shape, and the measured component is indicated by the color. The blue band represents a $\pm 20\%$ error band on the fit for R_{CM} .

²This is particularly interesting in the case of the sensor, which fills a large volume, with a potentially large range of temperatures. In Ref. [5] the analytic model parameters were extracted from the maximum sensor temperature predicted by FEA, whereas our subsequent studies have shown that the thermal stability limit is predicted more accurately if the average sensor temperature is used.

158 For a barrel module, the agreement of the network temperatures using the thermal impedances from the
159 fit with the data from FEA is better than 0.5°C for all nodes. This procedure is performed for both an EOS
160 module and a normal module. The thermal impedance from the sensor to the sink (R_{CM}) is consistently
161 between 1.1 and $1.4^{\circ}\text{C}/\text{W}$, but higher values (between 10 and $20^{\circ}\text{C}/\text{W}$) are found for other impedances in the
162 network (R_{HCC} and R_{FEAST}), mostly because these are for components with a small footprint constituting a
163 bottleneck for the heat flow. A 10% uncertainty is assigned to the thermal impedances in the barrel modules
164 for the purposes of assessing safety factors.

165 For the endcap modules, the procedure to determine the thermal impedances is performed for each of the
166 6 module types. R_{CM} ranges from 0.6 to $1.4^{\circ}\text{C}/\text{W}$, with other nodes between 5 and $20^{\circ}\text{C}/\text{W}$. Because the
167 location of powered components is more irregular on an endcap module, the difference between the predicted
168 temperatures of the linear network and the FEA can reach up to 1.2°C for key temperature-dependent
169 nodes. Therefore, a 20% uncertainty is assigned to the thermal impedances in the endcap modules.

170 There are two recognised departures from linearity of the thermal path: the rise in thermal conductivity
171 of the silicon sensor with decreasing temperature, and the rise in heat transfer coefficient (HTC) of the
172 evaporating CO_2 coolant with increasing thermal flux. The FEA models are run using mean values for these
173 quantities appropriate to the operating conditions, and the thermo-electrical model results are insensitive to
174 the variations expected in practice. However, if this level of realism is required and if reliable parametrizations
175 for these dependencies can be obtained, then the inclusion of such variations in the model is possible.

176 5. Other model inputs

177 The three temperature-dependent elements of the thermo-electrical model—the radiation-induced digital
178 current increase in the front-end chips, the efficiency of the FEAST-controlled DC-DC converter, and the
179 sensor leakage current—are described in this section. Each effect is studied experimentally and fit with
180 functional forms in order to accurately represent them in the model. The uncertainty in the experimental
181 data, and in our modelling assumptions, are estimated here and considered in the evaluation of safety factors,
182 described in detail in Section 7.2.

183 5.1. DC-DC converter

184 The DC-DC converter, controlled by the FEAST chip, supplies a low-voltage (1.5 V) current to the
185 ABC130 and HCC front-end chips on the module. The efficiency of the FEAST depends on its temperature
186 as well as the output (load) current load delivered to the front-end chips. To correctly model the FEAST
187 efficiency, experimental measurements have been performed to characterize the dependence and fitted with
188 a functional form.

189 For the measurement, the FEAST power board was glued to an aluminum cold plate, cooled with CO_2 , and
190 powered with the nominal working input and output voltages (11 V input, 1.5 V output). The temperature
191 of the FEAST was measured with an NTC (negative temperature coefficient) thermistor and a PTAT (point
192 to absolute temperature) sensor residing on the FEAST for a range of load currents up to the maximum
193 design current of 4A.

194 The data was then fit with a function with sufficient parameters to ensure reasonable agreement; the
195 choice of functional form has no physical interpretation. Fig. 7 depicts the FEAST efficiency data and the
196 parametrized fit used in the model. The parametrization fits the data with an accuracy better than 1% ;
197 this uncertainty in the FEAST efficiency modelling is small compared to other uncertainty sources, and is
198 therefore neglected in our model.

199 5.2. Digital current increase of chips using 130 nm CMOS technology

200 The ABC and HCC chips, designed using IBM 130 nm CMOS 8RF technology, are known to suffer from
201 an increase in digital current when subjected to a high-radiation environment [2]. This phenomenon, known
202 as the “TID bump,” is well-studied [10, 11] and has a characteristic shape whereby the effect reaches a
203 maximum as a function of the accumulated dose and then gradually diminishes (see Fig. 8).

204 In an effort to characterize the nature of the TID bump in the ABC and HCC chips empirically, many
205 irradiation campaigns have been conducted using a variety of radiation sources, testing the effect at different
206 temperatures and dose rates. The data collected from these studies was used to develop a model of the
207 TID bump that estimates the digital current increase given the total ionizing dose, the dose rate, and the

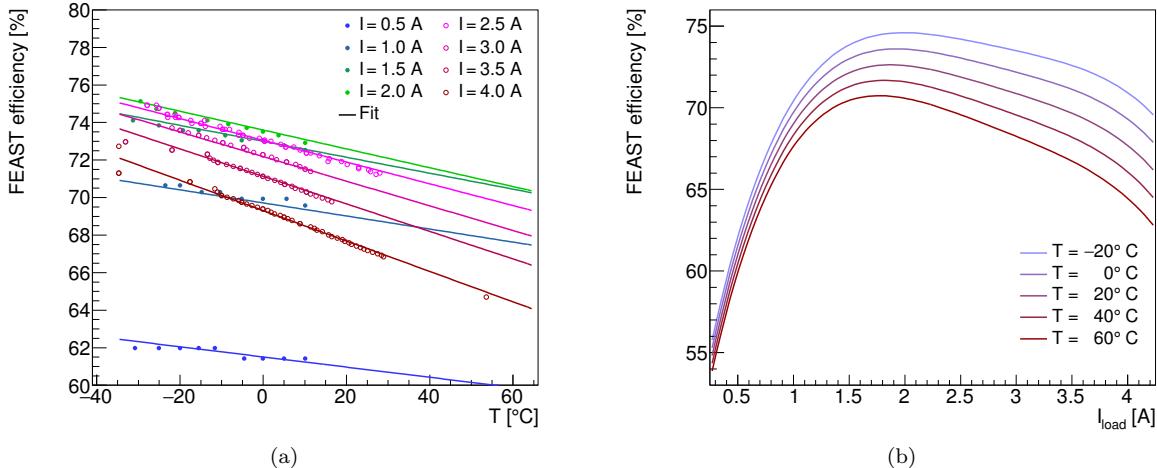


Figure 7: The FEAST efficiency model based on experimental data. (a) The experimental data points characterizing the FEAST efficiency are plotted as dots and color coded for load current. The data is compared to the analytic fit, evaluated in curves of equal current. (b) The same analytic fit, presented as a function of current load for curves of equal temperature.

208 operating temperature of the chip. This parametrization, which is depicted in Fig 8, is used as an input
 209 to the thermo-electrical model in order to correctly model the ABC and HCC currents. The TID bump is
 210 assumed to fully apply to the HCC digital current, and apply to 69% of the ABC digital current (according
 211 to our understanding of its digital circuitry).

212 The TID bump displays certain key features, which are reflected in the parametrization: first, the effect is
 213 larger at colder temperatures and higher dose rates. This means it can be mitigated by operating the chips at
 214 higher temperature (note that the dose rate is determined by the LHC operational conditions). Second, the
 215 figure illustrates how chips receiving different dose rates will reach their maximum digital current increase
 216 at different times. This feature is particularly important when modelling the total power consumed by the
 217 barrel and endcap systems. In both systems, the dose rate varies significantly depending on the position of
 218 the module in the detector. The effect means that the maximum system power will be smaller than the sum
 219 of the maximum power of each module, as each chip reaches its maximum at a different point in time.

220 The TID bump is an important source of uncertainty in our model. The experimental data exhibit a
 221 relatively large variation in the TID bump effect, in particular between different batches of the same type of
 222 chip delivered by the manufacturer, suggesting an unknown effect in the fabrication process. To estimate the
 223 uncertainty in the TID bump, the parametrized function is fit again using only the worst-performing data
 224 (defined as having the largest TID bump effect). This “pessimistic” parametrization is used as a safety factor
 225 to estimate the detector performance in worst-case scenarios.

226 The irradiation of individual chips have typically been performed at constant dose rate and temperature.
 227 However, both of these parameters will vary as a function of time in the scenarios that we attempt to model.
 228 In our current parametrization, we use only the instantaneous value of these two parameters, thus neglecting
 229 any possible history of the TID effect for a given chip. We also ignore any short-term effects due to variations
 230 in the dose rate on the scale of hours or days. This approach is mandated by the lack of more varied
 231 experimental data and the absence of a good theoretical model for this effect. This probably constitutes the
 232 largest source of uncertainty in our model.

233 5.3. Radiation-dependent leakage current

234 The radiation-induced sensor leakage current can be parametrized as a function of the hadron fluence
 235 expressed in 1 MeV equivalent neutrons. We have used linear parametrizations obtained from fits to ex-
 236 perimental data taken at 500 V and 700 V at -15 $^{\circ}$ C, and scale them to a given sensor temperature using
 237 Eq. 1.

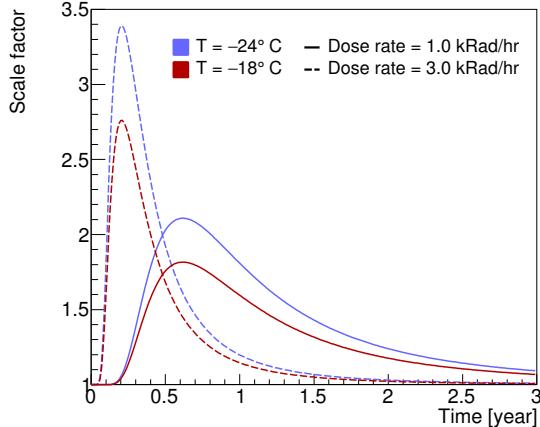


Figure 8: Parametrization of the impact of the total ionizing dose on the magnitude of the front-end chip digital current (the TID bump), presented as a function of time. The current is multiplied by a scale factor that is modeled as a function of total ionizing dose, dose rate, and temperature, based on experimental data.

238 6. Running the model

239 The thermo-electrical model constructs a profile of the sensor module operation conditions over the
 240 lifetime of the detector in the following manner. First, the total module power (including all components,
 241 but excluding the sensor leakage power) and the sensor temperature assuming no leakage current (T_0) are
 242 calculated using a reasonable set of initial component temperatures. The initial value for the module power is
 243 used to solve for the sensor power and temperature accounting for leakage current, using the thermal balance
 244 equation and the relationship from Eq. 1. Using this calculated sensor leakage current and temperature, the
 245 power and temperature of the module components are updated given the initial (year 0, month 0) startup
 246 parameters.

247 Next, the module conditions of the following month (year 0, month 1) are calculated. Using the compo-
 248 nent temperatures calculated from the previous month and the operational parameters (ionizing dose and
 249 dose rates) from the current month, the module total power (excluding sensor leakage) is again calculated,
 250 and subsequently the sensor temperature and leakage current are computed. Following this, the module
 251 component temperatures and power values are derived for this month. This process is repeated in one-month
 252 steps until the final year of operation, or until a real solution for the sensor temperature does not exist,
 253 indicating that thermal runaway conditions have been reached.

254 In the barrel subsystem, the above procedure is performed four separate times to represent the radiation
 255 conditions of the four barrel layers located at different radii from the beam axis³ for both a normal and an
 256 EOS-type module. Thus, eight modules are simulated in total for the barrel (4 layers \times normal/EOS), and
 257 they are combined in their proper proportion to simulate the entire barrel system.

258 In the endcap subsystem, the total ionizing dose and dose rates vary significantly depending on the
 259 position of the module; furthermore, the design of each module on a petal differs significantly. Therefore, all
 260 36 module types (6 rings \times 6 disks) are simulated independently, and combined to represent the full endcap.

261 We have implemented this algorithm in Mathematica (barrel) and Python (endcaps). In both cases, the
 262 calculation for a set of operating conditions over the full lifetime of the LHC takes between 5 and 10 minutes
 263 on a standard PC, thus enabling a quick turn-around for systematic studies of the parameter space.

264 7. Outputs of the thermo-electrical model

265 The thermo-electrical model provides a wide range of predictions for the operation of the strip system. A
 266 detailed discussion of all results is beyond the scope of this article; instead, we present here a subset of the

³The correct module type, short-strip in the inner two layers and long-strip for the outer two layers, is used for each layer.

267 results to demonstrate the capabilities and use of the thermo-electrical model for the design of the detector
 268 system.

269 7.1. Operational scenarios

270 To study the different aspects of our predictions for the operation of the ITk strip system throughout
 271 its lifetime, we performed the calculation of the system parameters over the expected 14 years of operation
 272 in monthly steps as outlined in Section 6. Time-dependent operational inputs to the calculation were taken
 273 from the expected performance of the HL-LHC (Fig. 9a). For the cooling temperature, which can be adjusted
 274 during data taking using detector control systems, we studied flat cooling profiles with temperatures as low
 275 as -35°C , the lowest evaporation temperature achievable with the ITk evaporative CO_2 cooling system, as
 276 well as a ‘ramp’ scenario in which the cooling temperature starts at 0°C and is gradually lowered down to
 277 -35°C over the course of 10 years (Fig. 9b).

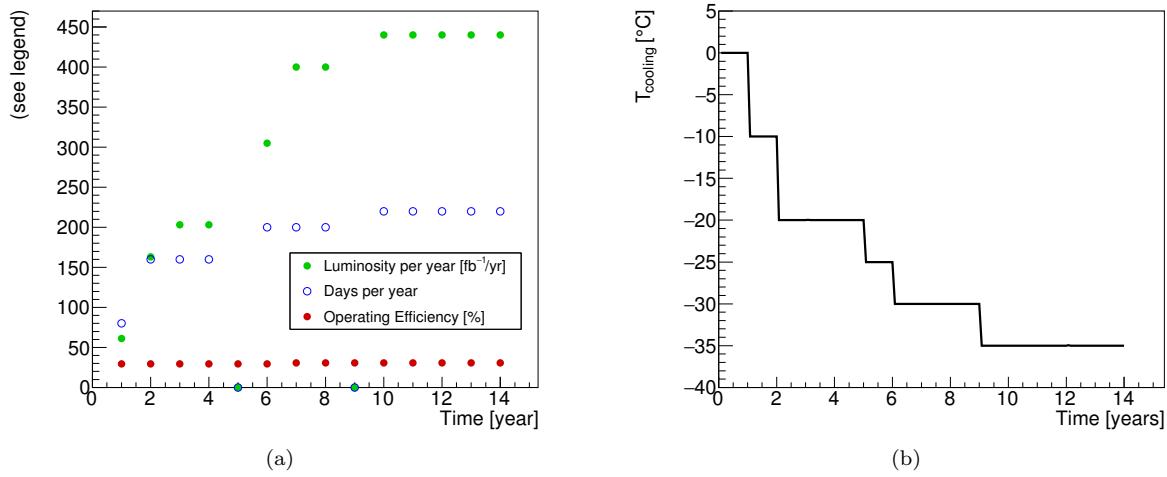


Figure 9: (a) Expected HL-LHC performance and (b) ‘cooling ramp’ scenario for the coolant temperature. Year-long shutdowns of the LHC are anticipated in years 5 and 9.

278 7.2. Safety factors

279 To ensure the robustness of the system design against uncertainties in the assumptions used in the model,
 280 we also evaluate the model using a set of input parameters with some key inputs degraded. The set of safety
 281 factors used is given in Table 1. Each safety factor has been estimated individually based on experience, the
 282 complexity of the system aspect described by the parameter, and from available data or the absence of such
 283 data. Note that the model can be evaluated with all the safety factors listed in Table 1 used together, a
 284 situation that is unlikely to occur in the real system, to provide a worst-case estimate for the performance of
 285 the ITk strip system. The individual effects of the different safety factors are demonstrated in Fig. 10.

286 It is important to note that combining multiple safety factors can have a compounding effect on the
 287 system. As an example, the effect of an increased bias voltage combined with a larger digital current will
 288 result in a much higher sensor leakage current at the detector end-of-life than either situation occurring
 289 individually. The analytical model presented here allows for scenarios like these to be examined quickly and
 290 effectively.

291 7.3. Module properties

292 Several module properties predicted by the thermo-electrical model are shown in Figs. 11 and 12 for
 293 the barrel system. The different radiation-dependent effects occur on different timescales. The maximum
 294 in the digital chip power due to the TID effect occurs relatively early (in year 1 to 4), although the bump
 295 has a long tail, particularly in the outer layers of the barrel. The sensor leakage power, on the other hand,
 296 grows towards the end of the lifetime of the ITk. If the leakage current continued to increase in the case of

Table 1: Safety factors.

Safety factor	Value	Reason
Fluence	50%	Accuracy of fluence calculations and uncertainties in material distributions
Thermal impedance	10% barrel, 20% endcap	Local support build tolerances, thermal network assumptions
Digital current	20%	Final chip performance and parametrization of TID effect
Analog current	5%	Final chip performance
Tape electrical impedance	10%	Electrical tape manufacturing tolerances
Bias voltage	700 V	Increased bias voltage from nominal 500 V to maintain S/N
TID parametrization	Nominal/Pessimistic	Different data sets for fit of TID bump

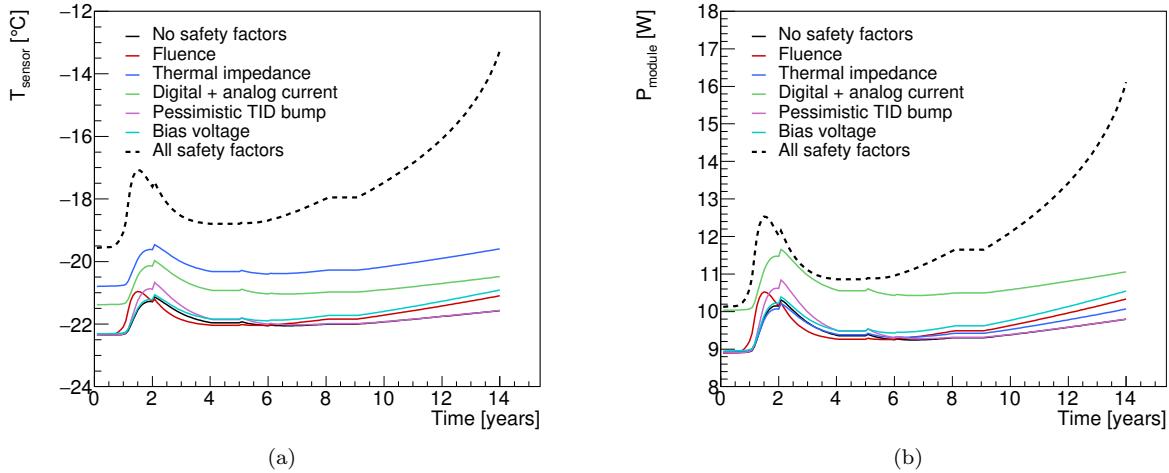


Figure 10: Comparing the impact of different safety factors on (a) the sensor temperature and (b) the module power for the endcap R3-type module, using a flat cooling scenario (-30°C). The dotted line depicts the effect of all safety factors applied at once.

297 further irradiation, or if the cooling temperature were raised, this growth would ultimately lead to thermal
 298 runaways. Due to the radial dependence of the radiation environment, the radiation-induced effects are most
 299 pronounced in the innermost barrel layers.

300 7.4. System properties

301 One of the key concerns for the design of the strip system is thermal stability of the system. If the
 302 cooling temperature is too high to limit the leakage power from the radiation-damaged sensors to a level
 303 where the heat can still be removed, the system is unstable (it goes into ‘thermal runaway’). To find the
 304 cooling temperature T_C at which this condition is reached, we make repeated simulations of the ITk strip
 305 system using the thermo-electrical model, with each simulation representing the full 14-year operation of
 306 the ITk at a fixed T_C . Between simulations, T_C is increased in steps of 5°C until the model finds thermal
 307 runaway. In the numeric evaluation of the thermo-electrical model this manifests itself in the absence of a
 308 solution to the system of equations. In the endcap strip system, this occurs at a cooling temperature of
 309 -15°C under nominal conditions (i.e. with no safety factors applied); in this scenario, thermal runaway
 310 would be reached in the 12th year of operation. With all safety factors applied, thermal runaway would occur
 311 at a cooling temperature of -25°C (in year 10). In the barrel system, where the radiation environment is
 312 slightly less intense, the conditions for thermal runaway occur at the same cooling temperatures, but a few
 313 years later than in the endcaps: in the final year of operation and a cooling temperature of -15°C under
 314 nominal conditions, and at -25°C (in year 13) with safety factors applied. As the design cooling temperature

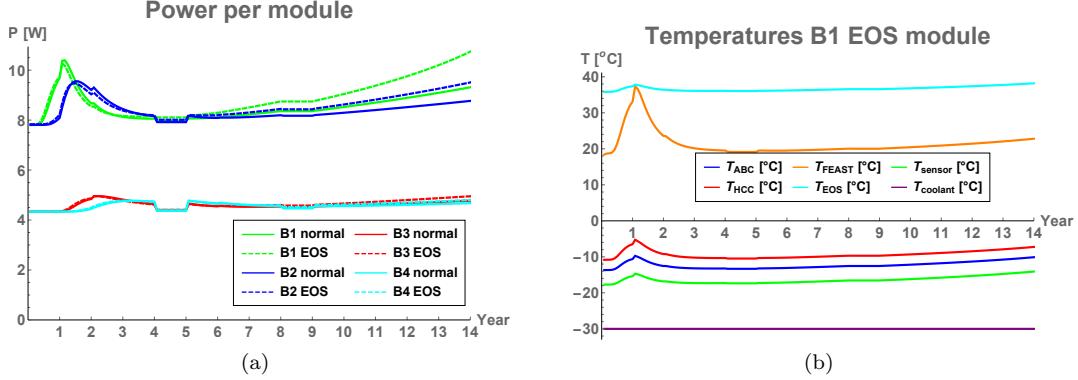


Figure 11: Examples of barrel module performance predictions for a flat cooling scenario (-30°C) including safety factors. (a) Power per module. (b) Temperatures for different nodes of an end-of-stave barrel module in the innermost barrel. The discontinuities in year 5 and 9 are due to anticipated year-long shutdowns of the LHC.

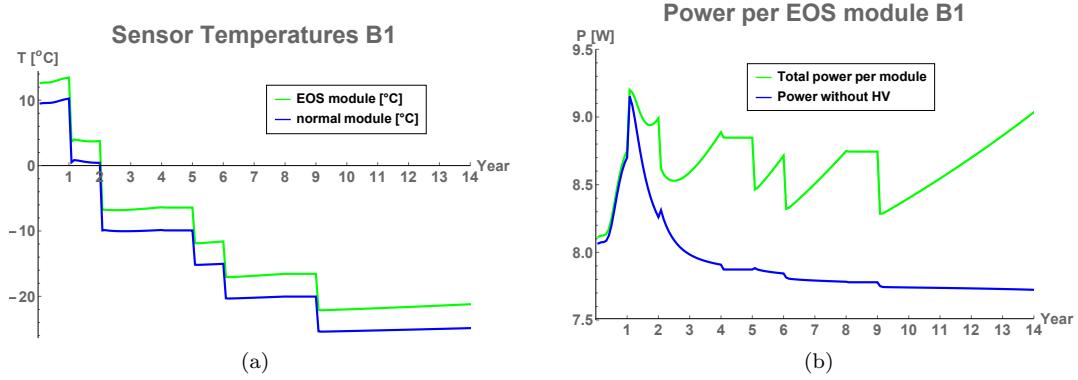


Figure 12: Examples of barrel module performance predictions for the ramp cooling scenario including safety factors. (a) Sensor temperature in the innermost barrel modules. (b) Power in an end-of-stave barrel module in the innermost layer.

315 of the ITk cooling system is -35°C , we have confidence that the ITk strip system has a sufficient margin for
316 thermal stability.

317 Beyond the issue of stability, the thermo-electrical model delivers predictions for the development of
318 current and power requirements for the overall system. Some of the predictions are shown in Fig. 13. Again,
319 the different timescales of the various radiation-induced effects are visible; ignoring this time dependence
320 could lead to over-specification of some system aspects like the total cooling power.

321 The predictions from this model are now used throughout the strip project to consistently size the power
322 supply and cooling systems. Including safety factors in the predictions gives us some confidence that the
323 designs are robust; by using commonly agreed safety factors, we ensure a consistent use of safety factors
324 throughout the project and prevent safety factor creep.

325 Because of the different timescales for the peak power due to the TID effect and the radiation-induced
326 sensor leakage, there is room to optimize the cooling temperature profile to minimize the total power in the
327 strip system while avoiding thermal runaway. The thermo-electrical model is a powerful tool to plan such an
328 optimized cooling profile. In fact, the cooling ‘ramp’ scenario introduced in Section 7.1 is the result of such
329 an optimization (see Fig. 14).

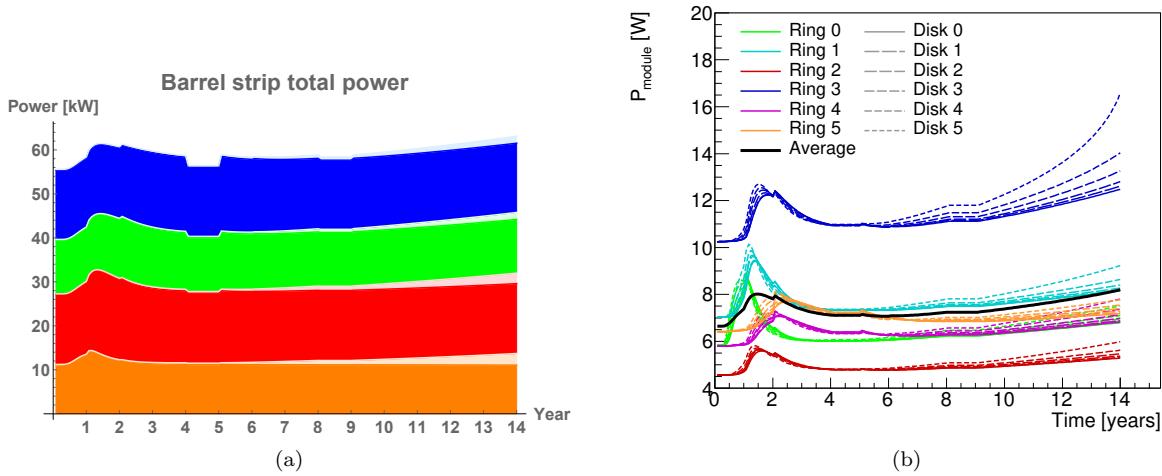


Figure 13: Examples of system performance predictions. (a) Barrel total power requirements. The plot shows the stacked power requirements for the four barrel layers (orange: innermost barrel, blue: outermost barrel). Full colour indicates power from the front-end electronics, greyed parts are contributions from HV power for the four barrels. The discontinuities in year 5 and 9 are due to anticipated year-long shutdowns of the LHC. (b) The power requirements for each of the 36 simulated endcap modules, labeled according to their ring type and disk position. The solid black line indicates the average module power. Both predictions use a scenario with flat -30°C cooling and including all safety factors.

330 8. Model performance verification

331 The accuracy of the predictions of the thermo-electrical model is affected by two major factors: the quality
 332 of the input parameters, and the error introduced by reducing the complex 3D geometry into a linear thermal
 333 impedance network. The former has been discussed throughout this paper where the different inputs have
 334 been presented. For the latter, we have studied the agreement of predictions from the network model with
 335 the more accurate results obtained from FEA for selected states of the system.

336 To verify the level of this agreement, we have calculated the sensor temperature curve for a barrel EOS-
 337 type module up to thermal runaway, both in the full FEA and in the network model. For this exercise, we do
 338 not vary any of the input parameters in the model other than the sensor leakage power with its temperature
 339 dependence. The resistor values in the network model are the same as used throughout for our model,
 340 obtained as described in Section 4. For the power from the various electronics components, the FEAST
 341 efficiency and the TID scale factor we have used representative nominal values.

342 Because the variable model inputs are kept constant for this study, we can reduce the complex thermal
 343 network to its Thévenin equivalent, which is identical to the network studied in Ref. [5], and use the analytical
 344 expressions given there. The reduced network is described by the base temperature T_0 , defined as the sum
 345 of the coolant temperature and the temperature rise due to the front-end electronics alone, and the total
 346 thermal impedance R_t from the sensor to the coolant. Using the nominal resistances and representative power
 347 numbers from the module, $T_0 = -21.9^{\circ}\text{C}$ and $R_t = 1.132 \text{ K/W}$ in the network model, compared to -22.4°C
 348 and 1.147 K/W obtained directly from the FEA. The comparison of the predicted sensor temperatures for
 349 both cases is shown in Fig. 15. Despite a large temperature variation of about 10°C across the sensor,
 350 the network model runaway prediction agrees well with the FEA⁴. This gives us confidence that the use
 351 of a thermal network model is not likely to significantly degrade the predictions beyond the uncertainties
 352 introduced by other inputs to the model.

⁴The critical temperature here is -12.4°C , which is higher than the numbers given in Section 7.4, because the study here ignores temperature effects such as the FEAST efficiency, which can only be modelled in the network model.

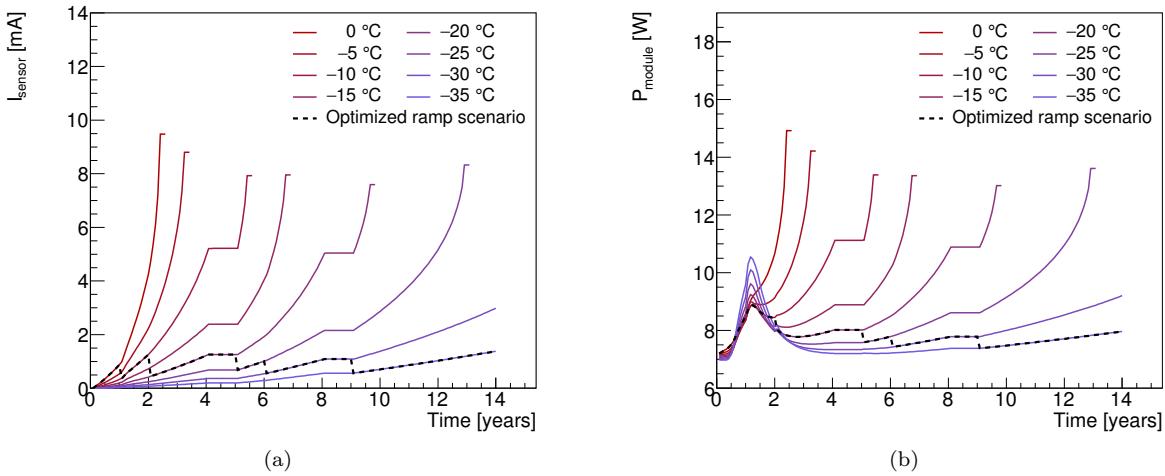


Figure 14: (a) Sensor leakage current and (b) total power of the endcap R1-type module for eight different flat cooling profiles, ranging from 0°C to -35°C , as well as the cooling ramp scenario specified in Fig. 9b (dashed curve). The curves that are discontinued before year 14 correspond to scenarios that have reached thermal runaway. The cooling ramp scenario has been selected to minimize the module power while keeping the sensor leakage current stable throughout the lifetime of the ITk. All safety factors are applied in these plots.

353 9. Conclusions

354 We have developed a model of the ATLAS ITk strip system that is based on the interplay between a
 355 thermal and an electrical network model. The set of equations in the model can be numerically solved using
 356 standard data analysis software in a short time, allowing for a quick turn-around for systematic studies of the
 357 system performance. The complexity of these networks is given by the number of interconnected components
 358 between the networks, many of which have a non-linear dependence on the temperature or electrical power.
 359 This approach can be easily adopted for any other silicon detector system.

360 In the case of the ATLAS strip system, several temperature-dependent heat sources had to be modeled.
 361 In addition to the sensor leakage current, these are the radiation-induced increase of the digital front-end
 362 power ('TID bump') and the efficiency of the DC-DC conversion system. The outputs of the model give
 363 us confidence that the ITk strip system will be thermally stable until the end of LHC Phase-II operation,
 364 even with the inclusion of safety factors on key inputs. Furthermore, the model provides information for
 365 benchmark system parameters like cooling, supply power and currents in power cables, which is used in the
 366 specification of these systems. The use of the model outputs throughout the strip project ensures consistent
 367 specifications, including a common strategy on safety factors. Using the thermo-electrical model, we can also
 368 propose an optimized cooling temperature 'ramp' scenario, which stabilizes leakage power throughout the
 369 lifetime of the experiment while minimizing the TID bump.

370 We have verified the performance of the thermal network model compared to a full FEA treatment, and we
 371 are confident that the level of disagreement is smaller than the uncertainty introduced by the model inputs.
 372 Among the inputs, the most likely source of uncertainty stems from the limitations in our understanding of
 373 the parametrization of the TID effect.

374 10. Acknowledgements

375 The evaluation of the thermo-electrical model depends critically on the input parameters to the model.
 376 To capture the whole of the system, these need to distill all that is known of the system, and we are therefore
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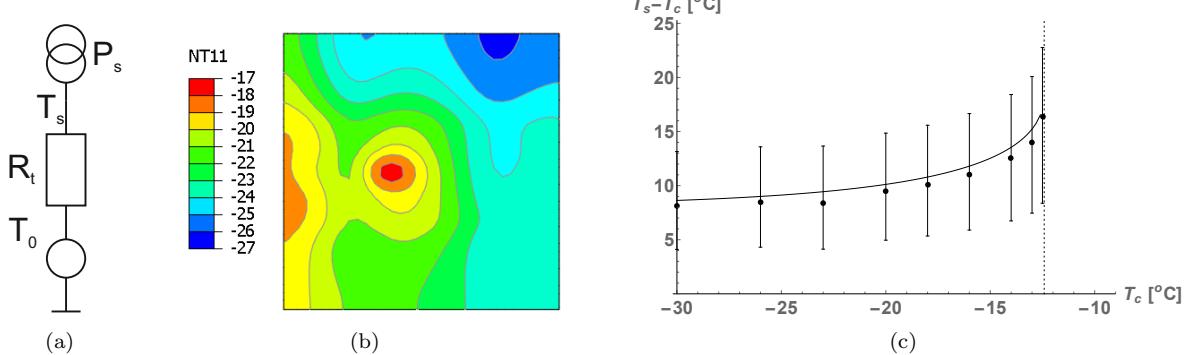


Figure 15: (a) Thévenin equivalent of the thermal network. (b) Result of sensor surface temperature calculations using FEA, assuming zero sensor power. The EOS card is to the left of the module, and the cooling pipes run from top to bottom about a quarter of the module width from each edge. (c) Difference of average sensor and coolant temperature, comparing FEA (dots) and the network model prediction (curve). The bars on the FEA data indicate minimum and maximum sensor temperature. The dotted vertical line indicates the critical temperature derived analytically using the network model (-12.4 °C).

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