

Thermoelectric modeling of the ATLAS ITk Strip Detector

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Abstract

Here is the abstract.

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1. Introduction

The temperatures in silicon detector systems are critically important to the performance of these systems. The leakage current shows a pronounced temperature dependence

$$I \propto T_S^2 e^{-T_A/T_S} \quad (1)$$

where T_S is the sensor temperature and $T_A \simeq 7000$ K. Leakage currents can become particularly significant after irradiation of the silicon material. The heat generated by these leakage currents in the silicon sensor, together with the heat from front-end electronics components on the detector needs to be removed by cooling systems. Due to the strong growth of leakage power with temperature there is a critical temperature T_C , above which the heat cannot be removed quickly enough, and the detector becomes thermally unstable ('thermal runaway'). The capability of the cooling system in removing this heat is limited by the temperature of the local cold sink (typically the coolant temperature) and the thermal impedance of the heat path between the source (electronics and sensor) and the sink.

In addition, there can be aspects of the front-end electronics which are temperature-dependent. For example, in the strip system for the ATLAS phase II upgrade (ref) there are two additional sources for temperature-dependent heat sources. The first is a radiation damage effect in the digital part of the readout-electronics (the ABC130 and HCC chips), which is manufactured in 130 nm technology by the xxx process (ref). This effect leads to a scaling of the digital power in the chip depending on the received dose rate (TID) and the temperature of the chip (ref). This has been first observed in the ATLAS IBL (ref). The other temperature dependence of the power generated by the front-end electronics stems from the temperature dependence of the converter chip (FEAST (ref)) used in the on-detector DC-DC converter system supplying power to the front-end electronics.

Even before the limit of thermal stability is reached, knowledge of temperatures in silicon detector systems is important, as they define system parameters like power supply capacity and cable dimensions.

In principle the temperatures in the system for a given set of operational parameters (power density, thermal conductivities etc.) can be predicted by FEA to an accuracy which is given by the quality of the input parameters. However, this is a time-consuming process and can be prohibitively difficult if there is a large number of local heat sources depending non-linearly on the temperature. A simplification to this problem which allows for an analytical solution in the case of a simple heat source topology has been developed in [1]. In this paper we develop this method further to include several temperature dependent non-linear heat sources in the front-end electronics. The resulting set of equations cannot be solved analytically any more, but with little effort using numerical problem solvers. This enables us to predict with some confidence the temperatures and power requirements in the ATLAS strip system throughout phase II operation. The results from this prediction have been used throughout the project to consistently dimension the different systems (cooling, power, services etc.) also with some robustness due to the inclusion of a common set of safety factors. This method can be easily adapted to any other system after adjustment of the system specific geometries and parameters.

1.1. The ATLAS strip system

The strip system for the ATLAS phase II upgrade (ref TDR) consists of two parts: the barrel system comprised of four concentric cylindrical barrels and the two endcaps, which consist of six disks each.

In the barrel the detector modules are made of square sensors ($96.85 \times 96.72 \text{ mm}^2$) with a hybrid on top, which hosts the front-end chips (ABC* and HCC*), but also circuitry to convert the supply voltage of larger than 10 V to the chip voltage of 1.5 V. This circuitry is controlled by the FEAST chip. The modules are glued onto both sides of a composite sandwich which contains two parallel thin wall titanium cooling pipes embedded in carbon foam (Allcomp K9 - ref) between two facesheets of UHM carbon fibre (3 layers of K13C2U/EX1515) with a co-cured Kapton/copper low-mass tape. A model of this geometry is shown in fig. 1. During final operation cooling will be achieved by evaporating CO_2 in the cooling pipes with a final target temperature of not higher than -35°C anywhere on the stave. With the exception of the end region of the stave, where a side-mounted End-Of-Structure (EOS) card is located and the thermal path is degraded by the presence of electrically insulating ceramic pipe sections, the geometry of the stave is uniform along its length.

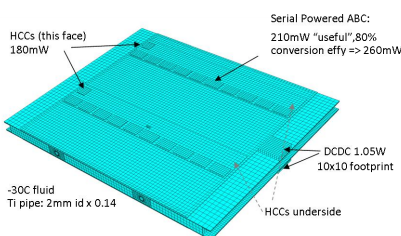


Figure 1: Barrel strip geometry

The endcap detector consists of six disks, each containing 32 “petals” loaded on both sides with six silicon modules (twelve total). The endcap detector modules consist of six distinct designs located at increasing radius from the beam pipe and labeled R0 through R5 (where “R” stands for ring). Each endcap module consists of one or two irregularly-shaped silicon sensors, and a varying number of front-end chips on each module (between 12 and 28 ABCs, and 2 to 4 HCCs). The EOS card is located adjacent to the R5 module, but the cooling pipes (and not the electrical breaks) run directly underneath it, in contrast to the barrel EOS. The remaining module and petal core design details are largely identical to the barrel module description above. Fig. 2 depicts the geometry of the endcap petal.

Figure 2: Endcap strip geometry

1.2. Radiation environment

A key input to the calculation is the radiation environment of the strip system, as several inputs depend on radiation damage effects. The sensor leakage current is a function of the fluence expressed in 1 MeV neutron-equivalents, and the TID effect on the digital chip current will be parametrized as a function of the total ionizing dose rate (more details on its dependencies can be found in section xxx).

Both these

2. The electrical model

The electrical model consists of low-voltage (LV) and high-voltage (HV) circuits, depicted in Fig. 4. The LV current is used to power the hybrid controller chips (HCCs), ATLAS Binary Chips (ABCs) and Autonomous Monitoring and Control chip (AMAC) located on PCBs that are glued directly onto the surface of the sensor. The number of chips vary according to the design of each different module type (barrel short-strip and long-strip modules, and six different endcap module designs).

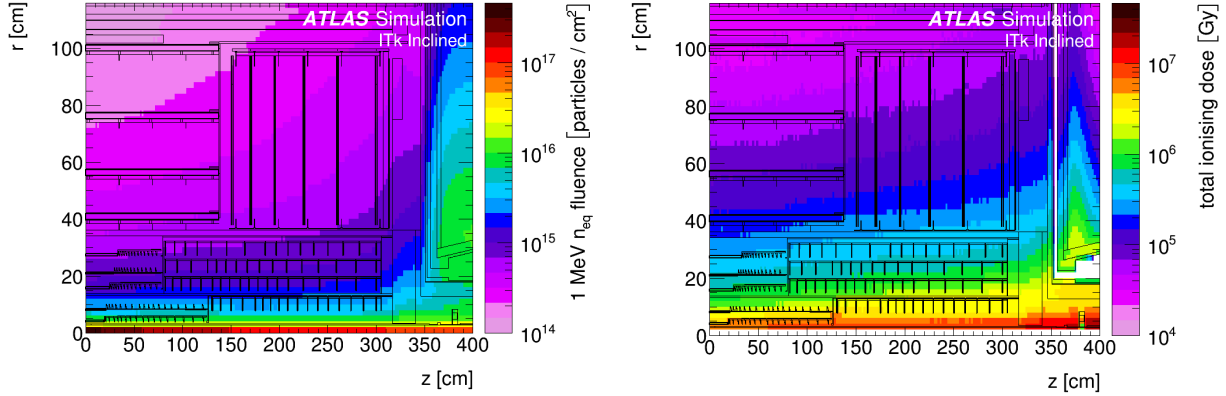


Figure 3: ATLAS ITk radiation environment. 1 MeV neutron equivalent fluence (left) and total ionizing dose (right). Both plots are for an integrated luminosity of 4000 fb^{-1} (ref strip TDR).

The ABCs and HCCs are all powered at 1.5 V using a DCDC converter (the FEAST) to step the voltage down from 11 V. Typically one FEAST is used per module is used to power the chips; however, due to the large number of ABCs on endcap module R3, the load is split across two FEAST converters.

The AMAC contains a component powered at 1.5 V and one powered at 3 V; both are delivered from the 11 V source by an LDO regulator with a 1.9 mA quiescent current. Again, the endcap module R3 differs from other modules, containing two AMACs each powered by its own LDO.

The bus tape, which carries both LV and HV currents, is expected to emit some heat due to the wire resistance. This impacts the module in two ways: first, the tape itself will radiate some heat according to the amount of current passing through it; this source of heat is accounted for in the model, however the contribution to the total power of the module is negligible. Second, the voltage supplied to the module will be affected by the small ΔV in the bus tape. This effect is largest for modules on the non-EOS end of the barrel stave or endcap petal, where the current has traveled a longer distance. The treatment of this effect is slightly different in the barrel and endcap models: in the barrel, the voltage delivered to every module is set at 10.5 V; in the endcap, the ΔV is estimated based on the calculated expected power loss along the tape for each module. In both cases, the effect of different treatment is small.

The low-voltage current is also delivered to the EOS card to power various data transfer components, which require 2.5 V and 1.2 V currents. On the EOS, a FEAST identical to the one used on the module is used to step the voltage down from 11 V to 2.5 V; an additional LDO regulator brings 2.5 V down to 1.2 V for some components.

Finally, the HV current is used to provide the voltage bias on the silicon sensors. An HV multiplexer switch (HVMUX) is placed in parallel to the sensor, which can be used to disconnect the sensor from the bias line. Two HV filters with an effective resistance of 10 k Ω are placed in series with the sensor. The nominal operating voltage of the sensor is expected to be 500V, but the system is designed to operate with a voltage bias of up to 700V.

3. The thermal model

The thermal network consists of heat sources (some of which are temperature dependent) and thermal resistances. The latter are given by the properties of the mechanical design (heat conductivities of the materials) and the geometry of the heat path. The geometry is generally 3-dimensional, but it is the strategy of the simple network models to lump the 3-dimensional behaviour into one thermal resistance parameter. In the models discussed here we have used a granularity corresponding to single detector modules for which the thermal resistance has been modelled. The temperatures in the model are then given for the nodes in the network in analogy to the potentials in an electrical network.

The complexity of the thermal network used in this study (see figure 5) is given by the variety of different temperature-dependent heat sources in the ATLAS strip system. In addition to the sensor leakage currents these are the digital power for each type of chip, and the heat generated by the FEAST chip, which is

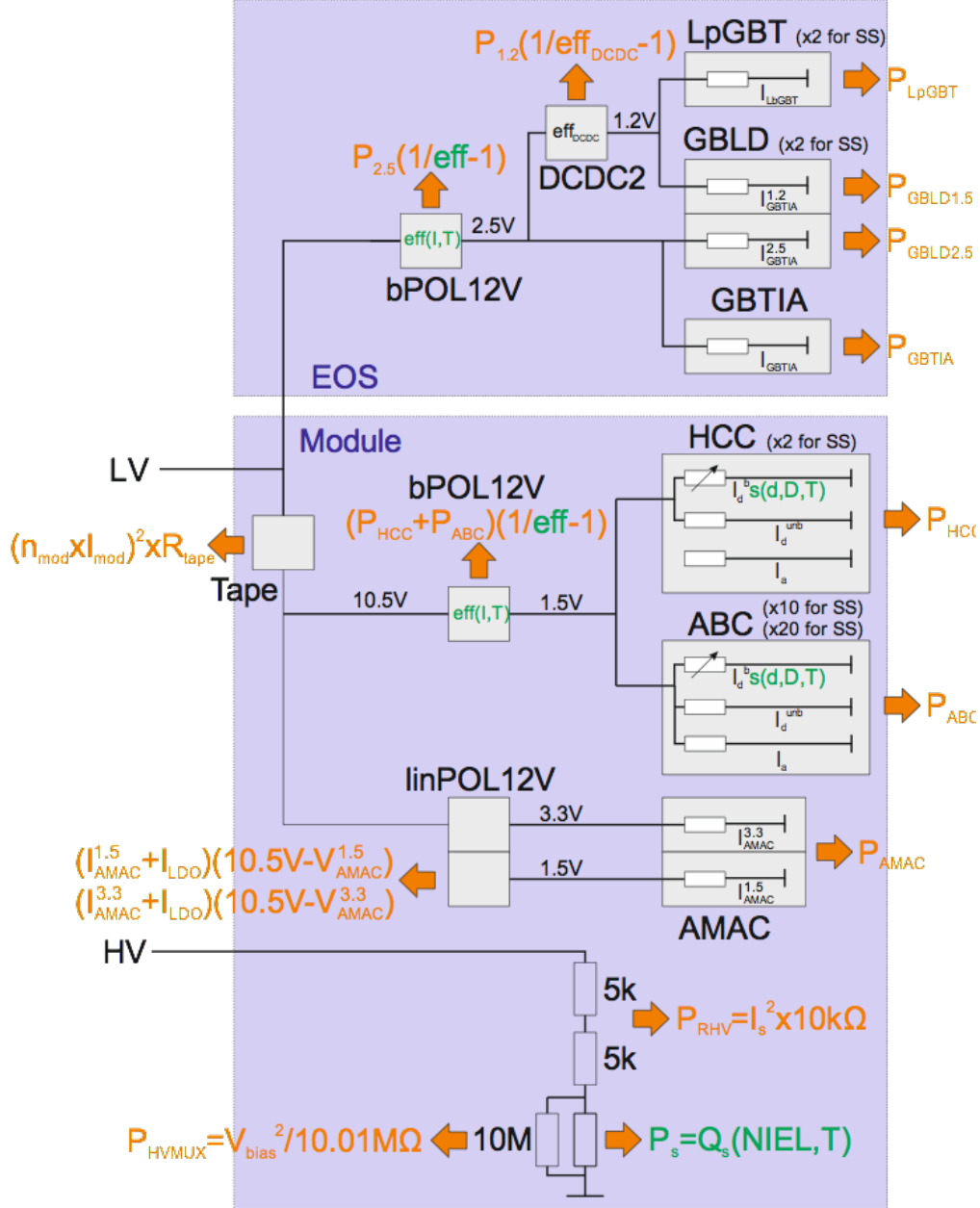


Figure 4: The electrical model of the ITk Strip barrel and endcap modules.

providing the DC-DC conversion on the detector. In the ATLAS SCT modules all these components are located on top of the sensors, so that the heat generated in them flows through the sensor into the support structure, the stave (barrel) or petal (endcap) core with the embedded cooling pipe. In the network model the heat flow from these sources is combined and flowing through a common impedance R_M to the sink at a temperature T_C . For each of the temperature-dependent heat sources (ABC, HCC, FEAST and the sensor) we have added a resistance from the common temperature T_{mod} to allow for a finite and different heat path for each if them. Finally, in the case of the barrel system, there is an additional source of heat for the last module on the stave, which is the adjacent End-of-substructure (EOS) card, which is modeled by an additional source with an impedance for its special heat path.

This is a more complex thermal network than the one studied in ref. [1], where an analytical solution

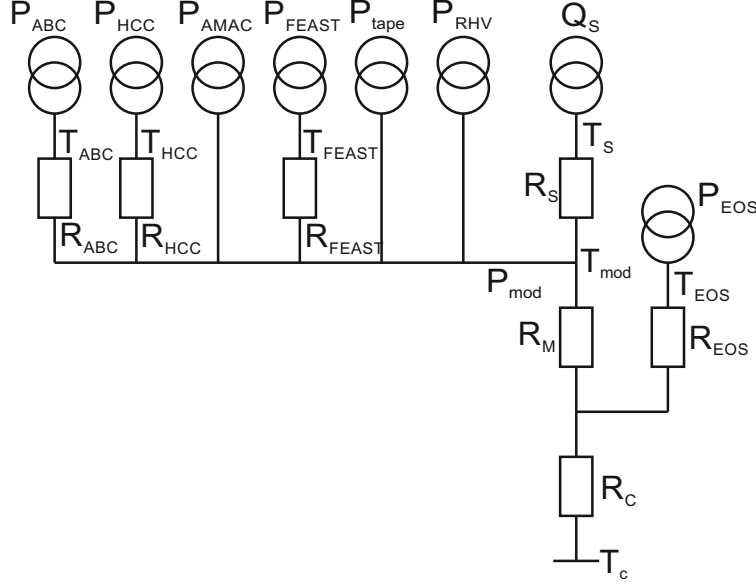


Figure 5: Thermal network model.

for the determination of thermal stability was given. In particular because of the non-linear temperature dependence of some of the heat sources it is not possible any more to solve the set of equations describing the model here analytically. However, the set of equations is still sufficiently small to solve it numerically using readily available functions in Mathematica (used in the barrel model) or xxx (used in the endcap system).

4. Obtaining thermal impedances using FEA

Explain the method of extracting impedances of thermal pathways using FEA.

5. Other model inputs

Explain the specific challenges in the strip detector that are parameterized and modeled in our case.

5.0.1. DCDC converter

The DCDC converter (FEAST) supplies a low-voltage (1.5 V) current to the ABC130 and HCC front-end chips on the module. The efficiency of the FEAST depends on its temperature as well as the output (load) current load delivered to the front-end chips. To correctly model the FEAST efficiency, experimental measurements are performed to characterize the dependence and fitted with a functional form.

To measure the FEAST efficiency, the FEAST power board was glued to an aluminum cold plate, cooled with CO₂, and powered with the nominal working input and output voltages (11 V input, 1.5 V output). The temperature of the FEAST is measured with an NTC thermistor and PTAT sensor residing on the FEAST, for a range of load currents up to the maximum design current of 4A¹.

The data is then fit with a function with sufficient parameters to ensure reasonable agreement; the choice of functional form has no physical interpretation. Figure 6 depicts the FEAST efficiency data and the parameterized fit used in the model.

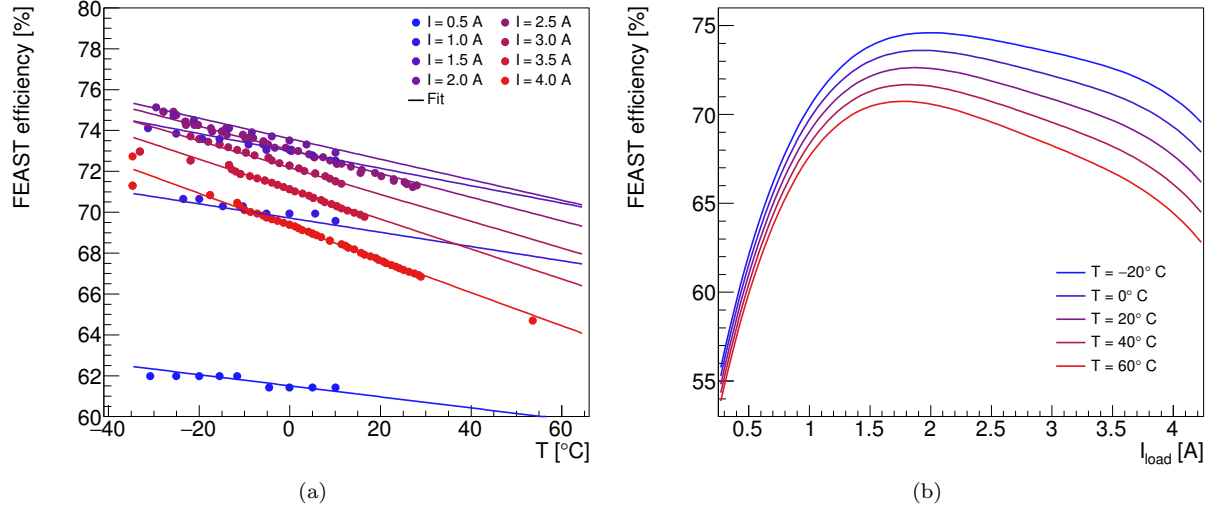


Figure 6: The FEAST efficiency model based on experimental data. (a) The experimental data points characterizing the FEAST efficiency are plotted as dots and color coded for load current. The data is compared to the analytic fit, evaluated in curves of equal current. (b) The same analytic fit, presented as a function of current load for curves of equal temperature.

5.0.2. Digital current increase of chips using 130 nm CMOS technology

5.0.3. Modeling flux and total ionizing dose in endcap modules

6. Running the model

The thermoelectric model constructs a profile of the sensor module operation conditions over the lifetime of the detector in the following manner. First, assuming a reasonable set of initial component temperatures, the module total power (including all components, but excluding the sensor leakage power) and the sensor temperature without leakage current (T_0) is calculated assuming these initial temperatures. The initial value for the module power is used to solve for the sensor power and temperature accounting for leakage current, using the thermal balance equation and the relationship from Eq. ???. Using the calculated sensor leakage current and temperature, the power and temperature of the module components are updated given the initial (year-0, month-0) startup parameters.

Next, the module conditions of the following month (year-0, month 1) are calculated. Using the component temperatures calculated from the previous month and the operational parameters (ionizing dose and dose rates) from month 1, the module total power (excluding sensor leakage) is again recalculated, and subsequently the sensor temperature and leakage current are recomputed. Following this, the module component temperatures and power values are updated. This process is repeated in one-month steps until the final year of operation, or until a real solution for the sensor temperature does not exist, indicating that thermal runaway conditions have been reached.

In the barrel subsystem, the above procedure is performed four separate times to represent the conditions of the four barrel layers located at different radii from the beam axis². The procedure is also performed once for a module adjacent to an EOS and a representative module of the remaining 13 without an adjacent EOS. In each case, the worst-case total ionizing dose and dose rate is assumed for each layer, though these values are relatively consistent for a given layer. In total, 8 modules are simulated, and they are combined in their proper proportion to simulate the entire barrel system.

In the endcap subsystem, the total ionizing dose and dose rates vary significantly depending on the position

¹ FEAST data spreadsheet: http://project-dcdc.web.cern.ch/project-dcdc/public/Documents/FEASTMod_Datasheet.pdf. Cite?

² The correct module type, short-strip in the inner two layers and long-strip for the outer two layers, is used for each layer.

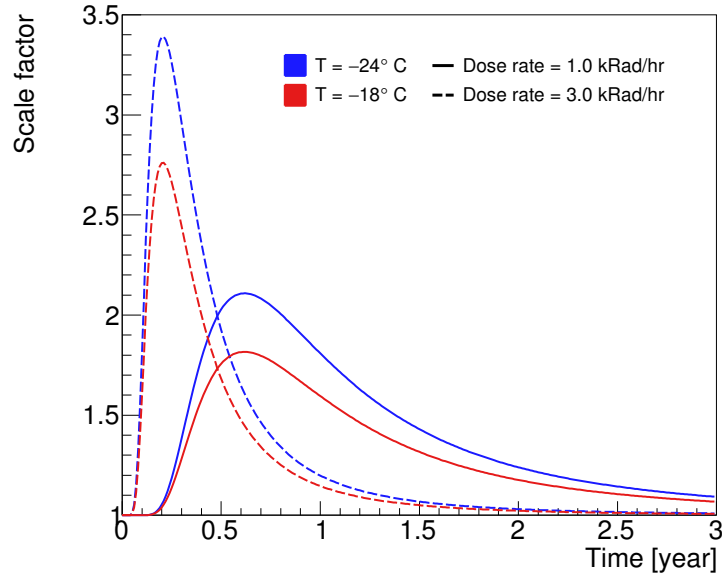


Figure 7: Parameterization of the impact of the total ionizing dose on the magnitude of the front-end chip digital current. The current is multiplied by a scale factor that is modeled as a function of dose rate and temperature, based on experimental data.

of the module; furthermore, the design of each module on a petal differs significantly. Therefore, all 36 module types (6 rings \times 6 disks) are simulated independently, and combined to represent the full endcap.

7. Outputs of the thermoelectric model

(Specifications using safety factor scenarios. Specifications for modules, global sytem requirements. Qualitative understanding of system properties and evolution.)

8. Model performance verification

9. Conclusions

(Conclusions.)

10. Acknowledgements

(Acknowledgements.)

References

- [1] G. Beck, G. Viehhauser, Analytic model of thermal runaway in silicon detectors, Nucl. Instrum. Meth. A618 (2010) 131–138. doi:10.1016/j.nima.2010.02.264.