

Thermoelectric modeling of the ATLAS ITk Strip Detector

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Abstract

Here is the abstract.

Keywords: Silicon detector, Thermal runaway, Thermal management, Cooling

1. Introduction

The temperatures in silicon detector systems are critically important for the performance of these systems.

The leakage current shows a pronounced temperature dependence

$$I \propto T_S^2 e^{-T_A/T_S}, \quad (1)$$

where T_S is the sensor temperature and $T_A \simeq 7000$ K. Leakage currents can become particularly significant after irradiation of the silicon material. The heat generated by these leakage currents in the silicon sensor, together with the heat from front-end electronic components on the detector, needs to be removed by a cooling system. Due to the strong growth of leakage power with temperature there is a critical temperature T_{crit} above which the heat cannot be removed quickly enough, and the detector becomes thermally unstable ('thermal runaway')¹. The capability of the cooling system to remove this heat is limited by the temperature of the local cold sink (typically a circulated fluid) and the thermal impedance of the heat path between the source (electronics and sensor) and the sink.

In addition, there can be aspects of the front-end electronics that are temperature-dependent. For example, in the strip system for the ATLAS Phase-II upgrade [1] there are two additional temperature-dependent heat sources. The first is a radiation damage effect in the digital part of the readout electronics (the ABC130 and HCC chips), which is manufactured in 130 nm technology by the CMOS 8RF process (ref). This effect leads to an increase of the digital power in the chip depending on the total ionisation dose (TID) and the temperature of the chip (ref). This has been first observed in the ATLAS IBL [2]. The other temperature dependence of the power generated by the front-end electronics stems from the converter chip (FEAST (ref)) used in the on-detector DC-DC converter system supplying power to the front-end electronics.

Even before the limit of thermal stability is reached, knowledge of temperatures in silicon detector systems is important, as they define system parameters like power supply capacity and cable dimensions.

In principle the temperatures in the system for a given set of operational parameters (power density, thermal conductivities, etc.) can be predicted by FEA to an accuracy that is limited only by the quality of the input parameters. However, this is a time-consuming process and can be prohibitively difficult if a number of local heat sources depend non-linearly on the temperature. A simplification to this problem that allows for an analytical solution in the case of a simple heat source topology has been developed in [3]. Here we develop this method further to include several temperature-dependent non-linear heat sources in the front-end electronics. The resulting set of equations cannot be solved analytically anymore, but the solution can be found with little effort using numerical problem solvers. This enables us to predict with some confidence the temperatures and power requirements in the ATLAS strip system throughout Phase-II operation. The results from this prediction have been used throughout the project to consistently dimension the different systems (cooling, power, services, etc.) also with some robustness due to the inclusion of a common set of

¹In a real detector system the resulting growth of sensor temperature would be arrested by overcurrent limits in the power supplies, resulting in a reduction of the bias voltage. At the same time the increased current leads to an increase of the noise, so that the overall result is a degradation of the S/N performance of the system.

37 safety factors. This method can be easily adapted to any other system by adjusting to the system-specific
38 geometries and parameters.

39 *1.1. The ATLAS strip system*

40 The strip system for the ATLAS Phase-II upgrade [1] consists of two parts: the barrel system comprises
41 four concentric cylindrical barrels, and the two endcaps, which consist of six disks each.

42 In the barrel, the detector modules are made of square sensors ($96.85 \times 96.72 \text{ mm}^2$) with a hybrid on
43 top, which hosts the front-end chips (ABC130 and HCC), but also circuitry to convert the supply voltage of
44 larger than 10 V to the chip voltage of 1.5 V. This circuitry is controlled by the FEAST chip. The modules
45 are glued onto both sides of a composite sandwich that contains two parallel thin-wall titanium cooling
46 pipes embedded in carbon foam (Allcomp K9 - ref) between two facesheets of UHM carbon fibre (3 layers
47 of K13C2U/EX1515) with a co-cured Kapton/copper low-mass tape. A model of this geometry is shown
48 in Fig. 1. During final operation, cooling will be achieved by evaporating CO₂ in the cooling pipes with a
49 final target temperature no higher than -35°C anywhere on the stave. The geometry of the stave is uniform
50 along its length, with the exception of the end region of the stave, where an End-Of-Structure (EOS) card is
51 mounted on both surfaces, which shares part of the heat path from the module, and where the thermal path
52 is degraded by the presence of electrically-insulating ceramic pipe sections.

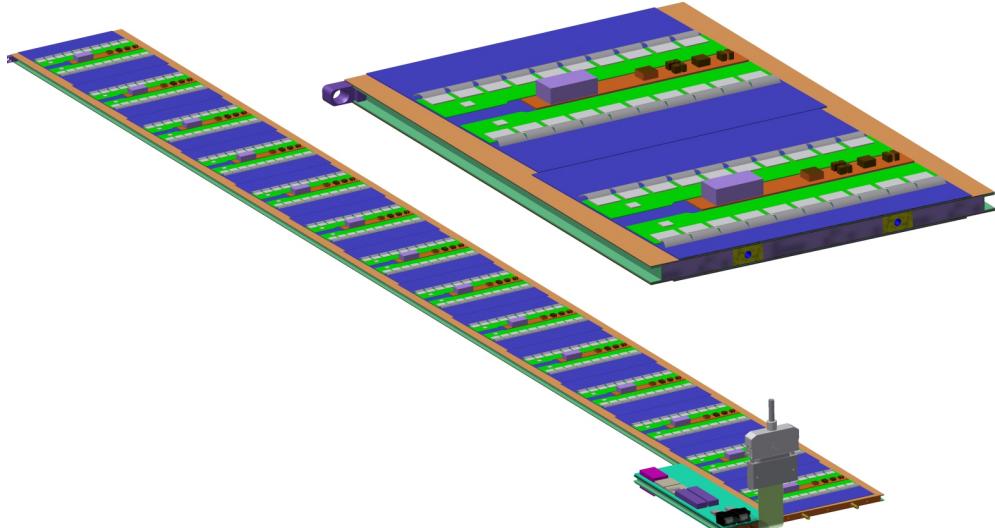


Figure 1: Strip barrel local support geometry. On the left, a complete stave is shown (EOS card in the foreground). The right picture shows a cross-section of the stave with the two cooling pipes visible inside the core.

53 The endcap detector consists of six disks, each containing 32 ‘petals’ loaded on both sides with six silicon
54 modules (twelve in total). The endcap detector modules consist of six distinct designs located at increasing
55 radius from the beam pipe and labeled R0 through R5 (where ‘R’ stands for ring). Each endcap module
56 consists of one or two irregularly-shaped silicon sensors, and a varying number of front-end chips on each
57 module (between 12 and 28 ABCs, and 2 to 4 HCCs). The EOS card is located adjacent to the R5 module,
58 but the cooling pipes (without electrical breaks) run directly underneath it without a shared heat path, in
59 contrast to the barrel EOS. The remaining module and petal core design details are largely identical to the
60 barrel module description above. Fig. 2 depicts the geometry of the endcap petal.

Figure 2: Endcap strip geometry

61 **1.2. Radiation environment**

62 A key input to the calculation is the radiation environment of the strip system, as several inputs depend
 63 on radiation damage effects. The sensor leakage current can be parametrized as a function of the fluence
 64 expressed in 1 MeV neutron-equivalents, and the TID effect on the digital chip current will be described as
 65 a function of the total ionizing dose rate (more details on its dependencies can be found in Section 7).

66 Predictions for both of these parameters for each point in the ITk are available which have been generated
 67 using the FLUKA particle transport code and the PYTHIA8 event generator (Fig. 3) [ref]. Both of these
 68 distributions display a weak dependence on z in the barrel, whereas they vary significantly along r and z
 69 over the length of the endcap petals. Because of this, and the linear uniformity of the stave compared to
 70 the more complex geometry along a petal, we modelled only two types of modules for the barrel (a generic
 71 module along the linear part of the stave and the module next to the end-of-structure card), but six different
 72 types of modules in a petal.

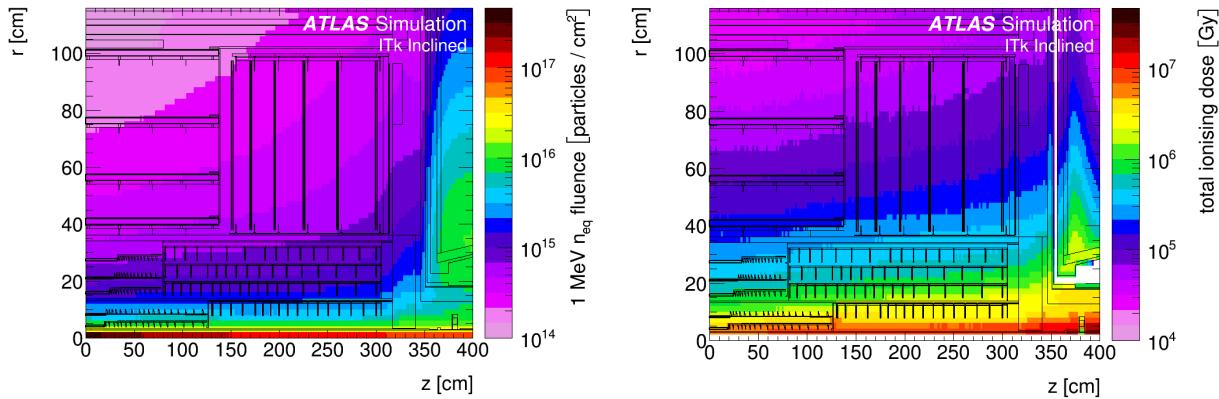


Figure 3: ATLAS ITk radiation environment. 1 MeV neutron equivalent fluence (left) and total ionizing dose (right). Both plots are for an integrated luminosity of 4000 fb^{-1} [1].

73 **2. The electrical model**

74 *From Graham: I think there is too much detail here (although it is doubtless accurate). Could the text be
 75 simplified, given that information is available in figure 4?*

76 The electrical model consists of low-voltage (LV) and high-voltage (HV) circuits, depicted in Fig. 4.
 77 The LV current is used to power the hybrid controller chips (HCCs), ATLAS Binary Chips (ABCs) and
 78 Autonomous Monitoring and Control chip (AMAC) located on PCBs that are glued directly onto the surface
 79 of the sensor. The number of chips vary according to the design of each different module type (barrel
 80 short-strip and long-strip modules, and six different endcap module designs).

81 The ABCs and HCCs are all powered at 1.5 V using a DCDC converter (the FEAST) to step the voltage
 82 down from 11 V (linPOL12V and bPOL12V in Fig. 4). Typically one FEAST per module is used to power
 83 the chips; however, due to the large number of ABCs on endcap module R3, the load is split across two
 84 FEAST converters on the module.

85 The AMAC contains a component powered at 1.5 V and one powered at 3 V; both are delivered from
 86 the 11V source by an LDO regulator with a 1.9 mA quiescent current. Again, the endcap module R3 differs
 87 from other modules, containing two AMACs each powered by its own LDO.

88 The bus tape, which carries both LV and HV currents, has a small wire resistance, which impacts the
 89 module in two ways. First, the tape itself will generate some heat according to the amount of current passing
 90 through it; this source of heat is accounted for in the model, however the contribution to the total module
 91 power is negligible. Second, the voltage supplied to the module reduces slightly with distance from the EOS
 92 end of the barrel stave or endcap petal. The treatment of this effect is slightly different in the barrel and
 93 endcap models: in the barrel, the voltage delivered to every module is set at 10.5 V; in the endcap, the ΔV
 94 is estimated based on the calculated expected power loss along the tape for each module. In both cases, the
 95 impact of using a different treatment is small.

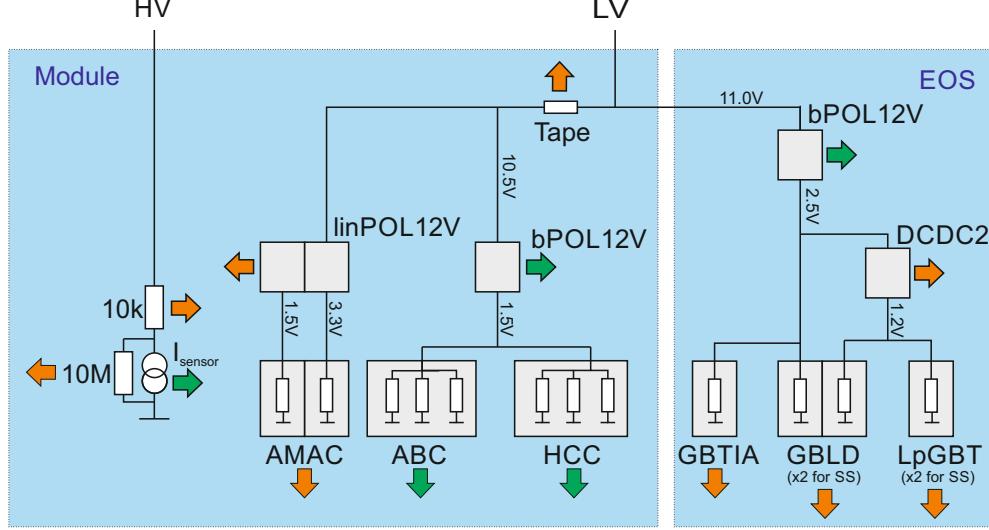


Figure 4: The electrical model of the ITk Strip barrel and endcap modules. Green arrows represent temperature-dependent heat sources, while orange arrows are temperature-independent. Grey squares are chips. Chip counts per module are linPOL12V/bPOL12V/AMAC: 1 each (2 each for EC R3); HCC: 1 for barrel LS, 2 for barrel SS and EC R0-R2 and R4-R5, 4 for EC R3; ABC: barrel: 10, 20 (LS, SS), EC: 17, 21, 21, 28, 16, 18 (R0-R5).

The low-voltage current is also delivered to the EOS card to power various data transfer components, which require 2.5 V and 1.2 V supplies. On the EOS, a FEAST identical to the one used on the module is used to step the voltage down from 11 V to 2.5 V; an additional LDO regulator brings the 2.5 V down to 1.2 V for some components. The EOS cards on the endcap petals and the long-strip staves have one GBLD and one LpGBT; EOS cards on the short-strip staves contain two of each. All EOS cards contain one GBTIA.

Comment from Graham: I think that if we are going to refer to GBLD, LpGBT etc. then there should be a short sentence that describes (in a word) what each of these chips does?

Finally, the HV current provides the voltage bias on the silicon sensors. An HV multiplexer switch (HVMUX) is placed in parallel to the sensor, which can be used to disconnect the sensor from the bias line requiring a parallel resistor in order to function. Two HV filters with an effective resistance of $10\text{ k}\Omega$ are placed in series with the sensor. The nominal operating voltage of the sensor is expected to be 500V, but the system is designed to operate with a voltage bias of up to 700V.

3. The thermal model

The thermal network consists of heat sources (some of which are temperature dependent) and thermal resistances. The latter are given by the properties of the mechanical design (heat conductivities of the materials) and the geometry of the heat path. The geometry is generally 3-dimensional, but it is the strategy of the simple network models to lump the 3-dimensional behaviour into one thermal resistance parameter. In the models discussed here we have used a granularity corresponding to single detector modules for which the thermal resistance has been modelled. The temperatures in the model are then given for the nodes in the network in analogy to the potentials in an electrical network.²

The complexity of the thermal network used in this study (see Fig. 5) is given by the variety of different temperature-dependent heat sources in the ATLAS strip system. These sources consist of the digital power for each type of chip, the heat generated by the FEAST chip providing the on-detector DC-DC conversion, and the sensor leakage currents. In the ATLAS ITk strip modules all of these components are located on top

²Historically Fourier's description of heat conduction pre-dated and inspired Ohm's work on electrical resistive networks. Here we follow the opposite direction.

120 of the sensors, such that the heat generated in them flows through the sensor into the support structure, the
 121 stave (barrel) or petal (endcap) core with the embedded cooling pipe. In the network model, the heat flow
 122 from these sources is combined and flowing through a common impedance R_M to the sink at a temperature
 123 T_C . For each of the temperature-dependent heat sources (ABC, HCC, FEAST and the sensor) we have added
 124 a resistance from the common temperature T_{mod} to allow for a finite and different heat path for each of them.
 125 Finally, the End-of-substructure (EOS) card adjacent to the last module on the barrel stave (endcap petal)
 126 is modeled as an additional source of heat with an independent impedance for its unique thermal path.

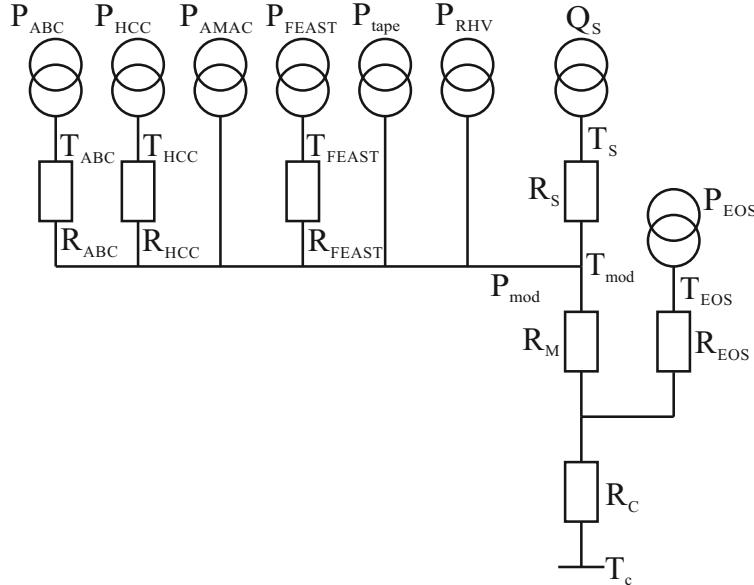


Figure 5: Thermal network model.

127 This is a more complex thermal network than the one studied in Ref. [3], where an analytical solution
 128 for the determination of thermal stability was given. In particular, because of the non-linear temperature
 129 dependence of some of the heat sources, it is not possible in this case to solve the set of equations describing
 130 the model analytically. However, the set of equations is still sufficiently small to solve numerically using
 131 functional programming languages such as Mathematica (used in the barrel model) or Python (used in the
 132 endcap system).

133 4. Obtaining thermal impedances using FEA

134 (*This section should be discussed and agreed between Graham and Yu-Heng*)

135 The cooling path between the sources dissipating electrical power and the cooling fluid is three-dimensional
 136 and includes components with orthotropic thermal conductivity. Hence the prediction of temperature at any
 137 node of the model requires a 3d thermal FEA Ref [Abaqus, Ansys]. However, the thermal conductivities of
 138 the components along the path are approximately constant, so that the temperature rise (above T_C) at any
 139 node of the structure is adequately described by a linear sum of contributions from individual sources, i.e:

$$T_i = T_c + \sum_j a_{ij} Q_j, \quad (2)$$

140 where Q_j is the heat generated at node j . In order to extract the matrix of coefficients a_{ij} , the finite
 141 element model is run with each heat source (or group of similar sources) switched on in turn with a repre-
 142 sentative amount of heat, and the temperature rise noted for each of the nodes of interest, which are those
 143 in the thermal network model (Figure 5).

144 BEGIN ALTERNATE DESCRIPTION

145 Ignoring the EOS components momentarily, the temperature rise $\Delta T_i \equiv T_i - T_c$ of a given node i can be
 146 expressed as:

$$\Delta T_i = R_i P_i + (R_C + R_M) \sum_j P_j, \quad i, j = (\text{ABC, HCC, AMAC, FEAST, tape, RHV, sensor}), \quad (3)$$

147 where the powered components are represented by the index j . In order to extract the coefficients R_i , R_C
 148 and R_M , the finite element model is run multiple times, with each heat source (or group of similar sources)
 149 switched on in turn with a representative amount of heat, and the temperature rise noted for each of the
 150 nodes of interest, which are those in the thermal network model (Figure 5). Using this data from the FEA,
 151 the quantity $R_{CM} \equiv R_C + R_M$ is first solved by focusing on the set of measurements where the measured
 152 temperature node (i) is not associated to the powered component (j). In these cases, the relationship can be
 153 expressed as:

$$\Delta T_i = R_{CM} P_j, \quad (4)$$

154 assuming that only one source j is powered at a time. Each pair of values for delivered power and ΔT is
 155 plotted in Fig. 6. The data is fit to a function of the form $\Delta T = R_{CM} \times P$; the slope of the line corresponds
 156 to the thermal impedance R_{CM} . The remaining thermal impedances (R_{FEAST} , R_{ABC} , etc.) are calculated
 157 by substituting R_{CM} into the equations remaining from Eq. 3. The value R_{EOS} is calculated using a similar
 158 procedure.

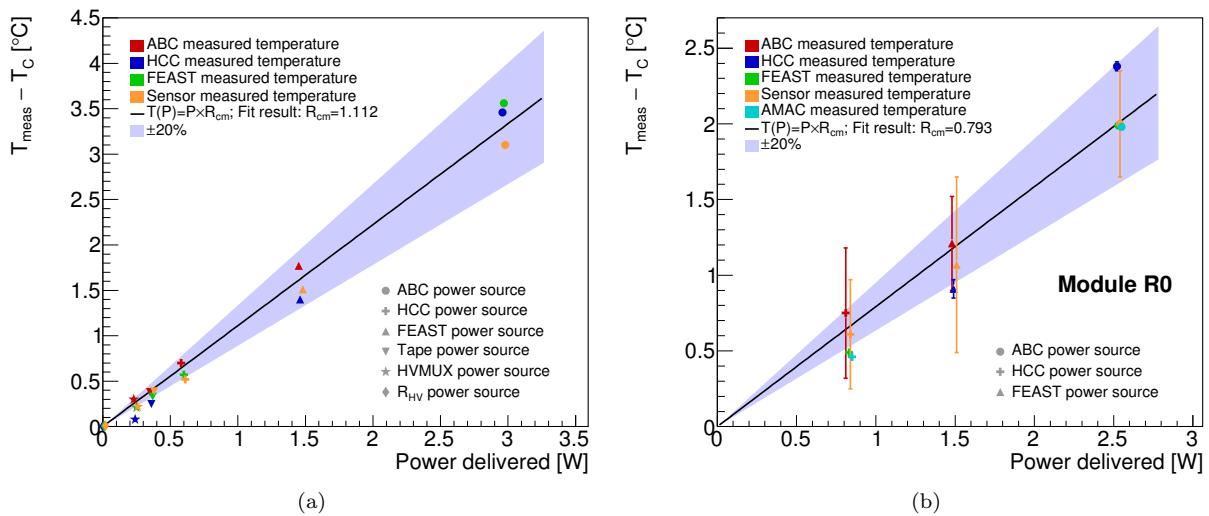


Figure 6: The relationship between the power delivered to each front-end component and the temperature of each component (as estimated by FEA). The slope of the fitted line is the estimate for R_{CM} . (a) The fit for a short-strip barrel module adjacent to the EOS. (b) The fit for the endcap R_0 module. For each data point marker, the source of power is indicated by the shape, and the measured component is indicated by the color. In (b), the error bars represent the standard deviation of temperatures of that particular component, and are not considered in the fit. The blue band represents a $\pm 20\%$ error band on the fit for R_{CM} .

159 END ALTERNATE DESCRIPTION

160 For a barrel module this gives six sets of node temperatures for each source of injected heat. The thermal
 161 impedances in the network are then found from a fit of the linear network to this data. The agreement of
 162 the network temperatures using the thermal impedances from the fit with the data from FEA is better than
 163 0.5°C for all nodes. This procedure is performed for both, the EOS and the normal module. The thermal
 164 impedance from the sensor to the sink ($R_M + T_c$) in all cases is between 1.1 and 1.4°C/W , but higher values
 165 (between 10 and 20°C/W) are found for other impedances in the network (R_{HCC} and R_{FEAST}), mostly
 166 because these are for components with a small footprint constituting a bottleneck for the heat flow.

167 *[Georg has written the paragraph above to explain the fitting procedure but is it confusingly different for
 168 the petals? I dont know how he makes the fit].*

169 There are two recognised departures from linearity of the thermal path: the rise in thermal conductivity
170 of the silicon sensor with decreasing temperature and the rise in heat transfer coefficient (HTC) to the
171 evaporating CO₂ coolant with increasing thermal flux. The FEA models are run using mean values for these
172 quantities appropriate to the operating conditions, and the thermoelectric model results are insensitive to
173 the variations expected in practice.

174 [GAB: Should we expand on this with plots and tables? There are detailed differences between stave and
175 petal that might be confusing, e.g. re coefficients for the sensor T. Maybe all we could addin the end is
176 confusion!].

177 5. Other model inputs

178 The two temperature-dependent elements of the thermoelectric model—the radiation-induced digital cur-
179 rent increase in the front-end chips, and the efficiency of the FEAST DCDC converter—are described in
180 this section. Both effects are studied experimentally and fit with functional forms in order to accurately
181 represent them in the model. The uncertainty in the experimental data, and in our modeling assumptions,
182 are estimated here and considered in the evaluation of safety factors, described in detail in Section 7.2.

183 5.0.1. DCDC converter

184 The DCDC converter (FEAST) supplies a low-voltage (1.5 V) current to the ABC130 and HCC front-
185 end chips on the module. The efficiency of the FEAST depends on its temperature as well as the output
186 (load) current load delivered to the front-end chips. To correctly model the FEAST efficiency, experimental
187 measurements have been performed to characterize the dependence and fitted with a functional form.

188 To measure the FEAST efficiency, the FEAST power board was glued to an aluminum cold plate, cooled
189 with CO₂, and powered with the nominal working input and output voltages (11 V input, 1.5 V output).
190 The temperature of the FEAST was measured with an NTC thermistor and PTAT sensor residing on the
191 FEAST, for a range of load currents up to the maximum design current of 4A³.

192 The data was then fit with a function with sufficient parameters to ensure reasonable agreement; the
193 choice of functional form has no physical interpretation. Figure 7 depicts the FEAST efficiency data and
194 the parameterized fit used in the model. The parameterization fits the data with an accuracy below 1%;
195 this uncertainty in the FEAST efficiency modeling is small compared to other uncertainty sources, and is
196 therefore neglected in our model.

197 5.0.2. Digital current increase of chips using 130 nm CMOS technology

198 The ABC and HCC chips, designed using IBM 130 nm CMOS8RF technology, are known to suffer from an
199 increase in digital current when subjected to a high-radiation environment [1]. This phenomenon, known as
200 the “TID bump,” is well-studied [4, 5] and has a characteristic shape whereby the effect reaches a maximum
201 as a function of the accumulated dose and then gradually diminishes (see Fig. 8).

202 In an effort to characterize the nature of the TID bump in the ABC and HCC chips empirically, many
203 irradiation campaigns have been conducted using a variety of radiation sources, testing the effect at different
204 temperatures and dose rates. The data collected from these studies was used to develop a model of the
205 TID bump that estimates the digital current increase given the total ionizing dose, the dose rate, and the
206 operating temperature of the chip. This parameterization, which is depicted in Fig 8, is used as an input to
207 the thermoelectric model in order to correctly model the ABC and HCC currents. The TID bump is assumed
208 to fully apply to the HCC digital current, and apply to 69% of the ABC digital current (according to our
209 understanding of its digital circuitry).

210 The TID bump displays certain key features, which are reflected in the parameterization: first, the effect
211 is larger at colder temperatures and higher dose rates. This means it can be mitigated by operating the
212 chips at higher temperature (note that the dose rate is fixed by the LHC conditions). Second, the figure
213 also illustrates how chips receiving different dose rates will reach their maximum digital current increase
214 at different times. This feature is particularly important when modeling the total power consumed by the

³ FEAST data spreadsheet: http://project-dcdc.web.cern.ch/project-dcdc/public/Documents/FEASTMod_Datasheet.pdf. Cite?

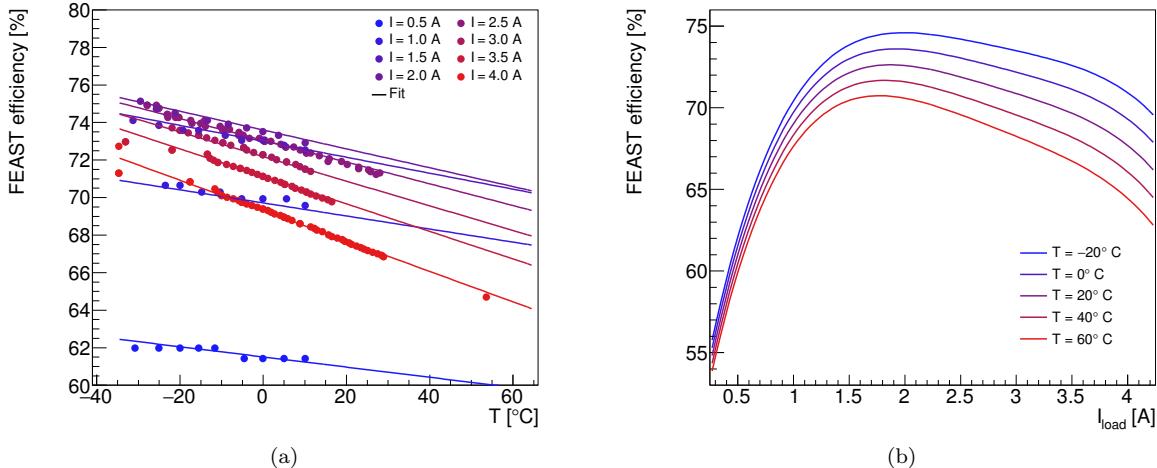


Figure 7: The FEAST efficiency model based on experimental data. (a) The experimental data points characterizing the FEAST efficiency are plotted as dots and color coded for load current. The data is compared to the analytic fit, evaluated in curves of equal current. (b) The same analytic fit, presented as a function of current load for curves of equal temperature.

215 barrel and endcap systems. In both systems, the dose rate varies significantly depending on the position of
 216 the module in the detector. The effect means that the maximum system power will be smaller than the sum
 217 of the maximum power of each module, as each chip reaches its maximum at a different point in time.

218 The TID bump is an important source of uncertainty in our model. The experimental data suggests a
 219 relatively large variation in the TID bump effect, in particular between different batches of the same type
 220 of chip delivered by the manufacturer, suggesting an unknown effect in the fabrication process. To estimate
 221 the uncertainty in the TID bump, the parameterized function is fit again using only the worst-performing
 222 data (defined as having the largest TID bump effect). This “pessimistic” parameterization is used as a safety
 223 factor to estimate the detector performance in worst-case scenarios.

224 The irradiations of individual chips have typically been performed at constant dose rate and temperature.
 225 In our model calculations both of these parameters vary throughout the evaluation. In our parametrization
 226 we use only the instantaneous value of these two parameters, thus neglecting any possible history of the
 227 TID effect. We also ignore any short-time effects due to variations in the dose rate on the scale of hours
 228 or days. This approach is mandated by the lack of more varied experimental data and the absence of a
 229 good theoretical model for this effect. This probably constitutes the largest source of unknown errors for our
 230 model.

231 5.0.3. Radiation-dependent leakage current

232 The radiation-induced leakage current can be parametrized as a function of the hadron fluence expressed
 233 in 1 MeV equivalent neutrons. The parametrizations we have used for the evaluation of our model are shown
 234 in Fig. 9 [ref Marcella Mikestikova]. The currents given there are at a sensor temperature of -15°C and are
 235 scaled in our model to the specific sensor temperature using eq. 1.

236 6. Running the model

237 The thermoelectric model constructs a profile of the sensor module operation conditions over the lifetime
 238 of the detector in the following manner. First, assuming a reasonable set of initial component temperatures,
 239 the module total power (including all components, but excluding the sensor leakage power) and the sensor
 240 temperature without leakage current (T_0) is calculated assuming these initial temperatures. The initial value
 241 for the module power is used to solve for the sensor power and temperature accounting for leakage current,
 242 using the thermal balance equation and the relationship from Eq. 1. Using this calculated sensor leakage

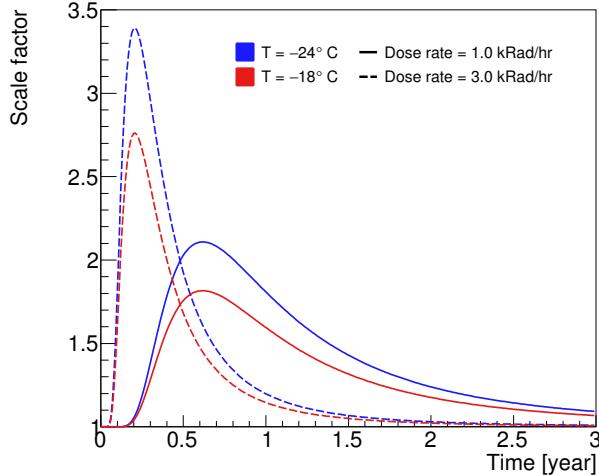


Figure 8: Parametrization of the impact of the total ionizing dose on the magnitude of the front-end chip digital current (the TID bump), presented as a function of time. The current is multiplied by a scale factor that is modeled as a function of total ionizing dose, dose rate, and temperature, based on experimental data.

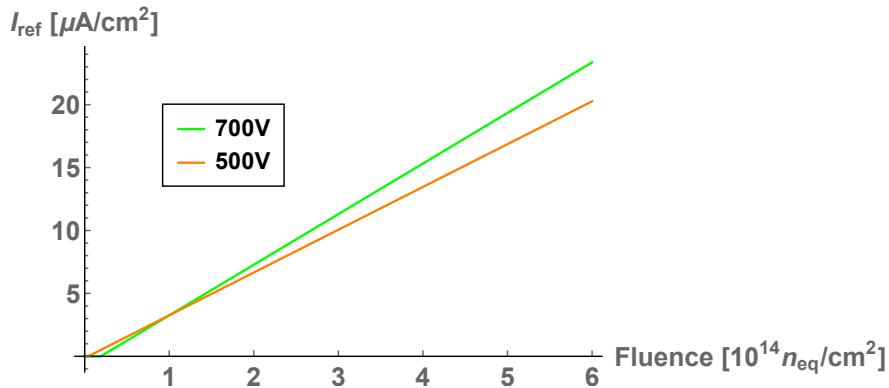


Figure 9: Parametrization used for the leakage current at $-15^\circ C$ as a function of the fluence for two different sensor bias voltages.

243 current and temperature, the power and temperature of the module components are updated given the initial
244 (year 0, month 0) startup parameters.

245 Next, the module conditions of the following month (year 0, month 1) are calculated. Using the component
246 temperatures calculated from the previous month and the operational parameters (ionizing dose and
247 dose rates) from month 1, the module total power (excluding sensor leakage) is again calculated, and sub-
248 sequently the sensor temperature and leakage current are computed. Following this, the module component
249 temperatures and power values are derived for this month. This process is repeated in one-month steps until
250 the final year of operation, or until a real solution for the sensor temperature does not exist, indicating that
251 thermal runaway conditions have been reached.

252 In the barrel subsystem, the above procedure is performed four separate times to represent the radiation
253 conditions of the four barrel layers located at different radii from the beam axis⁴ for both, a module next to
254 the EOS card (hereafter referred to as ‘EOS module’) and a module along the length of the stave away from the
255 EOS card (‘normal module’). Thus in total, 8 modules are simulated for the barrel (4 layers \times normal/EOS),
256 and they are combined in their proper proportion to simulate the entire barrel system.

⁴The correct module type, short-strip in the inner two layers and long-strip for the outer two layers, is used for each layer.

257 In the endcap subsystem, the total ionizing dose and dose rates vary significantly depending on the position
 258 of the module; furthermore, the design of each module on a petal differs significantly. Therefore, all 36 module
 259 types (6 rings \times 6 disks) are simulated independently, and combined to represent the full endcap.

260 We have implemented this algorithm in Mathematica (barrel) and Python (endcaps). In both cases the
 261 calculation for a set of operating conditions over the full lifetime of the LHC takes between 5 and 10 minutes
 262 on a standard PC, thus enabling a quick turn-around for systematic studies of the parameter space.

263 7. Outputs of the thermoelectric model

264 7.1. Operational scenarios

265 To study the different aspects of our predictions for the operation of the ITk strip system throughout
 266 its lifetime, we performed the calculation of the system parameters over the expected 14 years of operation
 267 in monthly steps as outlined in section 6. Time-dependent inputs to the calculations were given from the
 268 expected performance of the LHC (Fig. 10a) and different profiles for the cooling temperature. We studied
 269 flat cooling temperature scenarios at different temperatures starting at -35°C , the lowest evaporation tem-
 270 perature achievable with the ITk evaporative CO_2 cooling system, and a ‘ramp’ scenario in which the cooling
 271 temperature starts at 0°C and gradually is lowered down to -35°C over the course of 10 years (Fig. 10b).

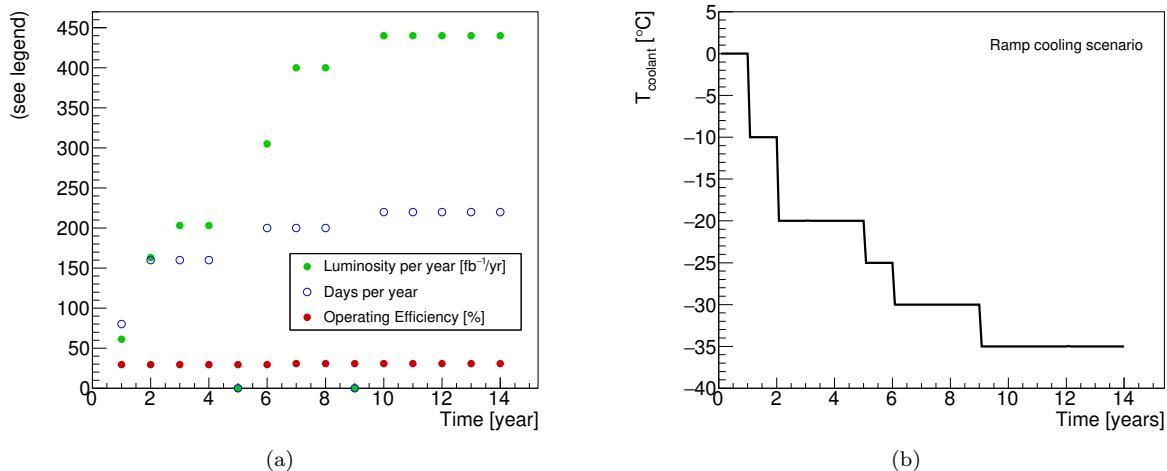


Figure 10: (a) Expected LHC performance and (b) ‘cooling ramp’ scenario for the coolant temperature. Year-long shutdowns of the LHC are anticipated in years 5 and 9.

272 7.2. Safety factors

273 To ensure the robustness of the system design against errors in the assumptions used in the model, we
 274 also evaluate the model using a set of input parameters with some key inputs degraded. The set of safety
 275 factors used is given in Table 1. Each safety factor has been estimated individually based on experience, the
 276 complexity of the system aspect described by the parameter, and from available data or the absence of such
 277 data. Note that the model can be evaluated with all the safety factors listed in Table 1 used together, a
 278 situation which is unlikely to occur in the real system, to provide a worst-case estimate for the performance
 279 of the ITk strip system. The individual effects of the different safety factors are demonstrated in figure 11.

280 7.3. Results

281 The thermo-electrical model provides a large range of predictions for the operation of the strip system.
 282 A detailed discussion of all results would only be of interest to ITk strip system experts and is beyond the
 283 scope of this article. Instead we will present here a subset of results to demonstrate the capabilities and use
 284 of the thermo-electrical model for the design of the detector system.

Table 1: Safety factors.

Safety factor on	Value	Reason
Fluence	50%	Accuracy of fluence calculations and uncertainties in material distributions
Thermal impedance	10% endcap, 20% petal	Local support build tolerances, thermal network assumptions
Digital current	20%	Final chip performance and parametrization of TID effect
Analog current	5%	Final chip performance
Tape electrical impedance	10%	Electrical tape manufacturing tolerances
Bias voltage	700 V	Increased bias voltage from nominal 500 V to maintain S/N
TID parametrization	Nominal/Pessimistic	Different data sets for fit of TID bump

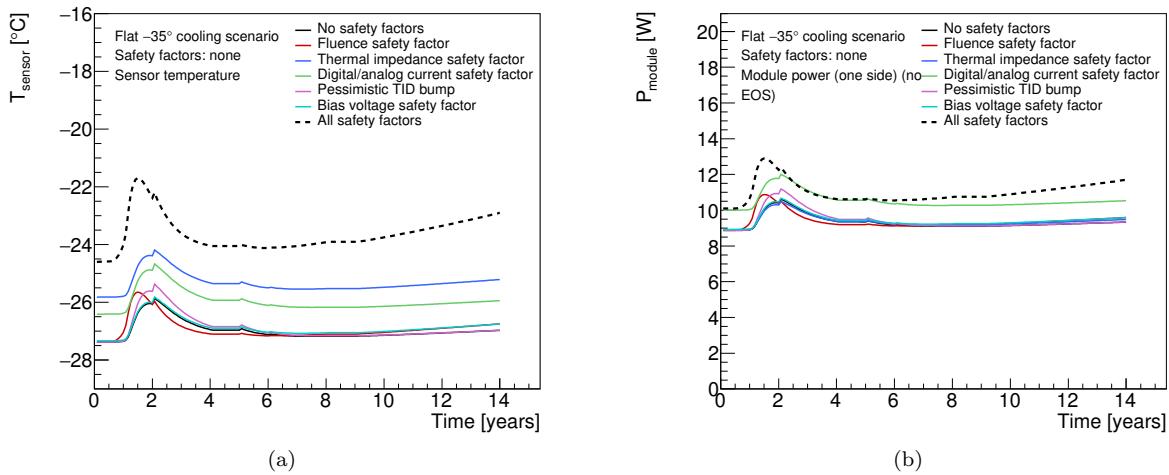


Figure 11: Comparing the impact of different safety factors on (a) the sensor temperature and (b) the module power for the R3 endcap module. The dotted line depicts the effect of all safety factors applied at once.

285 7.3.1. Module properties

286 Example output plots for module properties from the thermo-electrical modules are shown in Figures 12
 287 and 13. The different radiation-dependent effects occur on different times scales. The maximum in the digital
 288 chip power due to the TID effect occurs relatively early (in year 1 to 4), although the bump has a long tail,
 289 particularly in the outer layers of the barrel. The sensor leakage power on the other hand grows towards
 290 the end of the lifetime of the ITk. If the leakage current would continue to increase in the case of further
 291 irradiation, or if the cooling temperature would be higher, this growth would ultimately lead to thermal
 292 runaway. Due to the radial dependence of the radiation environment, the radiation-induced effects are most
 293 pronounced in the innermost layers.

294 7.3.2. System properties

295 One of the key concerns for the design of the strip system is thermal stability of the system. If the cooling
 296 temperature is too high to limit the leakage power from the radiation-damaged sensors to a level where it
 297 can still be removed the system is unstable (it goes into ‘thermal runaway’). In this case there is no solution
 298 to the set of equations in the thermo-electrical model any more and the numerical search for a solution fails.
 299 In the barrel strip system this happens in the last year of operation at a cooling temperature of -15°C under
 300 nominal conditions, and at -25°C (in year 13) with safety factors applied. As the design cooling temperature
 301 of the ITk cooling system is -35°C we have confidence that the ITk strip system has sufficient margin for
 302 thermal stability.

303 Beyond the issue of stability, the thermo-electrical model delivers predictions for the development of

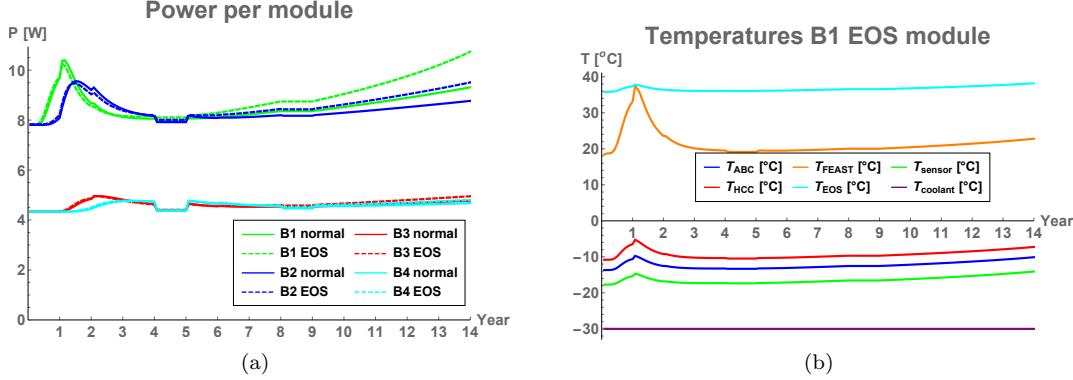


Figure 12: Examples of barrel module performance predictions for a flat cooling scenario (-30°) including safety factors. (a) Power per module. (b) Temperatures for different nodes of an end-of-stave barrel module in the innermost barrel.

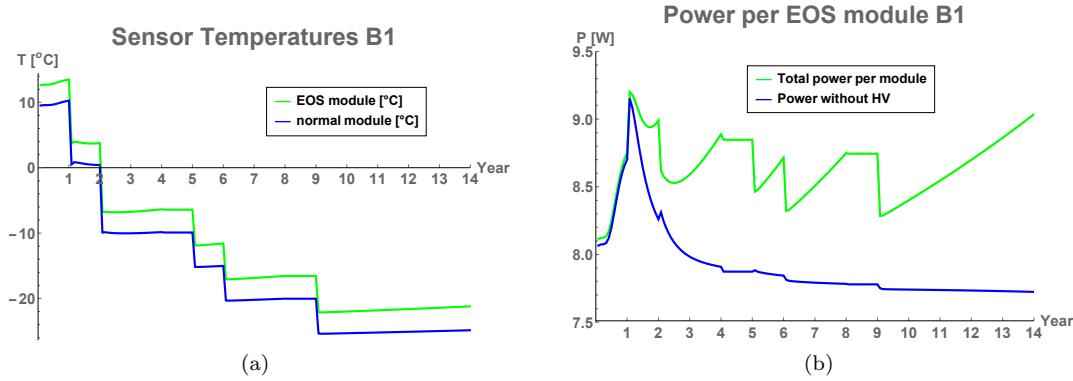


Figure 13: Examples of barrel module performance predictions for the ramp cooling scenario including safety factors. (a) Sensor temperature in the innermost barrel modules. (b) Power in an end-of-stave barrel module in the innermost layer.

304 current and power requirements for the overall system. Some of the predictions are shown in figure 14. Again,
 305 the different timescales of the various radiation-induced effects are visible. Ignoring this time dependence could
 306 lead to overspecification of some system aspects like the total cooling power.

307 These predictions are now used throughout the strip project to consistently size power supply and cooling
 308 systems. Including safety factors in the predictions gives us some confidence that the designs are robust and
 309 by using commonly agreed safety factors we ensure a consistent use of safety factors throughout the project
 310 and prevent safety factor creep.

311 Because of the different timescales for the peak power due to the TID effect and the sensor leakage due
 312 to radiation there is room for the optimization of the cooling temperature profile for minimal power. The
 313 thermo-electrical model is a powerful tool to plan such an optimized cooling profile. In fact, the cooling
 314 ‘ramp’ scenario introduced in Section 7.1 is the result of such an optimization (Fig. 15).

315 8. Model performance verification

316 The quality of the predictions of the thermo-electrical model is affected by two major factors: First, there
 317 is the quality of the input parameters, and second there are errors introduced by reducing the complex 3D
 318 geometry into a linear thermal impedance network. The former have been discussed throughout this paper
 319 where the different inputs have been presented. For the latter we have studied the agreement of predictions
 320 from the network model with the more accurate results obtained from FEA for selected states of the system.

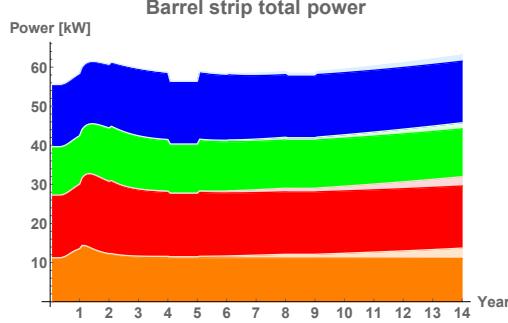


Figure 14: Examples for system performance predictions. Barrel total power requirements for flat -30° cooling including safety factors (left): The plot shows the stacked power requirements for the four barrels (orange: innermost barrel, blue: outermost barrel). Full colour indicates power from the front-end electronics, greyed parts are contributions from HV power for the four barrels.

321 For the verification of this agreement we have calculated the sensor temperature curve for a barrel end-
 322 of-stave module up to thermal runaway. For this we do not vary any of the input parameters in the model
 323 other than the sensor leakage power. We therefore can reduce the complex thermal network to its Thevenin
 324 equivalent, which is identical to the network studied in Ref. [3] and we can use the analytical expressions
 325 given there. The comparison of this prediction is shown in Fig. 16. Despite a large temperature variation
 326 of about 15°C across the sensor, which is caused by heat flux from the end-of-structure card and degraded
 327 thermal impedance at the end of the stave due to ceramic sections in the cooling pipe, the network model
 328 predicts the runaway within 1°C of the result from the FEA⁵. This agreement gives us confidence that the use
 329 of a thermal network model is not likely to significantly degrade the predictions beyond the errors introduced
 330 by other inputs to the model.

331 9. Conclusions

332 We have developed a model of the ATLAS ITk strip system which is based on the interplay between a
 333 thermal and an electrical network model. The set of equations in the model can be numerically solved using
 334 standard data analysis software in short time, allowing for a quick turn-around for systematic studies of the
 335 system performance. The complexity of these networks is given by the number of interconnected components
 336 between the networks which have a non-linear dependence on the temperature or electrical power. This
 337 approach could easily be adopted for any other silicon detector system.

338 In the case of the ATLAS strip system several temperature-dependent heat sources had to be included.
 339 In addition to the sensor leakage current these are the radiation-induced increase of the digital front-end
 340 power ('TID bump') and the efficiency of the DC/DC conversion system. The outputs of the model give us
 341 confidence that the ITk strip system will be thermally stable until the end of LHC phase II operation even if
 342 safety factors on key inputs are included. The model furthermore provides information for benchmark system
 343 parameters like cooling and supply power and currents in power cables, which is used in the specification of
 344 these systems. The use of the model outputs throughout the strip project ensures consistent specifications,
 345 including a common strategy on safety factors. Using the thermo-electrical model we can also propose an
 346 optimized cooling temperature 'ramp' scenario, which equalizes leakage power throughout the lifetime of the
 347 experiment while minimizing the TID bump.

348 We have verified the performance of the thermal network model compared to full FEA and are confident
 349 that the agreement is sufficient that the overall accuracy of the model is dominated by other inputs to the

⁵Ref. [3] is not clear about the exact definition of the sensor temperature to be used for the calculation of the thermal impedance. In fact, at the time we were still using the maximum sensor temperature for this. Since then we have acquired more experience with thermal network models and found that the best agreement can be achieved if the average sensor temperature is used.

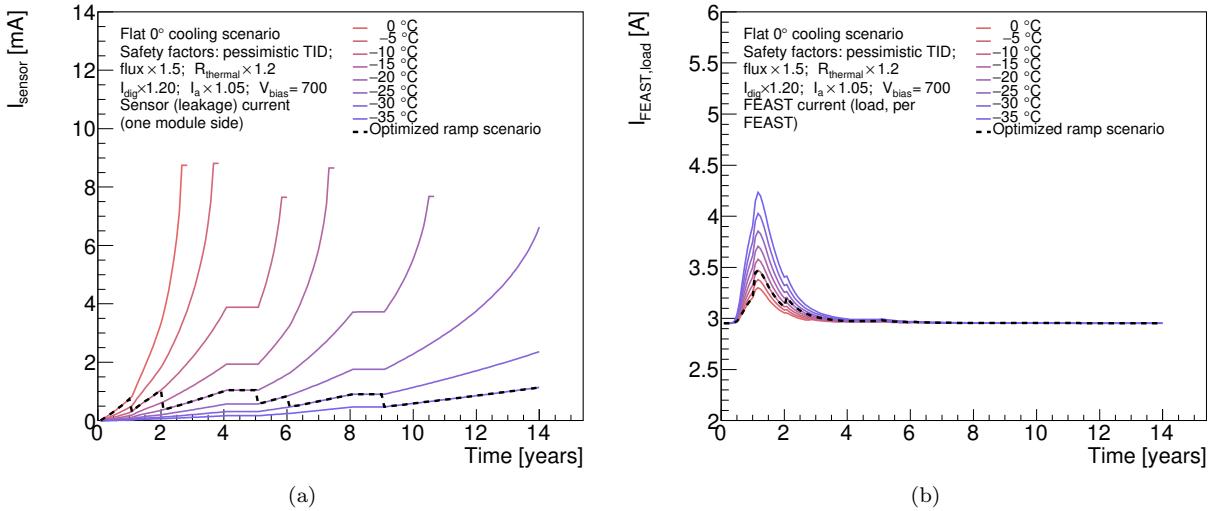


Figure 15: Performance of the cooling ‘ramp’ scenario specified in Fig. 10b. The dashed lines represents the ramp scenario, which has been selected so that the sensor leakage current (a) is stable throughout the lifetime of the ITk. A higher coolant temperature in the first few years reduces the TID effect, keeping the current load on the FEAST (b) well below its specified maximum of 4 A.

350 model, of which the most likely source of unknown error are limitations in the parametrization of the TID
 351 effect available for the model.

352 10. Acknowledgements

353 The evaluation of the thermo-electrical model depends critically on the input parameters to the model. To
 354 capture the whole of the system these need to distill all what is known of the system, and we are therefore
 355 indebted to the whole of the ITk strip community. In particular we would like to thank Tony Affolder, Kyle
 356 Cormier, Ian Dawson, Sergio Diez Cornell, Laura Gonella, Ashley Greenall, Alex Grillo, Paul Keener, Steve
 357 McMahon, Paul Miyagawa, Craig Sawyer, Francis Ward and Tony Weidberg for all their inputs to this work.

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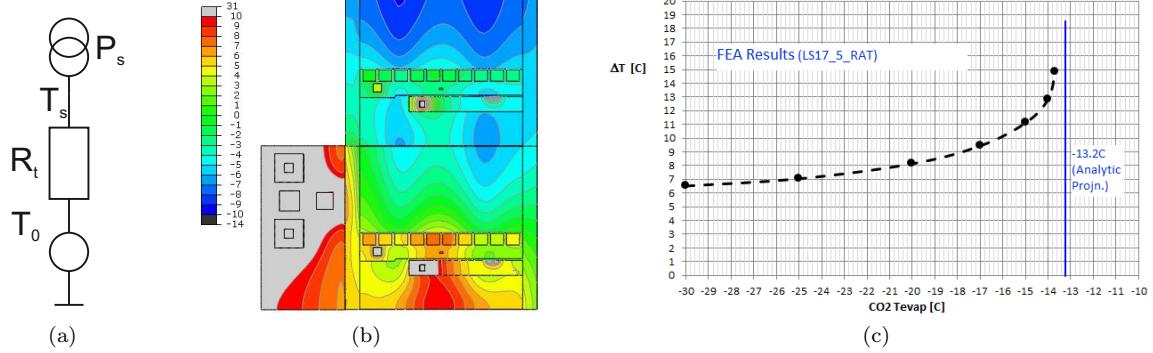


Figure 16: (a) Thevenin equivalent of the thermal network. (b) Result of surface temperature calculations using FEA. (c) Average temperature above cooling, comparing FEA (dots) and the network model prediction (dotted line).