Thermoelectric modeling of the ATLAS ITk Strip Detector

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Abstract

Here is the abstract.

Keywords: Silicon detector, Thermal runaway, Thermal management, Cooling

1. Introduction

The temperatures in silicon detector systems are critically important to the performance of these systems. The leakage current shows a pronounced temperature dependence

$$I \propto T_{\mathrm{S}}^2 e^{-T_{\mathrm{A}}/T_{\mathrm{S}}} \tag{1}$$

where T_{S} is the sensor temperature and $T_{\mathrm{A}} \simeq 7000$ K. Leakage currents can become particularly significant after irradiation of the silicon material. The heat generated by these leakage currents in the silicon sensor, together with the heat from front-end electronics components on the detector needs to be removed by cooling systems. Due to the strong growth of leakage power with temperature there is a critical temperature T_{C}, above which the heat cannot be removed quickly enough, and the detector becomes thermally unstable ('thermal runaway'). The capability of the cooling system in removing this heat is limited by the temperature of the local cold sink (typically the coolant temperature) and the thermal impedance of the heat path between the source (electronics and sensor) and the sink.

In addition, there can be aspects of the front-end electronics which are temperature-dependent. For example, in the strip system for the ATLAS phase II upgrade (ref) there are two additional sources for temperature-dependent heat sources. The first is a radiation damage effect in the digital part of the readout-electronics (the ABC130 and HCC chips), which is manufactured in 130 nm technology by the xxx process (ref). This effect leads to a scaling of the digital power in the chip depending on the received dose rate (TID) and the temperature of the chip (ref). This has been first observed in the ATLAS IBL (ref). The other temperature dependence of the power generated by the front-end electronics stems from the temperature dependence of the converter chip (FEAST (ref)) used in the on-detector DC-DC converter system supplying power to the front-end electronics.

Even before the limit of thermal stability is reached, knowledge of temperatures in silicon detector systems is important, as they define system parameters like power supply capacity and cable dimensions.

In principle the temperatures in the system for a given set of operational parameters (power density, thermal conductivities etc.) can be predicted by FEA to an accuracy which is given by the quality of the input parameters. However, this is a time-consuming process and can be prohibitively difficult if there is a large number of local heat sources depending non-linearly on the temperature. A simplification to this problem which allows for an analytical solution in the case of a simple heat source topology has been developed in [1]. In this paper we develop this method further to include several temperature dependent non-linear heat sources in the front-end electronics. The resulting set of equations cannot be solved analytically any more, but with little effort using numerical problem solvers. This enables us to predict with some confidence the temperatures and power requirements in the ATLAS strip system throughout phase II operation. The results from this prediction have been used throughout the project to consistently dimension the different systems (cooling, power, services etc.) also with some robustness due to the inclusion of a common set of safety factors. This method can be easily adapted to any other system after adjustment of the system specific geometries and parameters.

1.1. The ATLAS strip system

The strip system for the ATLAS phase II upgrade (ref TDR) consists of two parts: the barrel system comprised of four concentric cylindrical barrels and the two endcaps, which consist of nine disks each.

In the barrel the detector modules are made of square sensors (96.85×96.72 mm^2) with a hybrid on top, which hosts the front-end chips (ABC* and HCC*), but also circuitry to convert the supply voltage of larger than 10 V to the chip voltage of 1.5 V. This circuitry is controlled by the FEAST chip. The modules are glued onto both sides of a composite sandwich which contains two parallel thin wall titanium cooling pipes embedded in carbon foam (Allcomp K9 - ref) between two facesheets of UHM carbon fibre (3 layers of K13C2U/EX1515) with a co-cured Kapton/copper low-mass tape. A model of this geometry is shown in fig. 1. During final operation cooling will be achieved by evaporating CO_2 in the cooling pipes with a final target temperature of not higher than -35°C anywhere on the stave. With the exception of the end region of the stave, where a side-mounted End-Of-Structure (EOS) card is located and the thermal path is degraded by the presence of electrically insulating ceramic pipe sections, the geometry of the stave is uniform along its length.

Something on EC geometry.

1.2. Radiation environment

2. The electrical model

(Include network models of electrical components.)

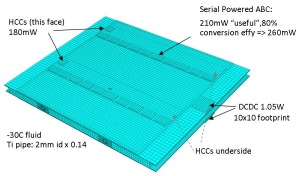

Figure 1: Barrel strip geometry

3. The thermal model

The thermal network consists of heat sources (some of which are temperature dependent) and thermal resistances. The latter are given by the properties of the mechanical design (heat conductivities of the materials) and the geometry of the heat path. The geometry is generally 3-dimensional, but it is the strategy of the simple network models to lump the 3-dimensional behaviour into one thermal resistance parameter. In the models discussed here we have used a granularity corresponding to single detector modules for which the thermal resistance has been modelled. The temperatures in the model are then given for the nodes in the network in analogy to the potentials in an electrical network.

The complexity of the thermal network used in this study (see figure 2) is given by the variety of different temperature-dependent heat sources in the ATLAS strip system. In addition to the sensor leakage currents these are the digital power for each type of chip, and the heat generated by the FEAST chip, which is providing the DC-DC conversion on the detector. In the ATLAS SCT modules all these components are located on top of the sensors, so that the heat generated in them flows through the sensor into the support structure, the stave (barrel) or petal (endcap) core with the embedded cooling pipe. In the network model the heat flow from these sources is combined and flowing through a common impedance R_{M} to the sink at a temperature T_{C}. For each of the temperature-dependent heat sources (ABC, HCC, FEAST and the sensor) we have added a resistance from the common temperature T_{mod} to allow for a finite and different heat path for each if them. Finally, in the case of the barrel system, there is an additional source of heat for the last module on the stave, which is the adjacent End-of-substructure (EOS) card, which is modeled by an additional source with an impedance for its special heat path.

This is a more complex thermal network than the one studied in ref. [1], where an analytical solution for the determination of thermal stability was given. In particular because of the non-linear temperature dependence of some of the heat sources it is not possible any more to solve the set of equations describing the model here analytically. However, the set of equations is still sufficiently small to solve it numerically using readily available functions in Mathematica (used in the barrel model) or xxx (used in the endcap system).

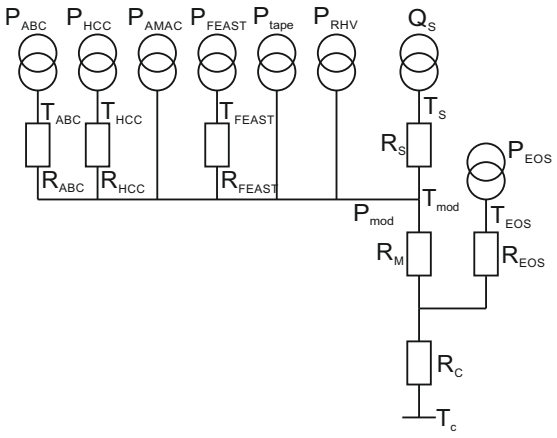

Figure 2: Thermal network model.

4. Obtaining thermal impedances using FEA

Explain the method of extracting impedances of thermal pathways using FEA.

5. Other model inputs

Explain the specific challenges in the strip detector that are parameterized and modeled in our case.

5.0.1. DCDC converter

5.0.2. Digital current increase of chips using 130 nm CMOS technology

5.0.3. Modeling flux and total ionizing dose in endcap modules

6. Outputs of the thermal model

(Specifications using safety factor scenarios. Specifications for modules, global sytem requirements. Qualitative understanding of system properties and evolution.)

7. Model performance verification

8. Conclusions

(Conclusions.)

9. Acknowledgements

(Acknowledgements.)

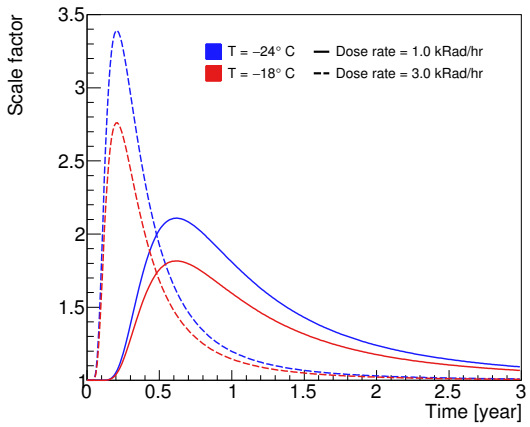

Figure 3: Parameterization of the impact of the total ionizing dose on the magnitude of the front-end chip digital current. The current is multiplied by a scale factor that is modeled as a function of dose rate and temperature, based on experimental data.

References

[1] G. Beck, G. Viehhauser, Analytic model of thermal runaway in silicon detectors, Nucl. Instrum. Meth. A618 (2010) 131–138. doi:10.1016/j.nima.2010.02.264.