Performance Analysis of XY Routing Algorithm Using 2-D Mesh ($M \times N$) Topology

by

Tahir Khan
B.Sc Electronics Engineering, Comsats Institute of Science and Technology, 2011

A Master's Project Submitted in Partial Fulfillment of the
Requirements for the Degree of

MASTER OF ENGINEERING

in the Department of Electrical and Computer Engineering

Performance Analysis of XY Routing Algorithm Using 2-D Mesh ($M \times N$) Topology

by

Tahir Khan
B.Sc Electronics Engineering, Comsats Institute of Science and Technology, 2011

Supervisory Committee

Dr. Fayez Gebali, Supervisor
(Department of Electrical and Computer Engineering)

Dr. Samer Moein, Department Member
(Department of Electrical and Computer Engineering)

ABSTRACT

Network-on-Chip (NoC) has been proposed as a scalable and flexible interconnect infrastructure for communication among hundreds of intellectual property (IP), computational and memory blocks on a core-based System on Chip (SoC). NoC has tackled the disadvantages of SoCs. In NoC topology, the performance is heavily depends on the underlying routing techniques. The packet routing is one of the major factors in the design of network-on-chip architecture. In this report, we have implemented XY routing algorithm in 2-D mesh topology on different network sizes using Matlab simulation. In the first chapter of this report the fundamentals of NoCs is explained which includes why we should use NoC. The next part of the report covers the basic building blocks of NoC architecture. The final part deals with the implementation and evaluation of XY routing algorithm in 2-D (4×4) mesh and (8×8) network topologies.

Contents

List of Figures

List of Acronyms

Acronym	**Definition**
2D	Two-Dimensional
3D	Three-Dimensional
CMOS	Complementary Metal-Oxide-Semiconductor
DSP	Digital Signal Processing
FIFO	First-In-First-Out
IP	Intellectual Property
IC	Integrated Circuit
I/O	Input-Output
NI	Network Interface
OSI	Open System Interconnection
SoC	Systems-on-Chip
VLSI	Very Large Scale Integration

ACKNOWLEDGEMENTS

All praises belong to Allah the merciful for his guidance and blessings

My Beloved Parents, who always supported me on every step of my life.

My Supervisor Prof. Dr. Fayez Gebali for their support and mentoring throughout degree.

Friends, who always encouraged me where it was really difficult to move forward.

Department of Electrical Engineering, whose friendly support and guidance made it possible.

Your education is a dress rehearsal for a life that is yours to lead.
Nora Ephron

DEDICATION

To my father **Habibullah** and my **Mother** whose life has been a perfect example for me.

Chapter 1

Introduction

With very large scale integration (VLSI) technology, a single silicon chip has been fabricated with millions of transistors in the recent years. The latest CMOS technology approximately one billion transistors can be designed on a single chip. This progress in fabrication extends to integrate several processing system on a single integrated circuit to carry out a complete system on a chip (SoC). SoC compose of interconnected Intellectual Property (IP) blocks which can be general purpose processor, a memory block, a specific application, a digital signal processing unit, an input-out controller, a mixed signal module etc. as in Figure 1.1.

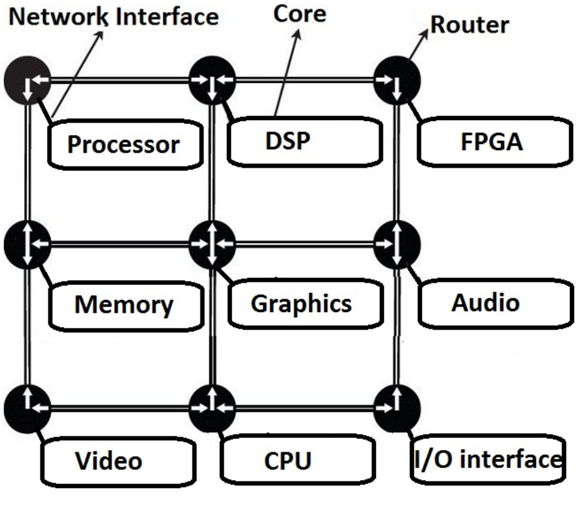

Figure 1.1: SoC based NoC communication infrastructure

Direct interconnections and normally shared busses is designed for on-chip communication [5]. Shared buses and direct interconnections are not scalable and inefficient for a very large number of IP cores only suitable for low communication. The traditional buses cannot meet the required bandwidth, latency and power demands for many application systems. A shared bus is a set of wires common to multiple cores. The busses permit only one communication operation at a time. Thus, all cores share the same communication bandwidth in the system and scalability is limited to a few Intellectual Property (IP) cores as shown in Figure 1.2.

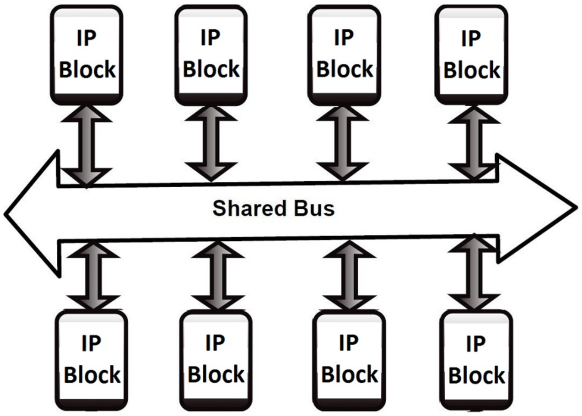

Figure 1.2: Shared Bus

To integrate a large number of IP cores, a new design method, other than Shared busses and direct interconnections is needed for communication among the IP cores. NoC has been brought in as a new approach to solve System on chip design challenges. In core based SoC design it is viewed the most suited nominee for carrying out interconnections [12]. Network-on-chip architecture has emerged as a dominating paradigm and efficient alternative to the bus based architecture. NoC has been proposed as a scalable and flexible interconnect infrastructure for communication among hundreds of (IP cores) computational and memory blocks on a core-based System on Chip. Packet-switched communication is used in the interconnected IP cores through network routers [16]. To analyze the performance characteristics of NoC network, in this project Matlab Simulation is used to evaluate the performance of 2-D mesh m×n architecture, using XY routing algorithm.

Chapter 2

Network-on-chip

2.1 NoC Architecure

The NoC comprise of Routers, network interface (NI), IPs and links are the main elements of NoC architecture as depicts these components for (4×4) Mesh topology in Figure 2.1 [2]. The way in which the Router, NI, IP and link are connected provide different network topologies i.e. Mesh Network, Torus Network, Fat tree Network, Butterfly Network etc. The most important features of NoC architecture are routing algorithm, network topology, and switching techniques. Same as the other networks; router is the most important element in SoC based on NoC architecture. The entire chip is connected together by communication links and NoC Router forwards the incoming packets either to destination core or to next router in the routing path from the source to destination.

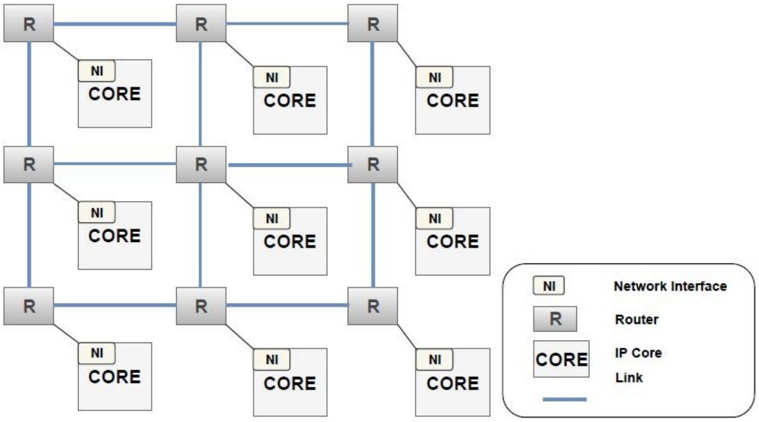

Figure 2.1: 2-D Mesh NoC Architecture

Network Interfaces connect the IP cores to the on-chip routers network. NI in NoC is a medium between the computational part and communication infrastructure. Network Interfaces exchange the data generated by the IP blocks into data packets and place extra routing information based on the underlying NoC network. NoC Routers are the main source of routing packets in communication network. The routers direct packets onto the right link to reach their proposed destination. A brief description of each of these NoC components is given bellow.

2.1.1 Router

A router is the most crucial element in NoC architecture [15]. It is the communication backbone of a Network-on-chip system. The router gives direction to network traffic from source to destination. It aligns the data flow which is very important in communication networks. The architecture of the router consist of five buffers i.e. north, south, east, west and local buffer as in Figure 2.2.

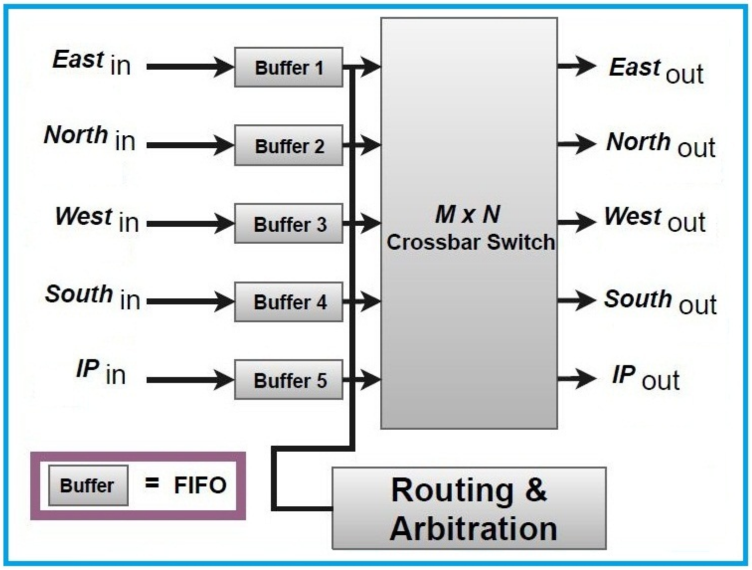

Figure 2.2: 2-D Mesh Router

The first four ports are used to connect to other routers in the network and the local buffer is used to connect the Intellectual Property (IP) core. Routers are intelligent devices that receive incoming packets, examine their destination and search out the best route to proceed packets from the source node to destination node [13]. A router reads the information provided by the incoming message based on the routing function and destination of the packet. The NoC router is built according to the OSI model. Each OSI layer has its own particular functions to perform.

2.1.2 Network Interface

The network interface (NI) makes the logical connection between the IP core and the network. The network interface is the interface between IP core and router. NI observes packets transmission and reception of a packet from and to the IP core. Network interface supports full duplex communication. Initially, it gathers data from IP core then packetizes, add a destination address to the packet and forward the packets to the router, then it receives packet from the associated routers and depacketizes, send the packets to a destination.

2.1.3 Links

Links connect two routers to the network and transmit packets between them. It consists of a set of wires and may have one or more physical channels and each channel is composed using a set of wires. Long links cause wiring delay in the network. To overcome such problem the NoC pipelines long wires in NoC by partitioning the wires into smaller segments [3].

2.1.4 Network Topology

NoC topology means how the Router, IP Core, NI, and Links are connected. In designing a NoC, the major step is to select a topology as the other functions such as bandwidth, latency, flow control and routing strategy mostly depend on topology [8]. Topology assists in checking the number of hops (or node) a message must traverse and also interconnect lengths between hops, which has a substantial influence on network latency. Network topologies provide different path over which packet travels from Source node to destination node. NoC topologies have two types regular and irregular topologies. Some of the standard NoC topologies are discussed below.

2.1.5 Mesh Topology

Mesh is a regular network topology. This network topology consists of n number of rows and m number of columns. Each router in a mesh topology is connected to the adjacent router through interconnection of wires. The address of the router and IP cores are described by (x, y) co-ordinates of the network. In Mesh Topology faults can be easily detected and faulty nodes can be avoided during routing a packet in the network. This is the simplest topology to implement among other topologies. In this topology, packets go through a committed link and the packets will only reach its proposed addresses. Figure 2.3 shows a (3×3) Mesh network.

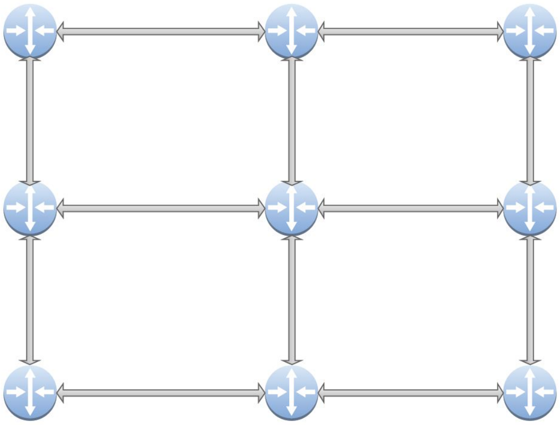

Figure 2.3: Mesh Topology

2.1.6 Torus Topology

It is also a regular network topology and improved version of mesh topology. Unlike Mesh topology the end nodes of a column are connected and the end nodes of a row are connected. This topology has some goods above mesh topology i.e. torus topology has better route variety than mesh and it has more possible minimal routes than mesh topology. Torus design is also simple [14]. Torus topology is shown in Figure 2.4.

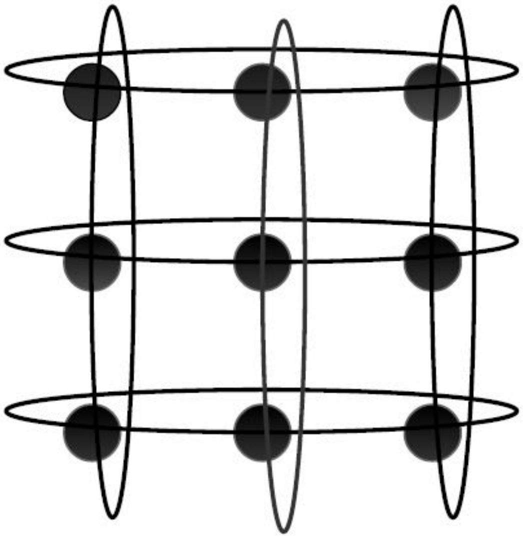

Figure 2.4: Torus Topology

2.1.7 Fat-Tree topology

Fat-Tree Topology is irregular network topology in a tree like structure. In the fat-tree, there is a root node, which is consists of some branches and those branch nodes are called child nodes. The total count of links in fat-tree topology going down to its child leaves is the same count of links going up to its root node [1]. This topology is shown in Figure 2.5.

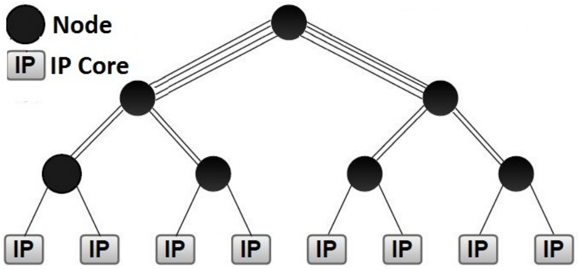

Figure 2.5: Fat-Tree Topology

2.1.8 Ring topology

In this kind of topology, each node in the network has connections with two other adjacent nodes also the first and last node are connected to make a ring. The data packets pass through every node in the network until they find the destination node [11].

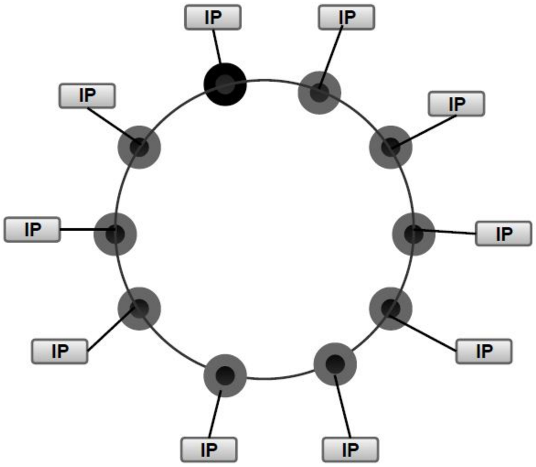

Figure 2.6: Ring Topology

Chapter 3

Routing Algorithms

3.1 Routing Algorithms in Network-on-chip

Routing algorithms play a vital role in communication performance of a network-on-chip. Routing algorithms are used to determine which path a packet will take to reach the concerned destination node [18]. Several kinds of routing techniques have been proposed in NoC, which may be categorized based on their characteristics and conditions. Based on the position where routing choice is made it may be classified as a source, distributed and centralized routing algorithm. In the case of centralized algorithm, the central controller chooses the path. In source routing, source router select path prior to sending packet, while in distributed routing the routing path is chosen by intermediary routers. Most commonly used NoC routing techniques are categorized below.

- Deterministic vs. Adaptive Routing
- Source vs. Distributed Routing

3.1.1 Deterministic vs. Adaptive Routing

In deterministic routing algorithms, the complete path between source nodes to the destination node is computed in advance by using the source and destination addresses without looking to the network conditions. Deterministic routing algorithms only decide defined paths whereas multiple routes are possible in adaptive routing algorithms. In adaptive algorithm network load, traffic condition and information about available output ports are always taken into account. Adaptive routing algorithms can result in deadlocks and livelocks situation [7].

3.1.2 Source Vs. Distributed Routing

In source routing, all the routing information is stored in the packet header. The path information cannot be changed because all the packets contain the entire path information. In distributed routing, a router either computes the output port dynamically by running a routing algorithm or chooses the output port by using the routing table that is stored in the router. Distributed routing considers dynamic network conditions to compute or select the path [7].

3.1.3 Deadlock

Two or more packets in the NoC network mutually block one another and expect for resources and there is no chance be free this situation is called deadlock. In this case, all packets will be withheld inside the deadlock situation and the packets can not be moved to reached their destination and results a big loss in the NoC. It is depicted in Figure 3.1. The packet P0 wants to progress to *D* but the resource is occupied by P2, similarly P2 is blocked by P3 and can not make progress. The packet P3 is blocked by P1 and P1 is blocked by P0, this situation is called deadlock.

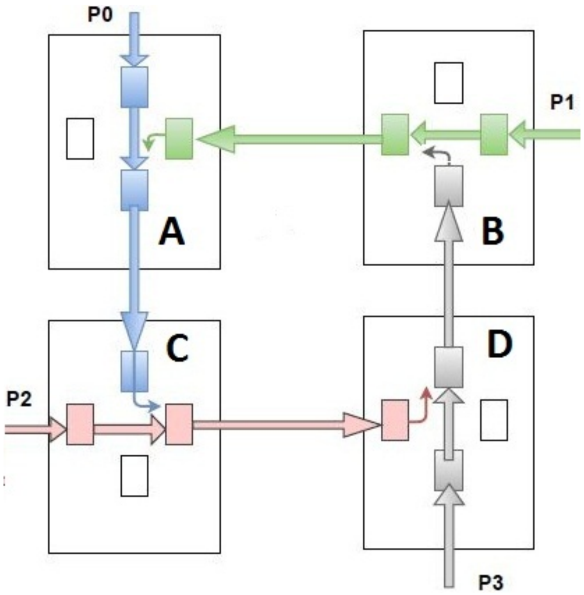

Figure 3.1: Deadlock

3.1.4 Livelock

Livelock problem happens when the packets are moving around a destination without reaching there. This way packet can't be routed to the destination. For throughput improvement, this kind of situations should be avoided.

3.1.5 Starvation

In this situation, a packet has no chance to gets a resource because of different priority assignment to the packets. So high priority data packets can reach their destination easily but the low priority packets will never reach their destination.

Routing Algorithm in NoC is the main factor which affects the communication efficiency. Routing techniques decide the path a packet will take to reach its destination from the source node, it is a key job in the network layer design of NoC [10]. NoC Routing is bit analogous to any network routing; the routing algorithm decides how to route the data packet in the shortest and possible way [4][17].

3.2 XY-Routing Algorithm for 2-D Mesh

The XY routing algorithm is simple in implementation and most common routing algorithm that is proposed by Wang Zhang and Ligang Hou used in NoC [19]. This routing technique comes under distributed deterministic routing algorithm. XY routing never runs into deadlock or livelock [9]. The XY routing algorithm generally follows the shortest path and the only one determined path for the packet. This algorithm is suitable for regular and irregular network topologies. In order to understand XY-routing, we consider the two-dimensional $n \times m$ Mesh as in Figure 3.2. To identify each node, in this mesh has a location in the form of (x, y) where x represents its position in the x-dimension and y represents its position in the y-dimension.

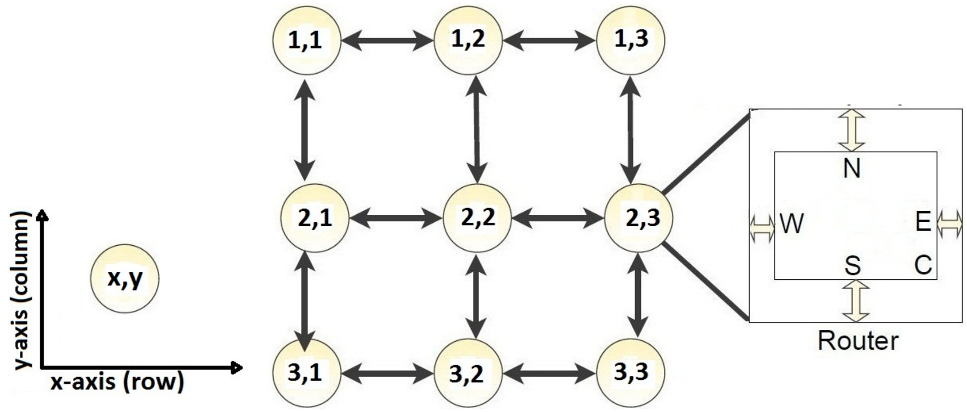

Figure 3.2: A 2-D (3×3) Mesh Topology

The route from the source node to the destination node is a determined path, no matter what the conditions of the network. When the NoC network has no congestion, it has a high reliability and short delay.

This algorithm states that "First the packet will move in X-direction and then in Y-direction", packets cannot use alternative routes to bypass the blocked routes. The (x, y) coordinate of the current router is compared to the (x, y) coordinate of destination router to compute the path [19]. The data packet is routed firstly along the X-dimension and then along the Y-dimension until the packet reaches its destination IP core in it.

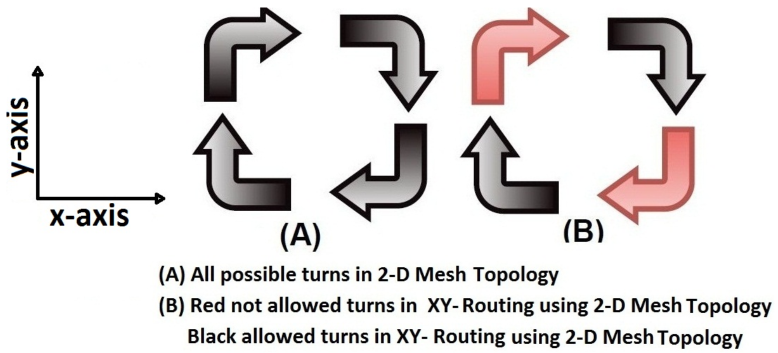
y-axis
x-axis
(A)
(B)
(A) All possible turns in 2-D Mesh Topology
(B) Red not allowed turns in XY- Routing using 2-D Mesh Topology
Black allowed turns in XY- Routing using 2-D Mesh Topology

Figure 3.3: (a) All possible turns in 2-D Mesh Topology (b) Allowed turns in XY-Routing

Out of eight possible turns in Mesh topology, XY routing algorithm permit half the turns by restraining rest of the half turns. According to XY routing a packet will first move in x-direction after reaching the destination column it will be moved along y-direction (up or down) as shown in Figure 3.3.

3.2.1 XY Routing Algorithm Pseudo-code for 2-D Mesh NoC

Algorithm 1 XY Routing Algorithm for 2-Dimensional Mesh NoCs

```
Inputs: Coordinates of source node ($Xsource, Ysource$),
destination node ($Xdest, Ydest$),
Output: Selected output Channel
Begin
Xoffset := Xdest-Xsource; Yoffset :=Ydest-Ysource;
if (Xoffset=0) and (Yoffset=0) then
  return
else
  if (Yoffset >0) then
    return $Y+$;
  end if
  if (Yoffset <0) then
    return $Y-$;
    if (Xoffset >0) then
      return $X+$;
    end if
    if (Xoffset <0) then
      return $X-$;
    end if
  end if
end if
```

In XY routing algorithm, if the Yoffset is greater than zero, then the packet is routed to the right (west buffer). If the value is less than zero, then moved to left (east buffer). However, if the Xoffset is not zero, then packet routed up or down along y-axis. In case, when Yoffset and Xoffset is equal to zero it means that the packet is reached its destination.

The route is always the shortest and identical between the source node and destination node. This technique has low latency at low network traffic due to its static, but the performance decreases rapidly due to congestion and lacking path variety. It is more beneficial than other NoC routing algorithms under consistent traffic pattern. The load in XY routing algorithm network is much higher in the center rather than total average and this results to a hotspot in the center of the network. If a faulty node is located on the route the packet will remain blocked in one of the switches.

Chapter 4

Simulation and Results

In this chapter, we present the experimental works to evaluate the performance of XY routing algorithm for different network sizes based on 2-D mesh topology. The quality of XY routing algorithm in terms of throughput, node throughput, latency, efficiency and packet lost is investigated, and calculated expected successful results.

4.1 NoC Simulation Operation

The Matlab script provides six major events during simulation: node generation, network topology, network size, packet generation, routing algorithm, and results. The routing Algorithm is simulated based on a 2-D Mesh topology. The network size we used to compare is (4×4) and (8×8) mesh.

The Matlab script generates nodes according to the network size (4×4) or (8×8) and also assigns Cartesian coordinates (x-dimension, y-dimension) to each node. Each node consists of five buffers (West, East, North, South, and Core). The IP Core is linked to the router and the router is connected to neighbor routers by four channels (West, East, North, and South). Every node in the network is named by a set of x-coordinate and y-coordinate. We are using Store and forward switching technique, in which packets move throughout the network as a whole. The entire packet is obtained and stored in the buffers of the router before being forwarded to the next node. The buffers are First-In-First-Out (FIFO) queue; FIFO is the most direct and simplest way of implementation where incoming packets are stored in one queue. Where the first input packet is stored in the head of the queue and the second is stored at the second place until the last packet which is stored at the tail of the buffer.

The simulation time is a 500-time step with a uniform traffic. The maximum number of packets generated during simulation is (simulation time × number of rows in mesh × number of columns in mesh). Packets are generated in the core of each node, Once a packet generated a node and destination addresses are assigned and labeled with generating time. The router select one buffer at a time and check the buffer if a packet needs to route, if there is a packet in the buffer then router extracts the destination address from the packet and forward to the concerned port by calculating the minimum distance to the destination. When the packet is in the destination node, if the link to the core is not busy it is moved to the core and arrival time is obtained.

4.2 Performance metrics

The performance metric used in the evaluation are total throughput, node throughput, average latency, average extra delay, efficiency and packet lost. which are defined as follows:

4.2.1 Total Throughput

The total throughput means how many packets are received by destination in the network in the simulation time. It is used to measure the performance of entire NoC network. It is derived by the following formula:

Total throughput=(total arrived packets)/(simulation time)

4.2.2 Node Throughput

Node throughput can be obtained by dividing the total throughput on the total number of nodes present in the NoC network.

Node throughput =(total arrived packets)/(Rows × Column)

4.2.3 Packet Latency

Packet latency is defined for each packet as the time between packet generation and actual arrival time.

Packet Latency= (actual arrival time – packet generation time)

4.2.4 Extra Delay

Extra delay can be calculated by subtracting the minimum arrival time from actual arrival time.

Extra delay = (actual arrival time of packet – minimum arrival time of packet)

4.2.5 Efficiency

Efficiency is the ratio between total packets and arrived packets in percent.

Efficiency = (total arrived packets ×100)/(total packets)

4.2.6 Packet Lost

If the core buffer is full and there is no space to add the packet with buffer queue this packet is considers lost.

Packet Lost: (count of lost packets ×100)/(total packet)

4.3 NoC Operation Example

In this report, packet-switched network is implemented in a 2-D (4×4) mesh topology. In this routing algorithm, a route is decided from the source router to destination router using x-dimension and y-dimension to the supposed locations of nodes within a NoC.

In Figure 4.1, algorithm 1 concept is used, the lower left-hand edge is the source (Sx, Sy) node (3, 1) and the destination (Dx, Dy) node (1, 4) is located at the upper right-hand corner of the network. The X-direction is calculated by deducting the y-coordinate value of the source node from the y-coordinate value of the destination node. In case the number is greater than zero, the way of the route is to the west port of neighbor node which is a node (3, 2). Before routing the packet router first check the west port link of the node (3, 2), whether the channel is busy or not, if not the packet is routed. If the selected port is busy, the packets will be blocked, it will be processed in future execution. If the value is less than zero, the way is to the east port. However, if the value is zero, like in figure 4.1 node (3, 4), it means packet reached to the same column of the destination node, now X-direction is needed to route the packet. This is done by deducting the x-coordinate value of the source node from x-coordinate value of the destination node. If the value is less than zero, the direction is to the south port (2, 4) of the upper node. If the value is greater than zero, the direction is to the north port (4, 4) of the lower node. However, if the value is zero, it means the packet reached its destination. The final route of the packet by using XY Routing is: (3, 1), (3, 2), (3, 3), (3, 4), (2, 4), (1, 4) as shown in Figure 4.1.

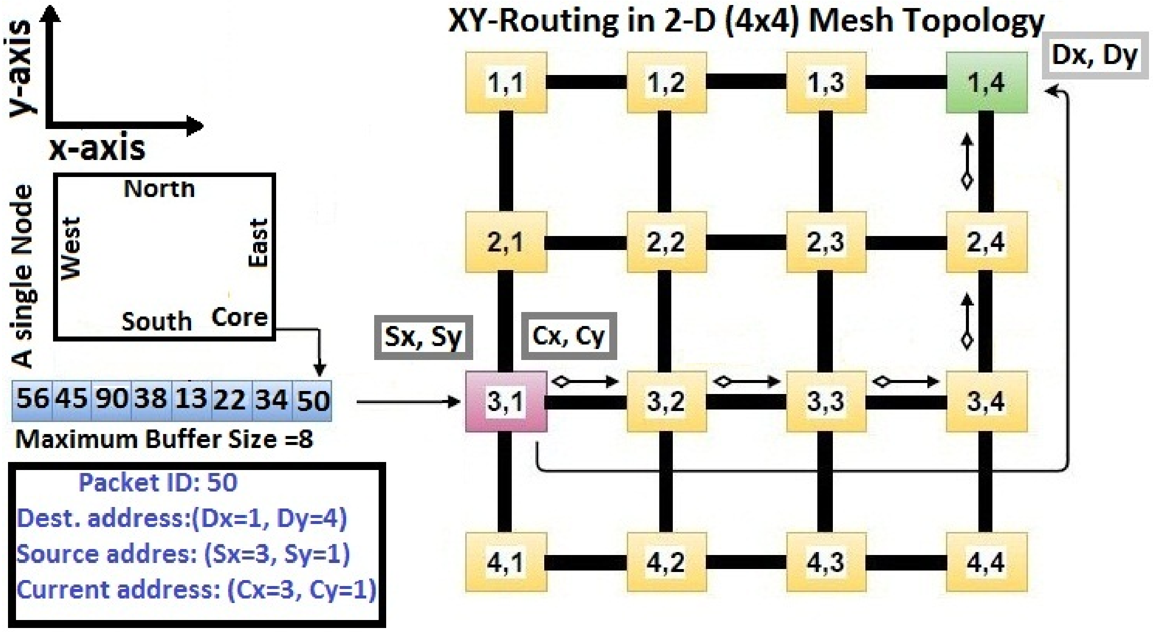

Figure 4.1: XY- Routing in 2-D (4×4) Mesh Topology

4.4 Results

The simulation is performed to see the effect of different network sizes on the performance of the xy-routing algorithm. In the below figures, network size effects on the node throughput, average latency, average extra delay, efficiency, packet lost, and network throughput are showed.

4.4.1 Network size effects on total network throughput

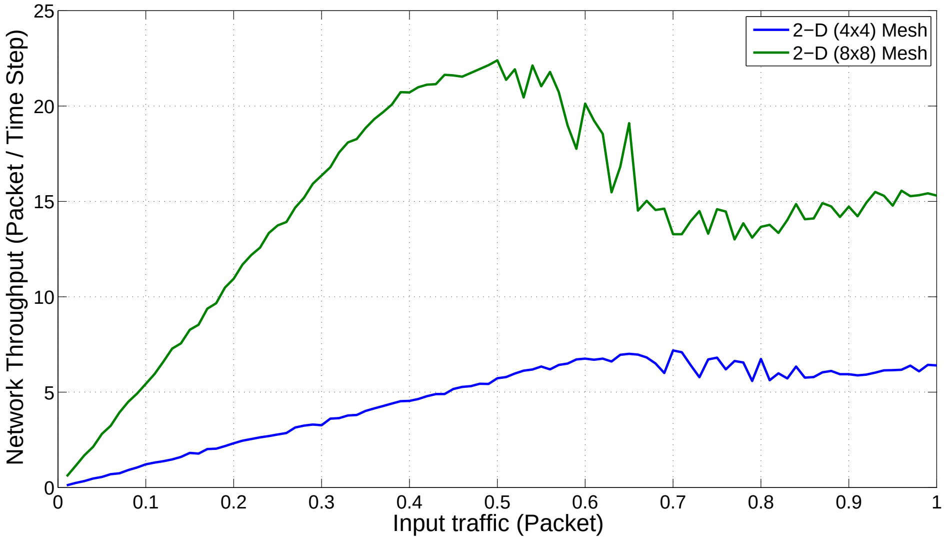

Figure 4.2: Total Network Throughput

4.4.2 Effect of network size on node throughput

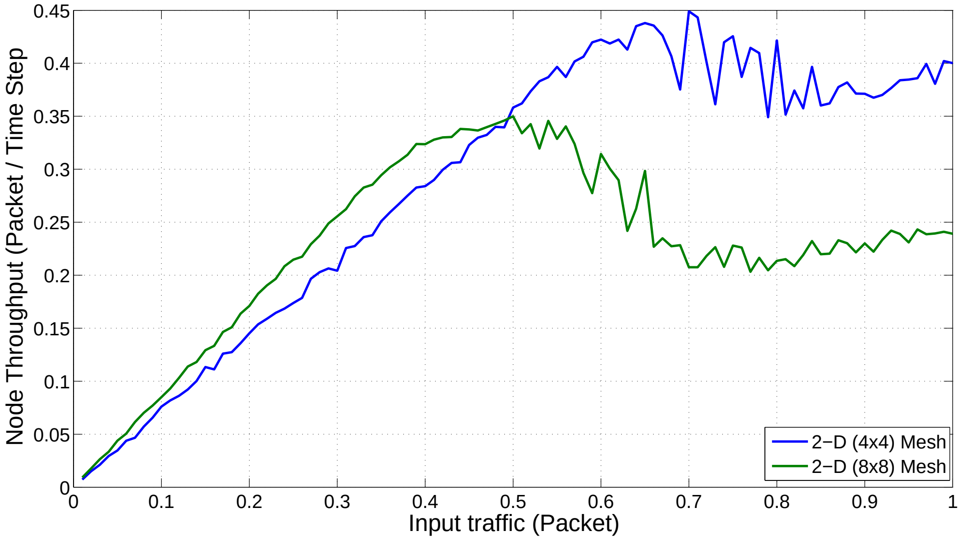

Figure 4.3: Node Throughput

4.4.3 Effect of NoC network size on average latency

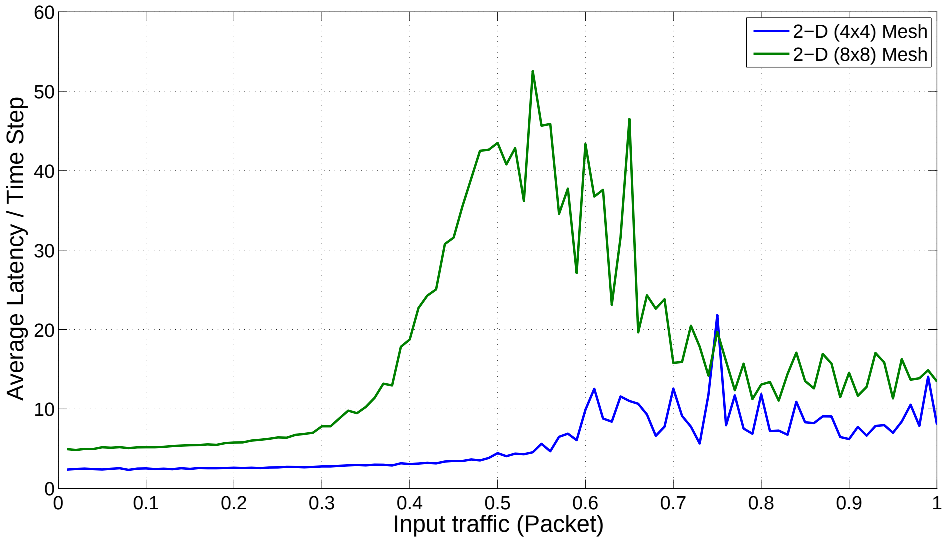

Figure 4.4: Average Latency

4.4.4 Effect of network size on average extra delay

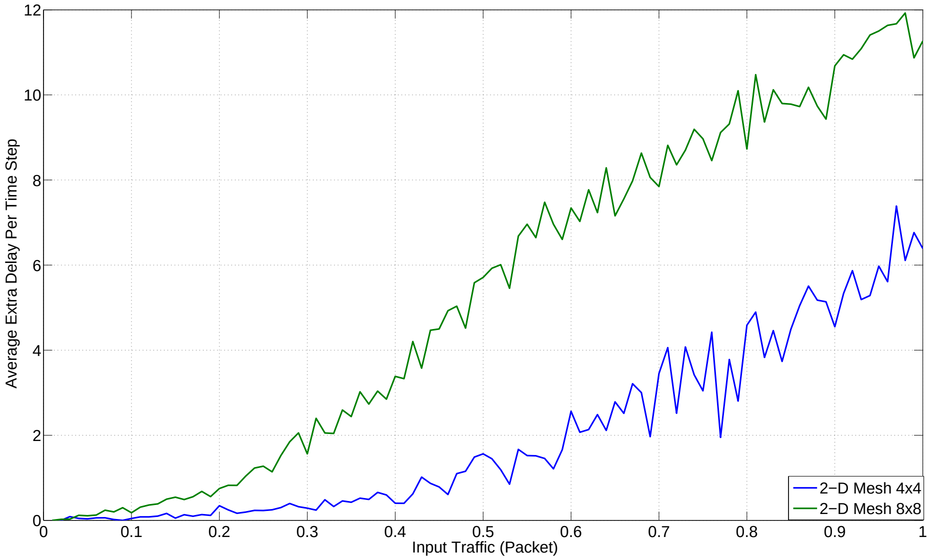

Figure 4.5: Average Extra Delay

4.4.5 Effect of NoC network size on packet lost

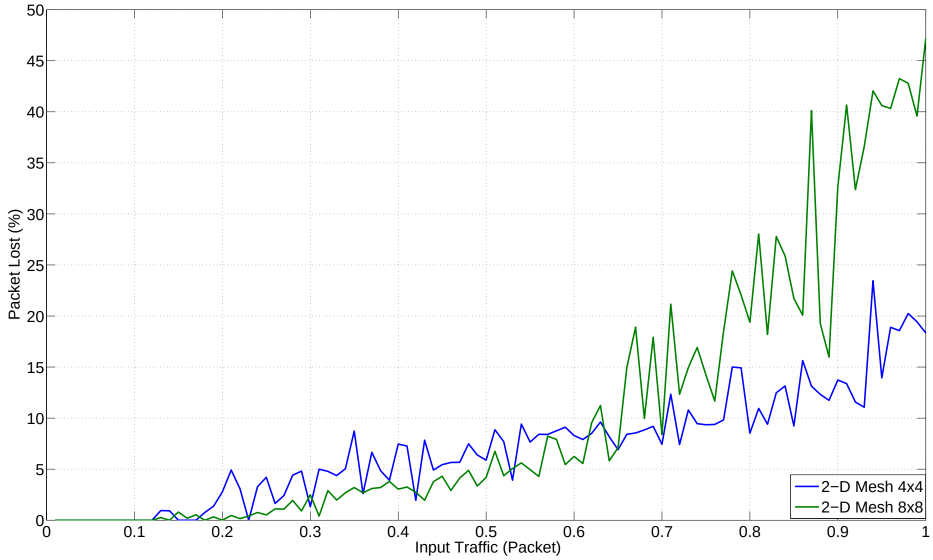

Figure 4.6: Packet Lost

4.4.6 Effect of network size on efficiency

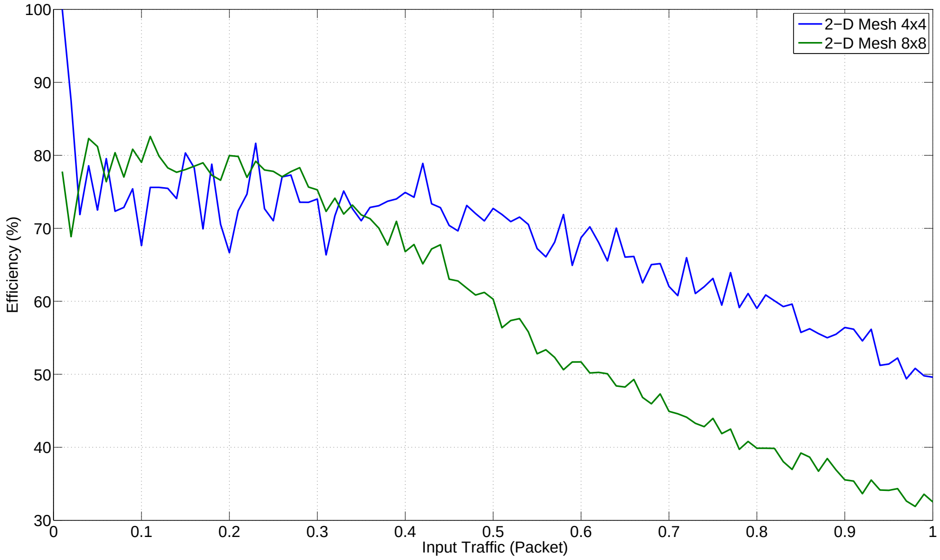

Figure 4.7: Efficiency

When the network size is increased the network throughput also grows in Figure 4.2, because the count of routers increases in the NoC network. we can notice that node throughput and efficiency decreases with the network expansion (Figures 4.3, 4.7), at the same time average latency, average extra delay and packet lost increases (Figures 4.4, 4.5, 4.6).

Chapter 5

Conclusion

In this report, we examined XY routing algorithm for different network sizes based on 2-D mesh topology using Matlab simulation. Implementation of XY routing algorithm is simple as compared to other techniques and it is used widely in all architectures. We studied that network size effects the total performance of XY routing. According to results, XY routing algorithm has better performance in small networks comparing to large NoC networks.

5.1 Future Work

The goal of this project is to evaluate XY routing algorithm for different network sizes based on 2-D mesh topology. The future scope of this work can be evaluating the effect of different buffer sizes on XY routing or using different network topology for this work.

Bibliography

[1] Abdul Quaiyum Ansari, Mohammad Rashid Ansari, and Mohammad Ayoub Khan. Performance evaluation of various parameters of network-on-chip (noc) for different topologies. In *India Conference (INDICON), 2015 Annual IEEE*, pages 1–4. IEEE, 2015.

[2] David Atienza, Federico Angiolini, Srinivasan Murali, Antonio Pullini, Luca Benini, and Giovanni De Micheli. Network-on-chip design and synthesis outlook. *INTEGRATION, the VLSI journal*, 41(3):340–359, 2008.

[3] Davide Bertozzi and Luca Benini. Xpipes: A network-on-chip architecture for gigascale systems-on-chip. *IEEE circuits and systems magazine*, 4(2):18–31, 2004.

[4] Tobias Bjerregaard and Shankar Mahadevan. A survey of research and practices of network-on-chip. *ACM Computing Surveys (CSUR)*, 38(1):1, 2006.

[5] Evgeny Bolotin, Israel Cidon, Ran Ginosar, and Avinoam Kolodny. Qnoc: Qos architecture and design process for network on chip. *Journal of systems architecture*, 50(2):105–128, 2004.

[6] Shubhangi D Chawade, Mahendra A Gaikwad, and Rajendra M Patrikar. Review of xy routing algorithm for network-on-chip architecture. *International Journal of Computer Applications*, 43(21):975–8887, 2012.

[7] William J Dally and Charles L Seitz. Deadlock-free message routing in multiprocessor interconnection networks. *IEEE Transactions on Computers*, 36(5):547–553, 1987.

[8] William James Dally and Brian Patrick Towles. *Principles and practices of interconnection networks*. Elsevier, 2004.

[9] Masood Dehyadgari, Mohsen Nickray, Ali Afzali-Kusha, and Zainalabein Navabi. Evaluation of pseudo adaptive xy routing using an object oriented model for noc. In *Microelectronics, 2005. ICM 2005. The 17th International Conference on*, pages 5–pp. IEEE, 2005.

[10] Jose Duato, Sudhakar Yalamanchili, and Lionel M Ni. *Interconnection networks: an engineering approach*. Morgan Kaufmann, 2003.

[11] Somulu Gugulothu and MD Chawhan. Design and implementation of various topologies for networks on chip and its performance evolution. In *Electronic Systems, Signal Processing and Computing Technologies (ICESC), 2014 International Conference on*, pages 7–11. IEEE, 2014.

[12] Axel Jantsch, Hannu enhunen, et al. *Networks on chip*, volume 396. Springer, 2003.

[13] NE Jerger and L Peh. On-chip networks-synthesis lecture on computer architecture. *Morgan & Claypool Publishers*, 2009.

[14] Nan Jiang, James Balfour, Daniel U Becker, Brian Towles, William J Dally, George Michelogiannakis, and John Kim. A detailed and flexible cycle-accurate network-on-chip simulator. In *Performance Analysis of Systems and Software (ISPASS), 2013 IEEE International Symposium on*, pages 86–96. IEEE, 2013.

[15] AS Kale and MA Gaikwad. Design and analysis of on-chip router for network on chip. *International Journal of Computer Trends and Technology*, 9(6):182–6, 2011.

[16] Shashi Kumar, Axel Jantsch, J-P Soininen, Martti Forsell, Mikael Millberg, Johny Oberg, Kari Tiensyrja, and Ahmed Hemani. A network on chip architecture and design methodology. In *VLSI, 2002. Proceedings. IEEE Computer Society Annual Symposium on*, pages 117–124. IEEE, 2002.

[17] Lionel M. Ni and Philip K. McKinley. A survey of wormhole routing techniques in direct networks. *Computer*, 26(2):62–76, 1993.

[18] Sudeep Pasricha and Nikil Dutt. *On-chip communication architectures: system on chip interconnect*. Morgan Kaufmann, 2010.

[19] Wang Zhang, Ligang Hou, Jinhui Wang, Shuqin Geng, and Wuchen Wu. Comparison research between xy and odd-even routing algorithm of a 2-dimension 3x3 mesh topology

network-on-chip. In *Intelligent Systems, 2009. GCIS'09. WRI Global Congress on*, volume 3, pages 329–333. IEEE, 2009.