File: C:/Users/Sir/Documents/HDLDesigns/Design1/Design1/src/partD.v

```
1
2   `timescale 1 ns / 1 ps
3
4   module partD (a,b,y1,y2,y3);
5       input a,b;
6       output y1,y2,y3;
7       assign y1=a&b;
8       assign y2=a||b;
9       assign y3=~(a||b);
10
11  endmodule
12
```