```
1   module adder(a,b,cin,sum,cout);
2       input a,b,cin;
3       output sum,cout;
4       wire cout, y1a, y3a_, y3a, y1b,y3b;
5
6       OAO U1(cin,a,b,a,y1a,y3a_,cout);
7       not U3(cout_,cout);
8       not U4(y3a,y3a_);
9       OAO U2(cout_,y1a,cin,y3a,y1b,y3b,sum);
10
11  endmodule
12
13  module OAO(d,e,f,g,y1,y3_,y4);
14      input d,e,f,g;
15      output y1,y3_,y4;
16
17      not U5(e_,e);
18      not U6(f_,f);
19      nand U1(y1,e_,f_);
20      nand U2(y2,d,y1);
21      nand U3(y3_,f,g);
22      nand U4(y4,y2,y3_);
23  endmodule
```