```
1   `timescale 1 ns / 10 ps
2
3   module testbench;
4       reg a,b,cin;
5       wire s,cout;
6
7       adder UUT(a,b,cin,sum,cout);
8
9       initial
10          begin
11              a=0; b=0; cin=0;
12              $display("                  TIME |  A B Ci | sum | Co");
13              $monitor($time, "%b %b %b %b %b", a,b,cin,sum,cout);
14              $dumpfile("adder.vcd");
15              $dumpvars(1,a,b,cin,sum,cout);
16              $dumpflush;
17              #80 $finish; //specify end time
18          end
19
20      always
21          #10 cin=~cin; //invert cin every 10 time units
22      always
23          #20 b=~b; //invert b every 20 time units
24      always
25          #40 a=~a; //invert a every 40 time units
26  endmodule
```