```
1
2    `timescale 1 ns / 1 ps
3
4    module partS (a,b,y1,y2,y3);
5        input a,b;
6        output y1,y2,y3;
7        and U1(y1,a,b);
8        or U2(y2,a,b);
9        nor U3(y3,a,b);
10
11   endmodule
12
```