File: c:/Users/Sir/Documents/HDLDesigns/Design1/Design1/src/TestBench.v

```
1   module TestBench;
2
3       reg a,b;
4       wire y1,y2,y3;
5
6       partD UUT(a,b,y1,y2,y3);
7
8       initial
9           begin
10              a=0;b=0;
11              $display("                TIME |A| B|Y1|Y2|Y3");
12              $monitor($time,"  %b  %b  %b  %b  %b",a,b,y1,y2,y3);
13          end
14      always
15          begin
16              #10 b=1;
17              #10 a=1;b=0;
18              #10 b=1;
19          end
20      initial
21          #40 $finish;
22
23  endmodule
```