```
1   `timescale 1 ns / 10 ps
2
3   module testbench;
4       integer ctr;
5       wire a = ctr[2];
6       wire b = ctr[1];
7       wire cin = ctr[0];
8       wire sum,cout;
9
10      adder UUT(a,b,cin,sum,cout);
11
12      initial
13          begin
14              ctr=0;
15              $display("                 TIME |  A B Ci | sum | Co");
16              $monitor($time, "     %b %b  %b    %b     %b", a,b,cin,sum,cout
    );
17              $dumpfile("adder.vcd");
18              $dumpvars(1,a,b,cin,sum,cout);
19              $dumpflush;
20              #80 $finish; //specify end time
21          end
22
23      always
24          #10 ctr=ctr+1; //increment counter every 10 time units
25
26  endmodule
```