Prelab 4

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Brennen Green

Verilog Module

```
module prelab(input x, input y, input z, output f);
    always @(x or y or z)
        begin
        case({x,y,z})
            3'b000: f = 'b1;
            3'b001: f = 'b1;
            3'b010: f = 'b1;
            3'b111: f = 'b1;
            default: f = 'b0;
        endcase
        end
endmodule
```

Schematics