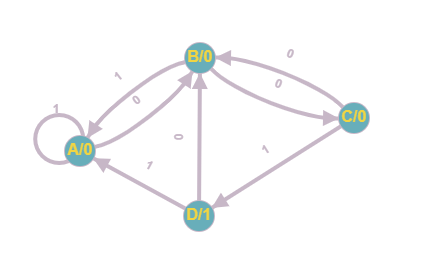
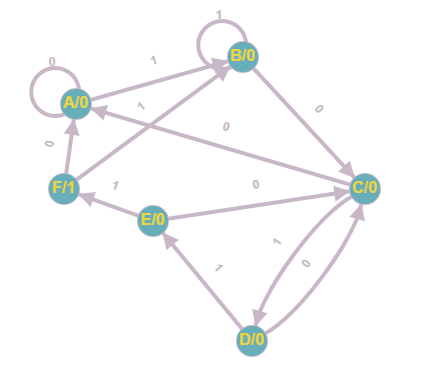
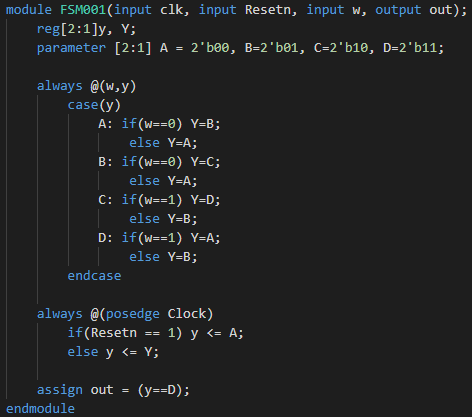
**0 0 1**



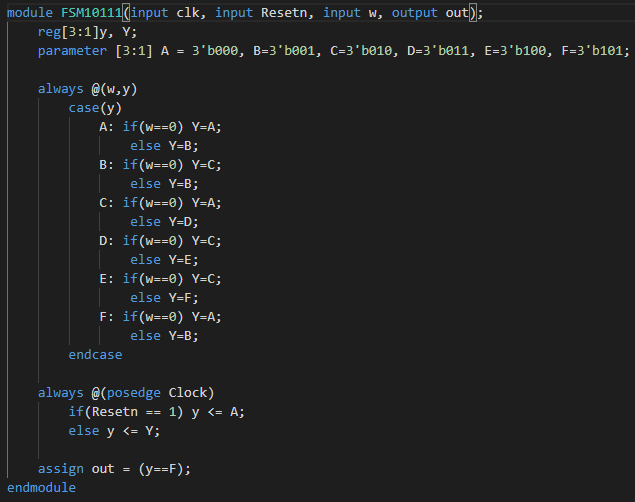
**1 0 1 1 1**

**Verilog**

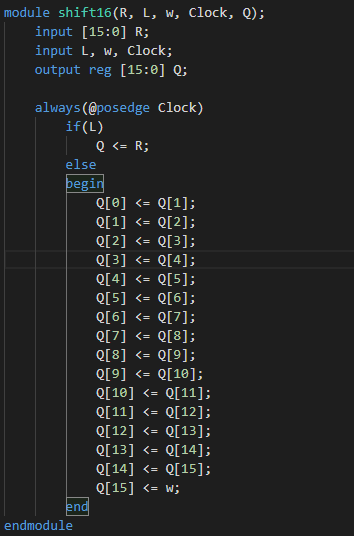
* 1. **0 0 1**



* 1. **1 0 1 1 1**



**16 bit shift register**



**4 bit counter**

