EECS 314: Computer Architecture, Spring 2012

Homework #5 (Each problem is worth 10 points.)

Cache and Memory Hierarchy

1. AMAT (Average Memory Access Time) is useful as a figure of merit for different cache systems since it captures the fact that the time to access data for both hits and misses affects performance. It is computed as: *AMAT = Time for a hit + Miss rate × Miss penalty*

Find the AMAT for a processor with a 2 ns clock, a miss penalty of 20 clock cycles, a miss rate of 0.05 misses per instruction, and a cache access time of 1 clock cycle.

Suppose we can improve the miss rate to 0.03 misses per reference by doubling the cache size. This causes the cache access time to increase to 1.2 clock cycles. If the cache access time determines the processor's clock cycle time, which is often the case, AMAT may not correctly indicate whether one cache design is better than another. If the processor's clock cycle time must be changed to match that of a cache, is this a good trade-off? Assume the processors are identical except for the clock rate and the number of cache miss cycles; assume 1.5 references per instruction and a CPI without cache misses of 2. The miss penalty is 20 cycles for both processors.

[**Clue** for the second part: compare the execution time in the original and new processor. Execution time = IC * (CPI_{base} + Cache miss cycles per instruction) * Clock cycle]

2. Here is a series of address references given as word addresses: 2, 3, 11, 16, 21, 13, 64, 48, 19, 11, 3, 22, 4, 27, 6, and 11. Assuming a direct-mapped cache with 16 one-word blocks that is initially empty, label each reference in the list as a hit or a miss and show the final contents of the cache.

3. Consider three processors with different cache configurations:

- Cache 1: Direct-mapped cache with one-word blocks
- Cache 2: Direct-mapped cache with four word blocks
- Cache 3: Two-way set associative with four-word blocks

The following miss rate measurements have been made:

- Cache 1: Instruction miss rate is 4%; data miss rate is 6%

- Cache 2: Instruction miss rate is 2%; data miss rate is 4%
- Cache 3: Instruction miss rate is 2%; data miss rate is 3%

For these processors, one half of the instructions contain data reference. Assume that the cache miss penalty is 6 + Block size in words. The CPI for this workload was measured on a processor with cache 1 and was found to be 2.0. Determine which processor spends the most cycles on cache misses.

4. Consider a virtual memory system with the following properties:

- 40-bit virtual byte address
- 16 KB pages
- 36-bit physical byte address

What is the total size of the page table for each process on this processor, assuming that the valid, protection, dirty and use bits take a total of 4 bits and that all the virtual pages are in use? (Assume that disk addresses are not stored in the page table.)

5. If all misses are classified into one of three categories – compulsory, capacity, or conflict – which misses are likely to be reduced when a program is re-written so as to require less memory? How about if the clock rate of the processor the program is running on is increased? How about if the associativity of the existing cache increased?

Superscalar Processor

6. Compare the two approaches of a multiple-issue pipeline design: VLIW (Very Large Instruction Word) and SuperScalar. Describe the advantages and disadvantages of both approaches.

How can you overcome different data dependencies (true dependency, output dependency and anti dependency) in a superscalar pipeline? How does the RUU (Register Update Unit) to manage a consistent machine state with out-of-order issue and completion (OOI and OOC)?