Homework #2

EECS 314: Computer Architecture

Spring 2012

- There are 10 problems in total. Each problem has 10 points.

1.

The following MIPS instruction sequence could be used to implement a new instruction that has two register operands. Give the instruction a name and describe what it does. Note that register $t0 is being used as a temporary.

srl $s1, $s1, 1 #

sll $t0, $s0, 31 # These 4 instructions accomplish

srl $s0, $s0, 1 # “new $s0 $s1”

or $s1, $s1, $t0 #

2.

Add comments to the following MIPS code and describe in one sentence what it computes. Assume that $a0 and $a1 are used for the input and both initially contain the integers *a* and *b*, respectively. Assume that $v0 is used for the output.

Can you re-write the code with less number of instructions? If yes, write the new code.

```
            add $t0, $zero, $zero
loop:       beq $a1, $zero, finish
            add $t0, $t0, $a0
            sub $a1, $a1, 1
            j loop
finish:     addi $t0, $t0, 100
            add $v0, $t0, $zero
```

3.

As discussed in class, pseudoinstructions are not part of the MIPS instruction set but often appear in MIPS programs. For each pseudoinstruction in the following table, produce a minimal sequence of actual MIPS instructions to accomplish the same thing. You may need to use $at for some of the sequences. In the following table, big refers to a specific number that requires 32 bits to represent and small to a number that can fit in 16 bits.

pseudoinstruction	What it accomplishes
move $t1, $t2	$t1 = $t2
clear $t0	$t0=0
beq $t1, small, L	if ($t1=small) go to L
beq $t2, big, L	if ($t2 = big) go to L
li $t1, small	$t1 = small
li $t2, big	$t2 = big
ble $t3, $t5, L	if ($t3 <= $t5) go to L
bgt $t4, $t5, L	if ($t4 > $t5) go to L
bge $t5, $t3, L	if ($t5 >= $t3) go to L
addi $t0, $t2, big	$t0 = $t2 + big
lw $t5, big ($t2)	$t5 = Memory [$t2 + big]

4.

Given your understanding of PC-relative addressing, explain why an assembler might have problems directly implementing the branch instructions in the following code sequence:

```
here:   beq $s0, $s2, there

…

there   add $s0, $s0, $s0
```

Show how the assembler might rewrite this code sequence to solve these problems.

5.

Suppose that all of the conditional branch instructions except beq and bne were removed from the MIPS instruction set along with slt and all of its variants (sltgi, sltu, sltui) Show how to perform

```
slt $t0, $s0, $s1
```

Using the modified instruction set in which slt is not available (Hint: it requires more than two instructions)

6.

Find the shortest sequence of MIPS instructions to perform double precision integer multiplication. Try to do it in 35 instructions or less. Assume that one 64-bit, unsigned integer is in registers $t2 and $t5 and another is in registers $t6 and $t7. The 128-bit product is to be placed in registers $t0, $t1, $t2, and $t3. In this example, the most significant word is found in the lower-numbered registers, and the least significant word is found in the higher-numbered registers. (Hint: Write out the formula for (a * 2^32 + b) * (c * 2^32 + d).

7.

Bits have no inherent meaning but we assign them specific interpretation. Given the bit pattern:

101011010001 0000 0000 0000 0000 0010

What does it represent, assuming that it is

a. a two's complement integer?

b. an unsigned integer?

c. a single precision floating-point number?

d. a MIPS instruction?

You may find the MIPS opcode description and the instruction format in the green MIPS reference data page useful.

8.

With x=0100 0010 1101 1000 0000 0000 0000 0000_{two} and y=1011 1110 1110 0000 0000 0000 0000 0000_{two} representing single precision IEEE 754 floating-point numbers, perform, showing all work,:

a. x+y

9.

Consider two different implementations, P1 and P2, of the same instruction set. There are five classes of instructions (A, B, C, D, and E) in the instruction set.

P1 has a clock rate of 4 GHz. P2 has a clock rate of 6 GHz. The average number of cycles for instruction class for P1 and P2 is as follows:

Class	CPI on P1	CPI on P2
A	1	2
B	2	2
C	3	2
D	4	4
E	3	4

Assume peak performance is defined as the fastest rate that a computer can execute any instruction sequence. What are the peak performances of P1 and P2 expressed in instructions per second?

10.

You are the lead designer of a new processor. The processor design and compiler are complete, and now you must decide whether to produce the current design as it stnds or spend additional time to improve it.

You discuss this problem with your hardware engineering team and arrive at the following options:

a. Leave the design as it stands. Call this base computer Mbase. It has a clock rate of 500MHz, and the following measurements have been made using a simulator:

Instruction Class	CPI	Frequency
A	2	40%
B	3	25%
C	3	25%
D	5	10%

b. Optimize the hardware. The hardware team claims that it can improve the processor design to give it a clock rate of 600 MHz. Call this computer Mopt. The following measurements were made using a simulator for Mopt:

Instruction Class	CPI	Frequency
A	2	40%
B	2	25%
C	3	25%
D	4	10%

What is the CPI for each computer?