Design Project #2

ELECENG 2EI4

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L03

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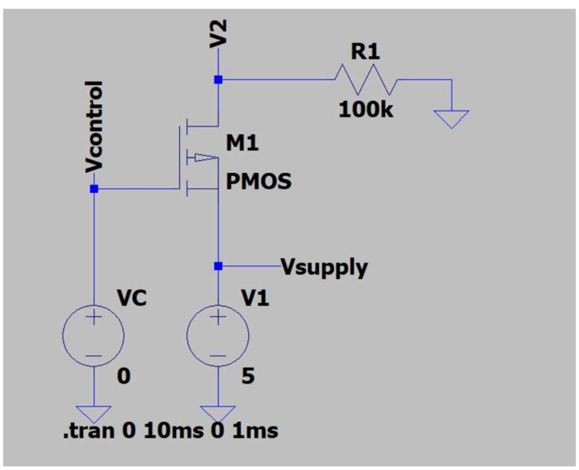
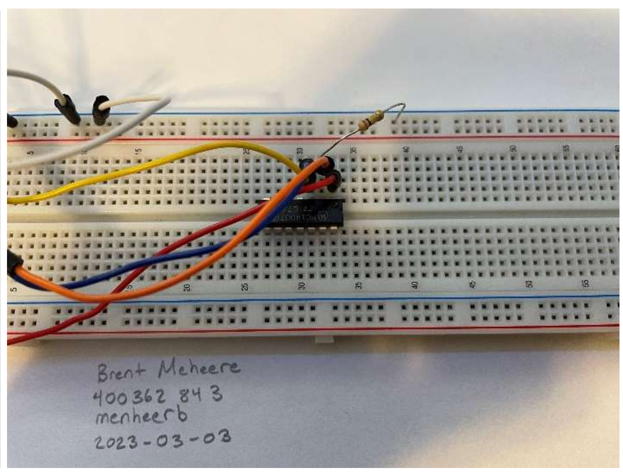
Test Plan:

In order to test the functionality of the circuits involved in this project and measure the non-idealities associated with switches a test plan needs to put in place. To test the functionality of the first switch, the OFF state will best tested first. To test the OFF state, the following values need to be set; Vcontrol = 5 V and Vsupply = 5 V. The value of V1 can be measured from Vsupply, which will be 5 V, and V2 will be measured from the output side of the MOSFET connected to the 100 kOhm resister. The expected measurement of V2 is 0 V. From this state we can test the leakage current by taking the measured value of V2 over 100 kOhm. To test the ON, Vcontrol must be changed to 0 V. Again, V1 will be measured from Vsupply and V2 will be measured from the output side of the MOSFET connected to the 100 kOhm resistor. The expected value of V2 is 5 V. The non-ideality we can measure in this state is Ron. This can be measured by taking the difference between V1 and V2. If there is a difference between the two that means that there is some sort of resistance within the MOSFET. In this state the function of V2 following V1 can be tested by varying the voltage of V1 and seeing how V2 responds. A similar testing process can be used when testing the second switch. To measure the functionality of this switch, measurements must be taken at V1 (supply), VA, and VB. The first state is VA ON. To test this state the following values are set; Vcontrol= 0 V and Vsupply = 5 V. VA must be around 5 V and VB 0 V. To measure the functionality of VB ON, Vcontrol must now be 5V. The expected values of VA and VB are 0 V and 5 V respectively. The same non-idealities apply in terms of this switch.

Switch Type 1:

Circuit Schematic:





Measurements:

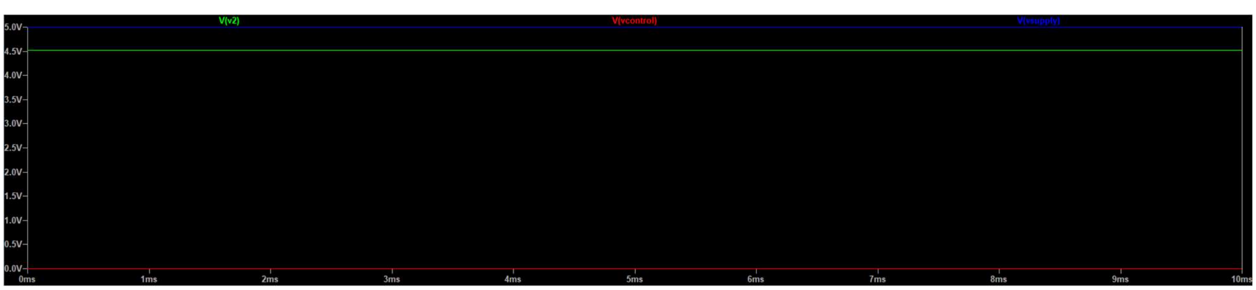


Figure 1 Vcontrol = 0, switch ON

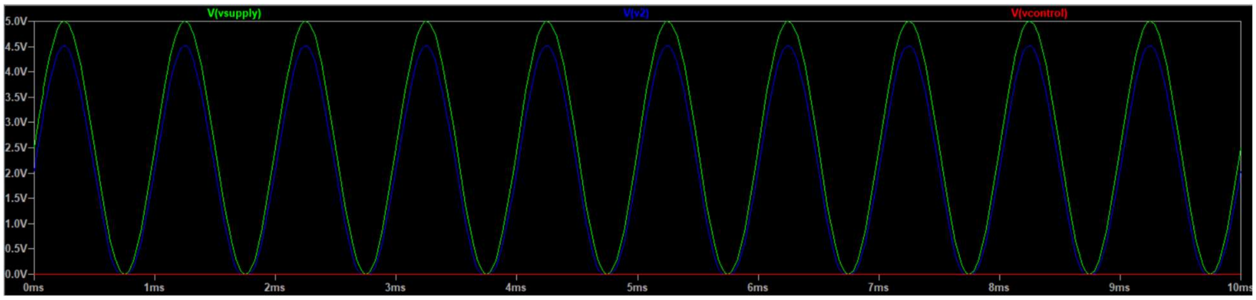


Figure 2 Verifies that V2 follows V1 when ON

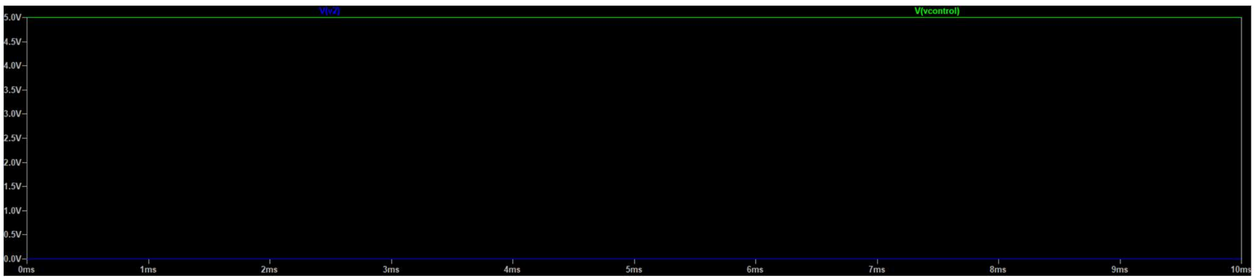


Figure 3 Vcontrol = 5, V2 = 0, switch OFF, Vsupply not shown since it got covered by Vcontrol

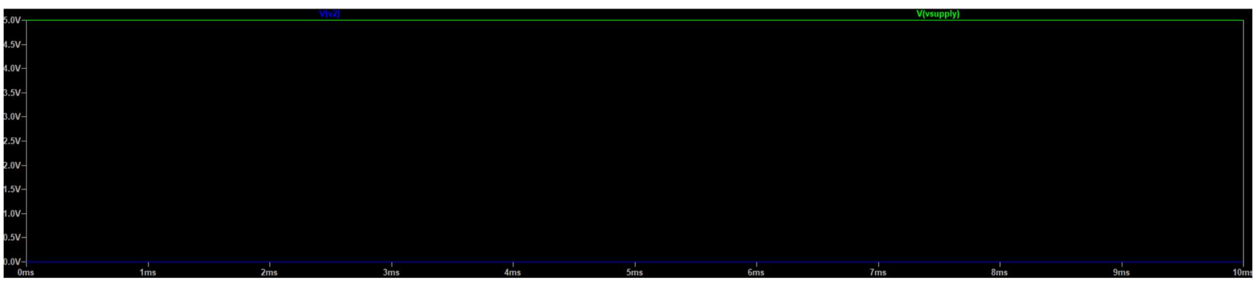


Figure 4 Vsupply = 5, V2 = 0, switch OFF, , Vcontrol not shown since it got covered by Vsupply

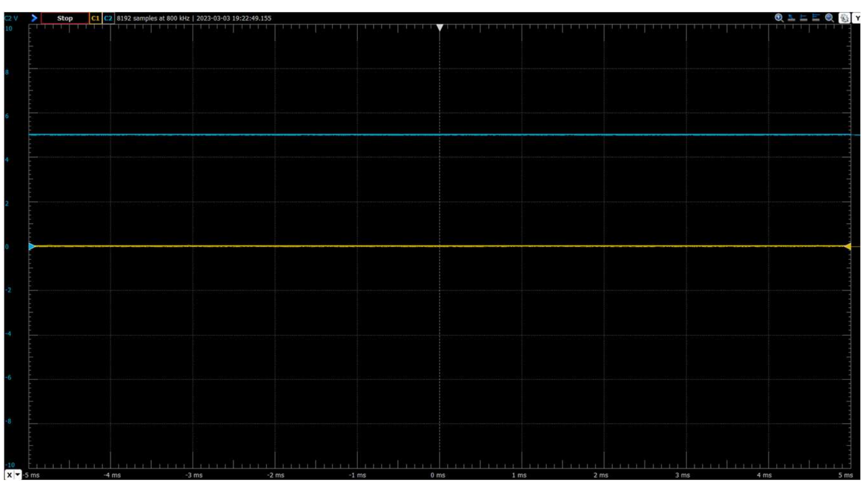


Figure 5 Switch OFF, C1 = V1, C2 = Vcontrol

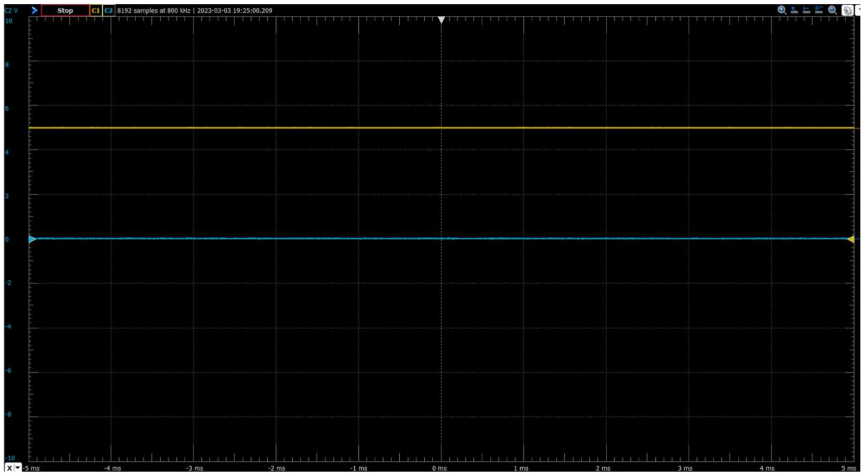


Figure 6 Switch ON, C1 = V1, C2 = Vcontrol

OFF:

I(leakage) = V2/R = 0 A

ON:

V1 – V2 = 0.5 V

Explanation:

The results of the LTSpice simulation are shown in Figures 1 through 4. Figure 1 and 2 show measurements associated with the ON state. From Figure 1 its evident that Vcontrol was set to zero and Vsupply/V1 was set to 5 V. In Figure 2, Vsupply/V1 was set to a varying AC source to test the effects that V1 have on V2. These two figures verify the functionality of the switch. However, some non-idealities are shown as well. Its clear in both figures that V2 is capped at 4.5 V, which represents that the max voltage this switch can operate at is 4.5 V. Along with this, it is visible in Figure 2 that V2 doesn't exactly follow V1 at all times. This can be related to an internal resistance in the MOSFET or simply a time delay between changes. Figures 3 and 4 show measurements associated with the OFF state. Both figures show the same state and inputs, Vcontrol and Vsupply = 5 V, however I split them up so that Vcontrol and Vsupply would not cover each other. From the figures, when Vcontrol is 5 V the switch is OFF and V2 is measured to be 0 V. From this state, the leakage current can be calculated. Since V2 is zero, there is no leakage current. Finally, in figures 5 and 6, the OFF and ON states are tested on the physical circuit. Unexpectedly, there is no capped output voltage seen, and V2 exactly reflects V1. This could be because the MOSFET used in the simulation is not the exact MOSFET used in the physical circuit.

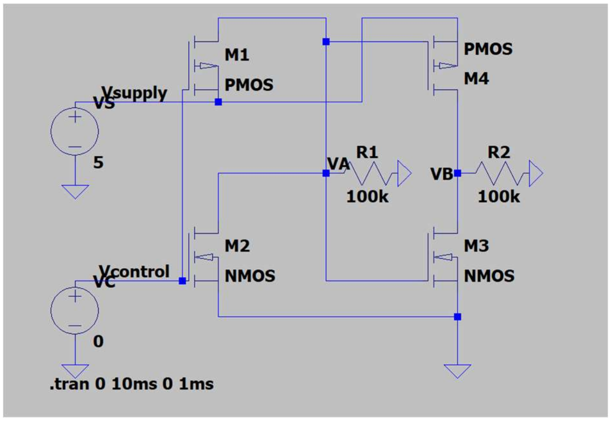
NOTE: All non-idealities were calculated with simulated results, I could not produce results for non-idealities on AD2.

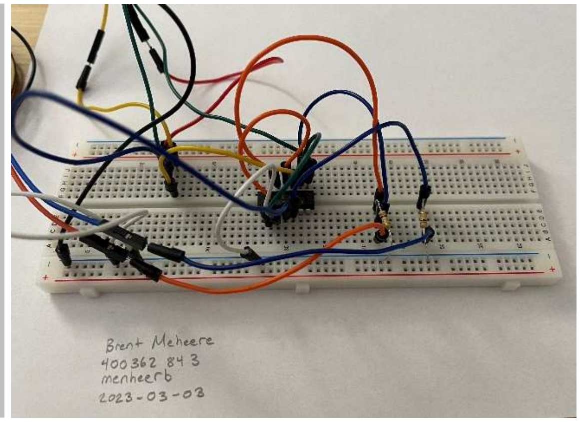
Design Trade-offs:

The design used in switch 1 utilizes the most basic function of a MOSFET. Since MOSFETS have 3 inputs and this switch uses a total of 3 inputs/outputs, there were no trade-offs since it cannot be simpler than this. This design is most likely the cheapest and least complex voltage-controlled switch that can be made to meet our needs.

Switch Type 2:

Circuit Schematic:





Measurements:

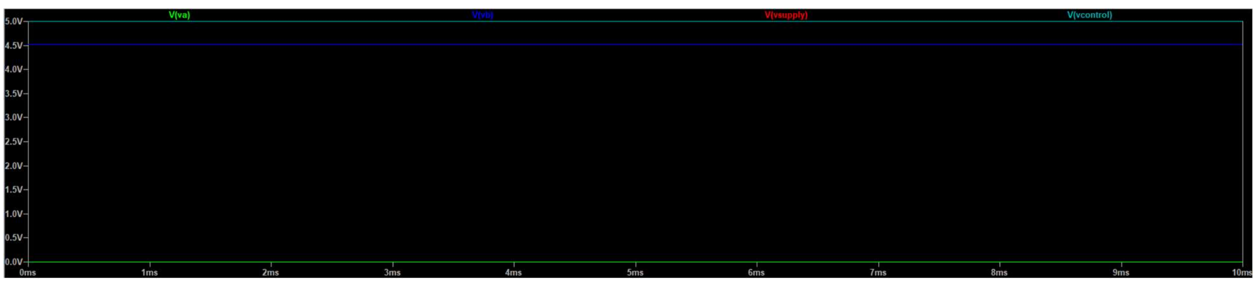


Figure 7 Vcontrol = 5, VB = ON, VA = OFF

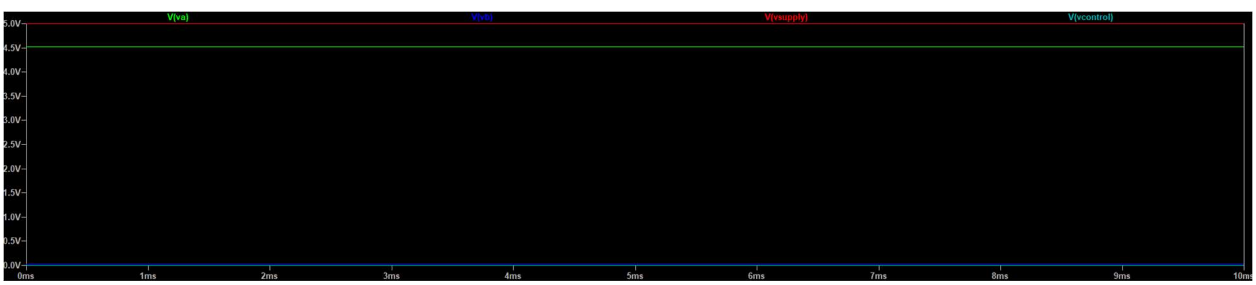


Figure 8 Vcontrol = 0, VB = OFF, VA = ON

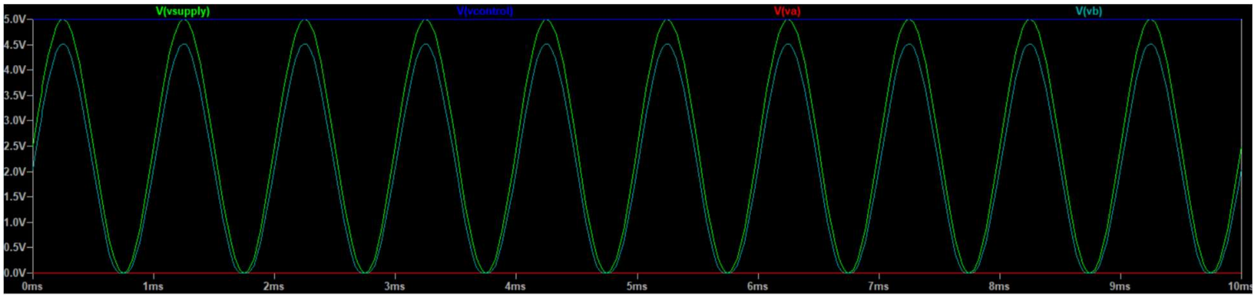


Figure 9 VB ON, VA OFF, Varying V1

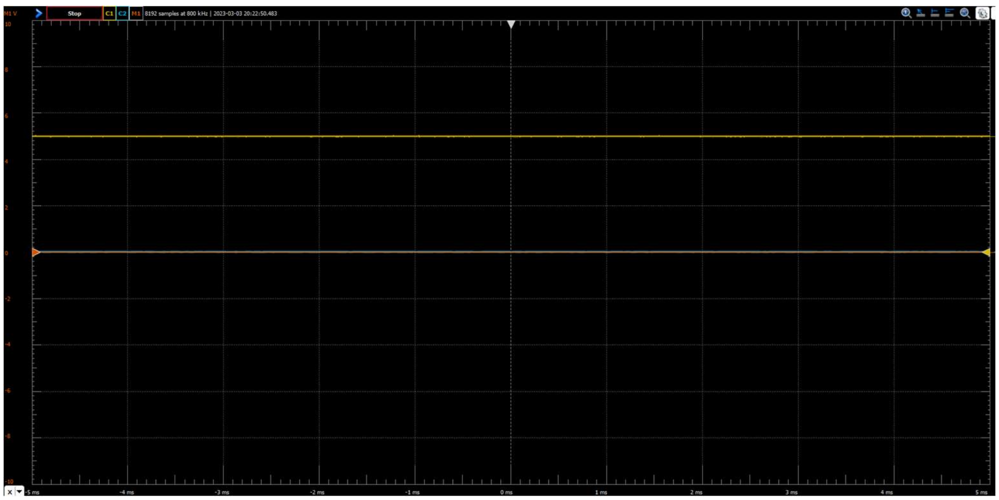


Figure 10 Vcontrol = 0, VB = OFF, VA = ON, C1 = VA, C2 = VB, MATH = Vcontrol

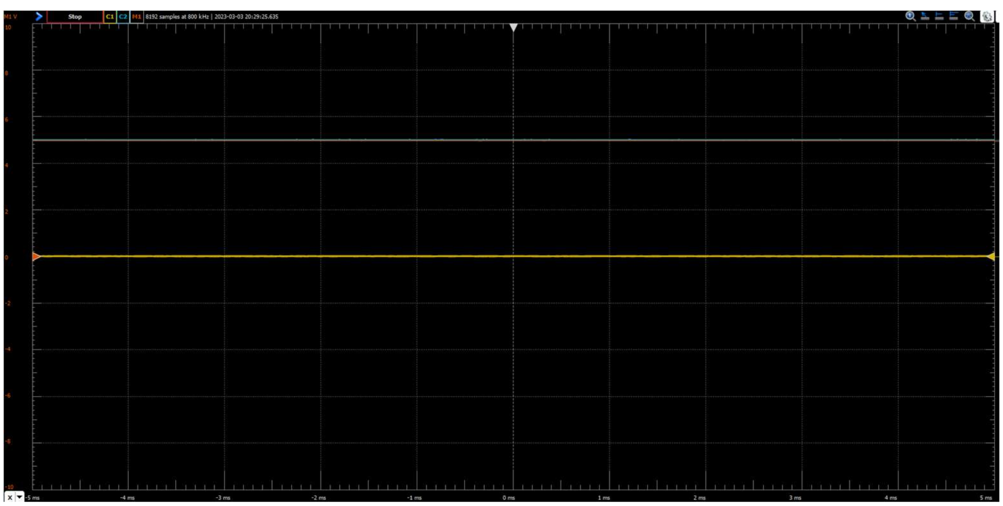


Figure 11 Vcontrol = 5, VB = ON, VA = OFF, C1 = VA, C2 = VB, MATH = Vcontrol

IA(leakage) = VA/R1 = 0 A

IB(leakage) = VB/R2 = 0 A

VA ON:

V1 – VA = 0.5 V

VB = 0 V

VB ON:

V1 – VB = 0.5 V

VA = 0:

Explanation:

Figures 7 and 8 verify the basic functionality of switch 2. When Vcontrol = 0, VA should reflect V1, when Vcontrol = 5 V, VB should reflect V1. In both cases, Vsupply/V1 was set to 5 V. Similar to switch 1, to test how the output voltage reflects the input voltage, in Figure 9 I set Vsupply/V1 to a varying AC source and measured how VB reacted. Again, the output voltage was capped at 4.5, showing that the max operating voltage is 4.5 V. It is also evident again that either an internal resistance or time delay causes the output voltage to not strictly follow the input voltage. Figures 10 and 11 show the outputs of VA ON, and VB ON implemented onto a physical circuit and measured on the AD2. Again, the expected capped voltage from the simulation was not seen when physically implemented.

NOTE: All non-idealities were calculated with simulated results, I could not produce results for non-idealities on AD2.

Design Trade-offs:

The most prevalent design decision for switch 2 was to make it as simple as possible. This design utilizes a total of 4 MOSFETS, 2 voltage sources, and 2 output terminals for measurement. When working with more complex circuits involving many connections and components, keeping things organized is essential for debugging and building purposes. The biggest step to make this circuit as simple as it can be, was to create a clean schematic to minimize error and confusion. To make the schematic easy to follow, the amount of wire and nodes were minimized. Along with this, the components used were minimized as well. The least amount of MOSFETS I could use while maintaining functionality was 4 (2 PMOS and 2 NMOS). If put into production, minimizing the amount of wire and components needed would reduce cost.