Design Project #4

ELECENG 2EI4

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L03

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Circuit Schematic:

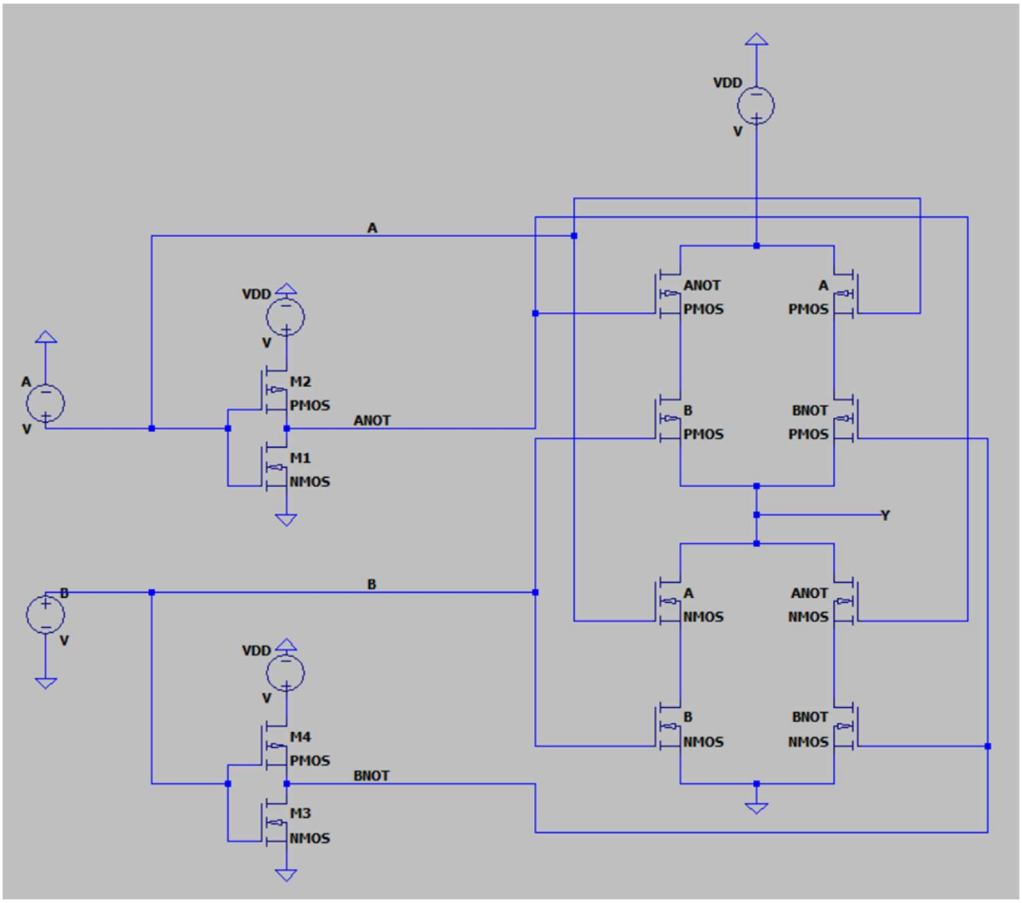


Figure 1 Schematic of circuit

NOTE: Schematic shows general layout of circuit, some sources and drains may not be entirely correct. Orientation of MOSFETS relates to orientation on the physical chip (i.e. top of MOSFET on schematic corresponds with top of MOSFET on chip).

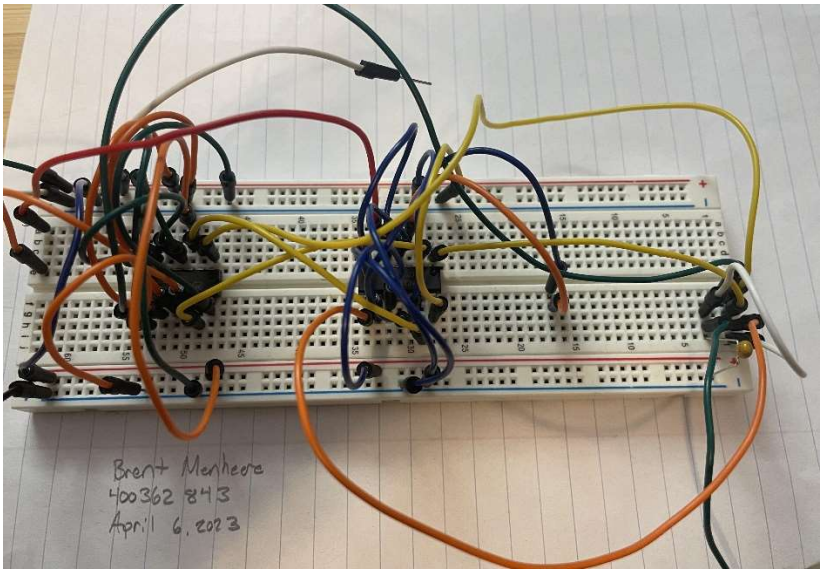
Ideal Sizing:

The ideal sizing of a MOSFET in relation to a system is associated with the transconductance and current properties. As the ratio between width and length increases, so does current gain, and in effect current for Vg. The ideal sizing ratio for PMOS and NMOS in a system should be 2.5. This is determined since the average sizing for PMOS is (W/L)P = 5/1 and NMOS is (W/L)N = 2/1. Therefore, the ratio is PMOS/NMOS (5/2 = 2.5).

This ideal sizing can be implemented in the hardware design, as the ratio of PMOS to NMOS sizing of this design is 2P/2N. This is calculated because the path of most ‘resistance’ from VDD to ground is two PMOS and two NMOS transistors. As mentioned above, the sizing of PMOS and NMOS is 5/1 and 2/1 respectively. There for the following calculation can be made:

PMOS/NMOS = 2P/2N = (10/1)/(4/1) = 2.5, which is the ideal sizing.

Testing:



Functional Testing:

A	B	Output
0	0	0
1	0	1
0	1	1
1	1	0

Figure 2 XOR gate truth table

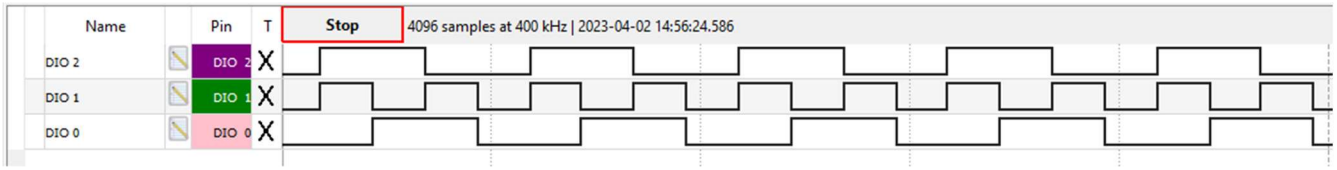


Figure 3 Functionality testing using digital IO pins

The functionality of the circuit built is shown in Figure 3. Digital IO pin DIO 0 represents input A and DIO 1 represents input B. DIO 0 was set to 1 kHz while DIO 1 was set to 2 kHz. This produces a staggered combination between the two which we can use to verify the XOR truth table. Starting from the far left of the plot and up until just before the first dotted vertical line, all four outputs can clearly be seen in DIO 2.

Static Level Testing:

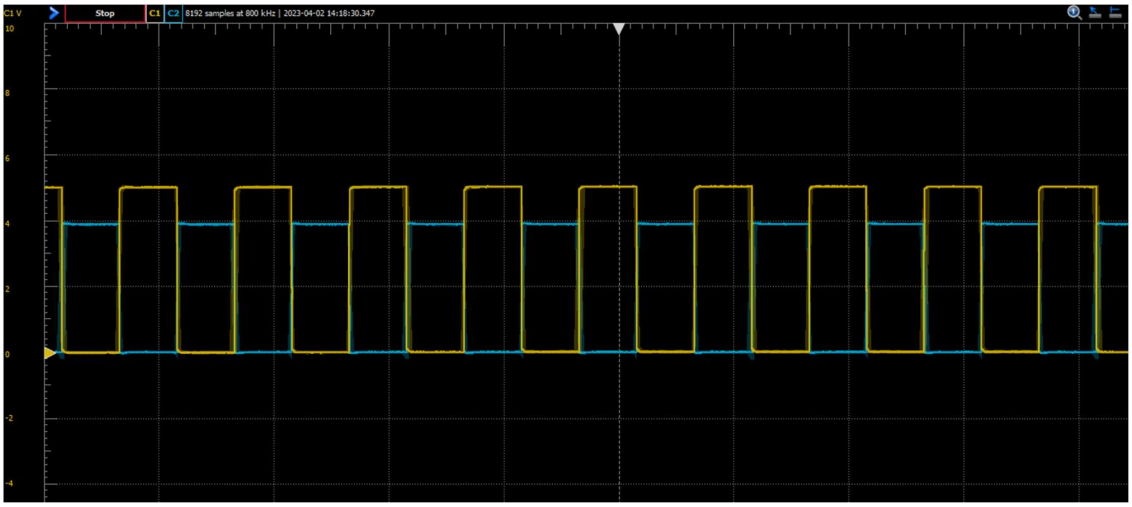


Figure 4 C1 (yellow) represents input A, C2 (blue) represents output of gate

To acquire results for static level testing, input A was set to a square wave between 0 and 5 V and unput B was set to a constant 5 V which represents logic-1. The output was measured on the AD2 scope and can be seen in Figure 4. From this plot it was determined, using the measurement function, that VH is 4.064 V and VL is around 0 V. When switching the inputs of A and B the plot measured was identical to the original, meaning VH and VL did not change.

	Name	Value
C1	Maximum	4.0636 V

Failing:

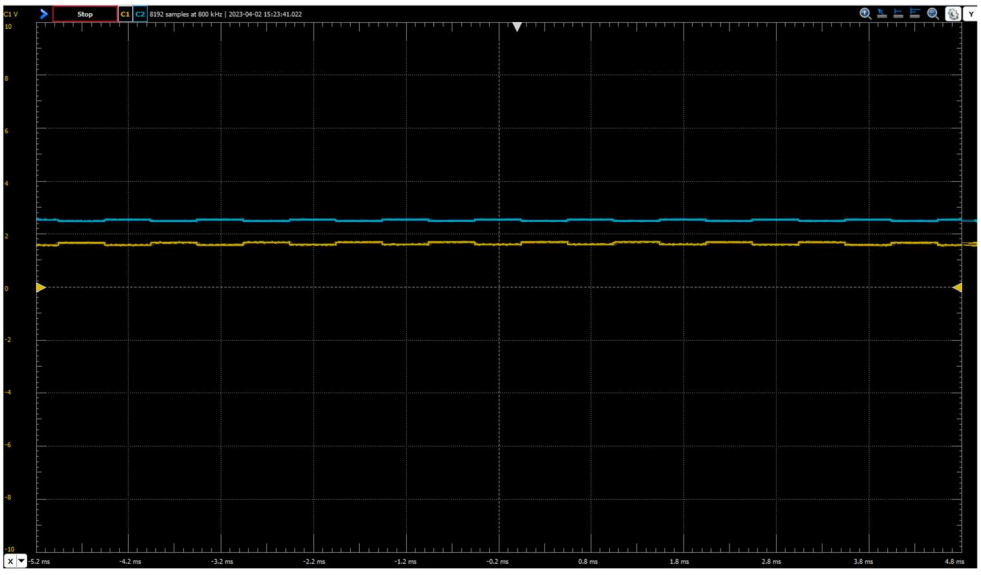


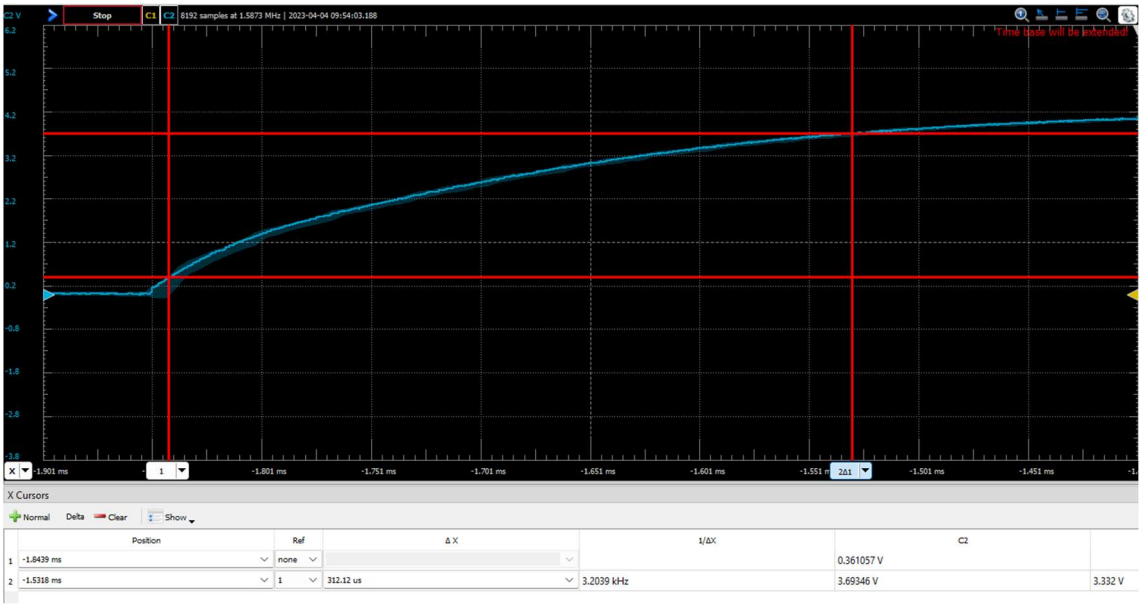
Figure 5 Plot of input and output just before failure

	Name	Value
C1	Maximum	1.7086 V
C1	Minimum	1.5452 V

To determine VIH and VIL, input B was set to a constant 5 V to represent logic-1 while input A was once again set to a square wave. The amplitude of A was gradually decreased until the different between HI and LO for the output was close to indifferent, meaning the gate no longer functions properly. From this it was determined that VIH is 1.71 V and VIL is 1.55 V. This means that the lowest input value recognized as logic-1 is 1.71 and the highest input recognized as logic-0 is 1.55 V.

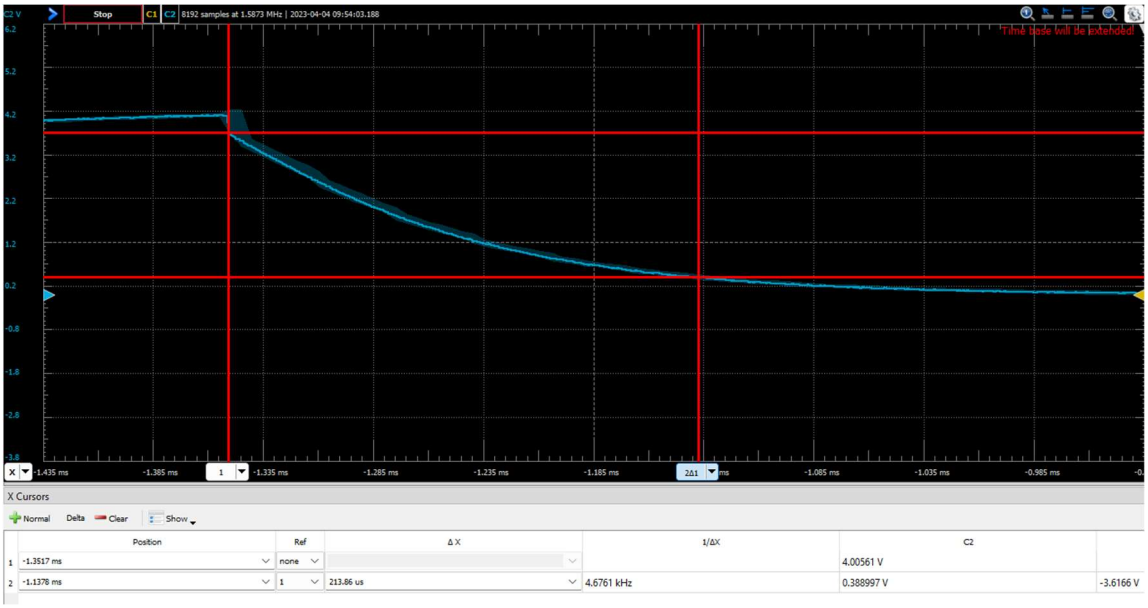
Timing:

Rise Time:



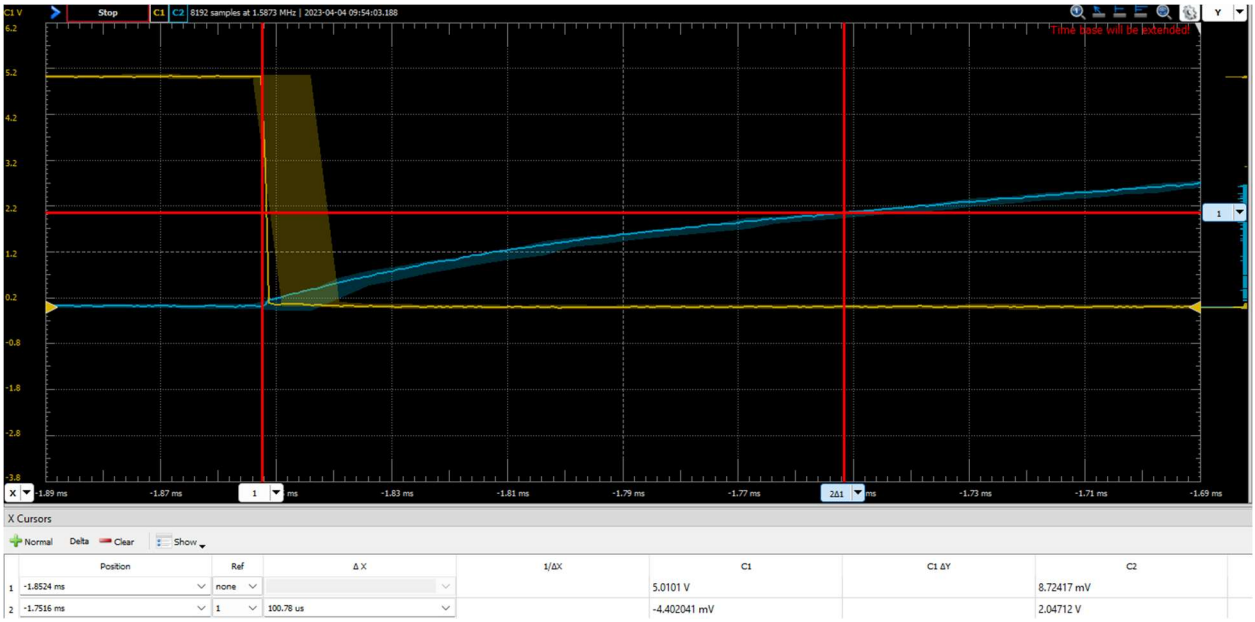
The rise time was calculated by measuring the time it takes the output to go from 10% of its highest voltage to 90% of its highest voltage. The rise time was measured to be 312 µs.

Fall Time:



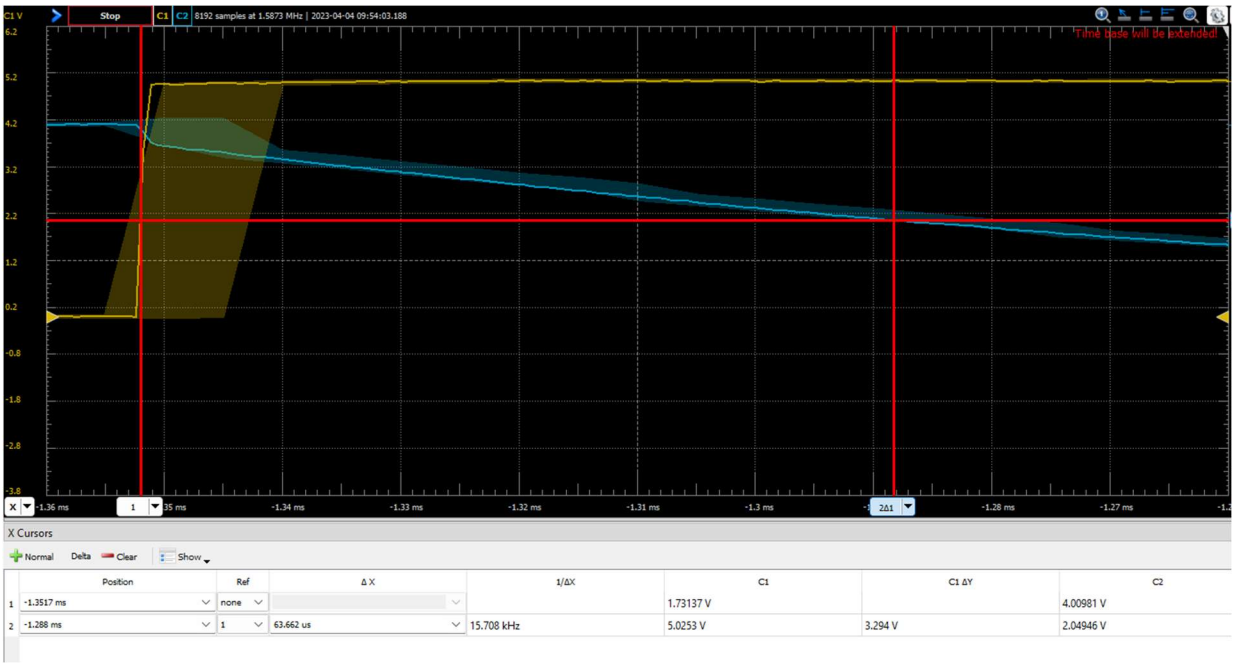
The rise time was calculated by measuring the time it takes the output to go from 90% of its highest voltage to 10% of its highest voltage. The fall time was measured to be 214 µs.

TPLH:



To calculate the low-to-high delay, the time was measured from the transition of high-to-low of the input waveform to half of the output waveform. In an ideal environment where the voltage does not drop from the source, this value would be 5/2 V, however since the output decreases, the halfway voltage was closer to 4/2 V. The delay was measured to be 101 µs.

TPHL:



To calculate the high-to-low delay, the time was measured from the transition of low-to-high of the input waveform to half of the output waveform. Again, in an ideal environment where the voltage does not drop from the source, this value would be 5/2 V, however since the output decreases, the halfway voltage was closer to 4/2 V. The delay was measured to be 64 μs.

To calculate the propagation delay we compute the following calculation:

$Tp = (Tplh + Tphl)/2 = (101 + 64)/ 2 = 82.5$ μs.