Design Project #1

ELECENG 2EI4

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L03

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Summary:

In Design Project #1, the problem being investigated was to deign and build a DC power supply. This supply is to deliver 10 mA at 3V from a 120 V (rms) source at 1 kHz. In general, a dc power supply includes a transformer, rectifier, filter, and regulator. For this project, the transformer was not to be physically implemented in our design, but rather theoretically used to step down the voltage for our rectifier. This design uses a full-wave center-tapped transformer as the rectifier technology. This system captures the positive and negative amplitude of the AC input signal to create a positive signal. A single capacitor is used as a filter to reduce the fluctuation in the output. This design does not involve a regulator as it would increase the complexity of the circuit and this current design could obtain the target output without one.

Design:

Transformer:

This design does not utilize a transformer; however, a transformer would be needed to step down the 120 V (rms) input to the needed voltage for rest of the circuit. This design requires 7.6 V of input into the rectifier. This number was determined experimentally after testing multiple input voltages in the LTSpice simulation. The turns ratio was calculated to be 21:1.

Rectifier:

The rectifier used in this design is a full-wave center-tapped transformer. Conventionally, this technology utilizes the secondary coil of a transformer, in which two diodes are connected to the top and bottom. In this design, since no transformer is used, two diodes are connected to two separate voltage sources of equal magnitude and opposite direction. This design functions as a rectifier by selectively passing a forward voltage into the load. Since diodes act as a one-way switch, only the positive amplitude of the first voltage source get pass through. Similarly, the second voltage source only passes its negative amplitude through its respective diode which is seen as positive voltage by the load since the source is reversed. This type of rectifier was chosen because it captures the full wave. The center-tapped transformer is also significantly simpler to implement compared to a full-wave bridge rectifier.

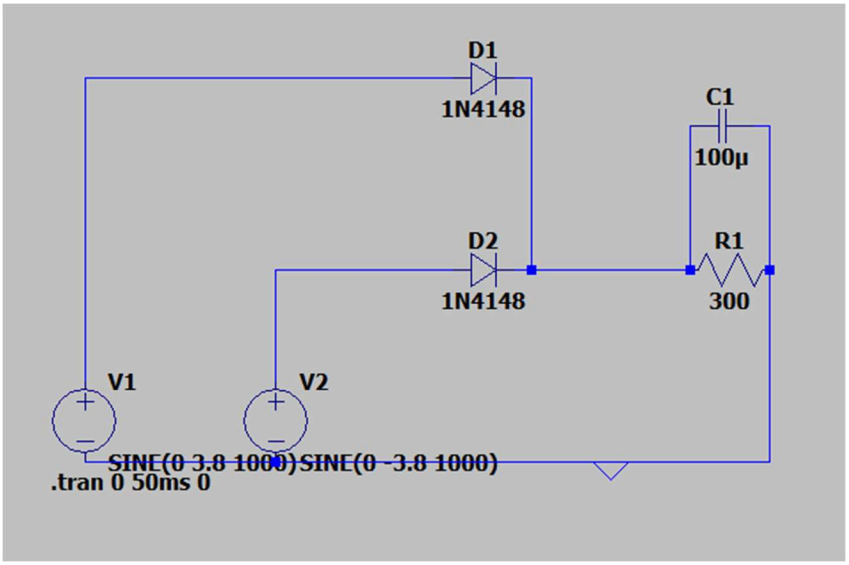
Filter:

The filter used in this design is a single capacitor. The purpose of the filter is to smoothen the signal that comes out of the rectifier. The value of the capacitor used in this design was calculated to be 100 uF. This specific capacitor is the 107M which as a voltage rating of 6.3 V.

Regulator:

A regulator was not used in this design since the targeted output voltage and current was achieved without one. Adding one would add no significant value to the design and may even hinder the simplicity of it.

Circuit Schematic:



Calculations:

$$V_{peak\text{-}to\text{-}peak} = V_{RMS} * 2\sqrt{2}$$
$$= 120 * 2\sqrt{2}$$
$$= 339.4\ V$$

$$V_{peak} = V_{peak\text{-}to\text{-}peak} / 2$$
$$= \frac{339.4}{2}$$
$$= 169.7\ V$$

$$\text{Turns Ratio} = \frac{V_{in\text{-}peak}}{V_{out\text{-}peak}}$$
$$= \frac{169.7\ V}{8\ V}$$
$$= 21:1$$

Capacitor Value:

$$V_{pp} = \frac{I_{out}}{fC} \qquad V_{pp} = 0.1\ V,\ I_{out} = 10\ mA,\ f = 1\ KHz$$
$$C = \frac{10\ mA}{(0.1\ V)(1\ KHz)}$$
$$= 100\ \mu F$$

Expected Performance:

The input voltage for the rectifier was chosen to be 8 V for this design. Since the design implements a full-wave center-tapped transformer, the 8 V input is divided into two 4 V inputs. This input in combination with a 100 uF capacitor and 300-ohm resistor is expected to create an output DC voltage of 3 V and current of 10 mA.

Design Trade-offs, Margins, and Safety:

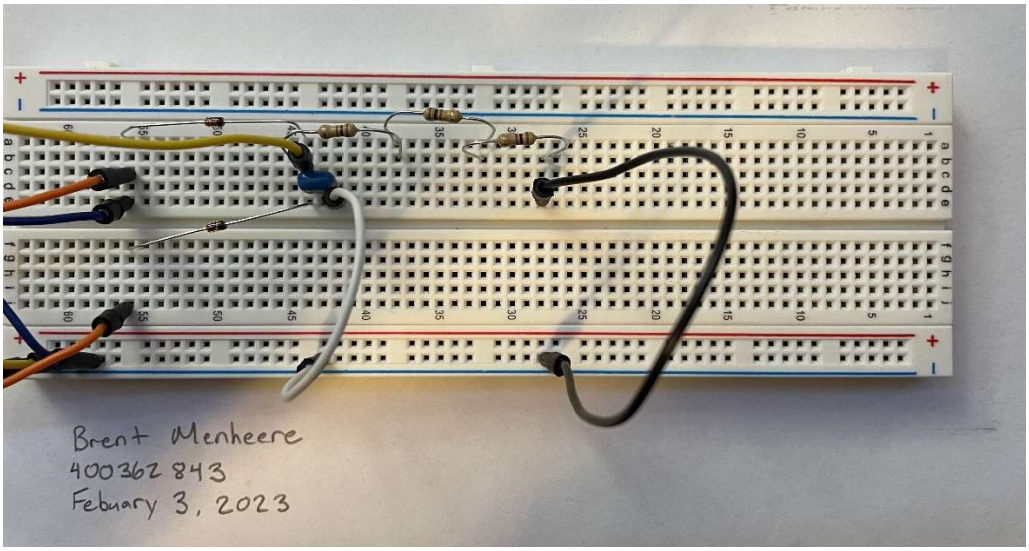
The biggest design trade-off in this project is the choice of rectifier. There were three options for rectifier topology to be used in this design; half-wave, full-wave bridge, and full-wave center-tapped transformer. A half-wave rectifier captures only the positive or negative part of the AC wave. To capture the most out of the AC signal, a full-wave design needs to be used. In the end the choice to use a full-wave center-tapped transformer was made because of the simplicity in implementing it physically into the circuit. A

full-wave bride rectifier uses a total of four diodes, while a full-wave center-tapped transformer only uses two. However, a full-wave bridge rectifier does not need a centre-tapper transformer, and thus in our circuit could be implemented with only one AC voltage source.

One safety issue that was considered in this design is the rating of the capacitor used. When a capacitor is exposed to a voltage greater than it is rated for it has the possibility of breaking down and exploding. Before implementing a capacitor into the physical circuit research was done on the 107M 100 uF capacitor and was found to have a voltage rating of 6.3 V. This component was deemed to be safe to use as the Analog Discovery 2 has the ability to put out a maximum of 5 V.

Measurement and Analysis:

Actual Circuit:



Measurement Procedure:

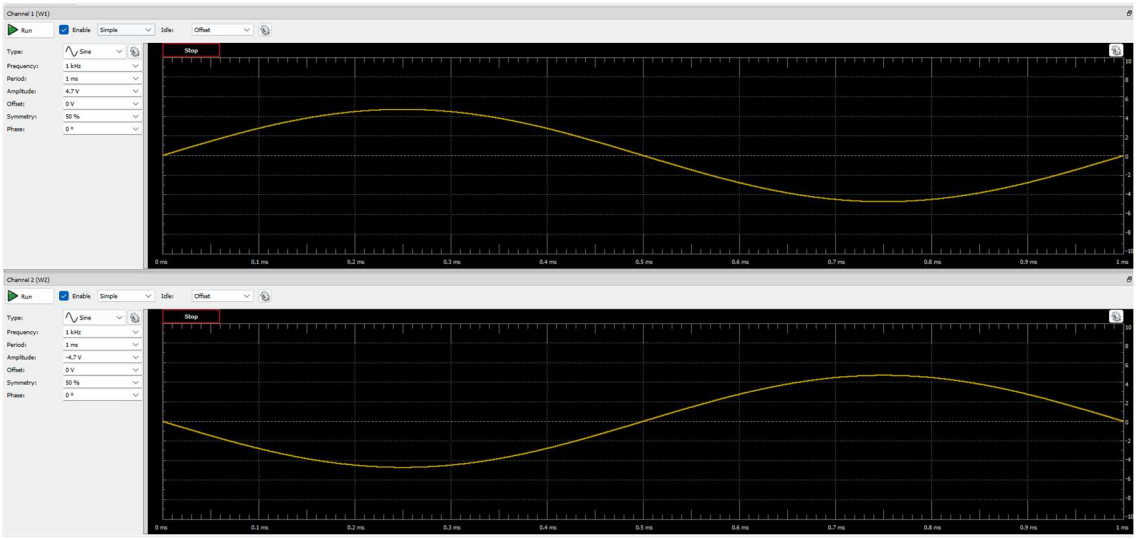
The performance of this design was determined by measurements taken on Waveforms with the Analog Discovery 2. Initially with the input voltage chosen earlier, the output voltage was too low. After various changes in the input, the correct voltage to be used was 4.7 V and -4.7 V. With the oscilloscope feature, the input AC signal was measured on channel 1, the DC output signal was measured on channel 2, and the current through the resistor load was measure using a custom math function. To confirm that the DC signal was 3 ± 0.1 V, the measurements tool was used to calculate the precise maximum and minimum voltage. This tool was also used to confirm that the current was at 10 mA with an acceptable amount of variation.

Key Measurements:

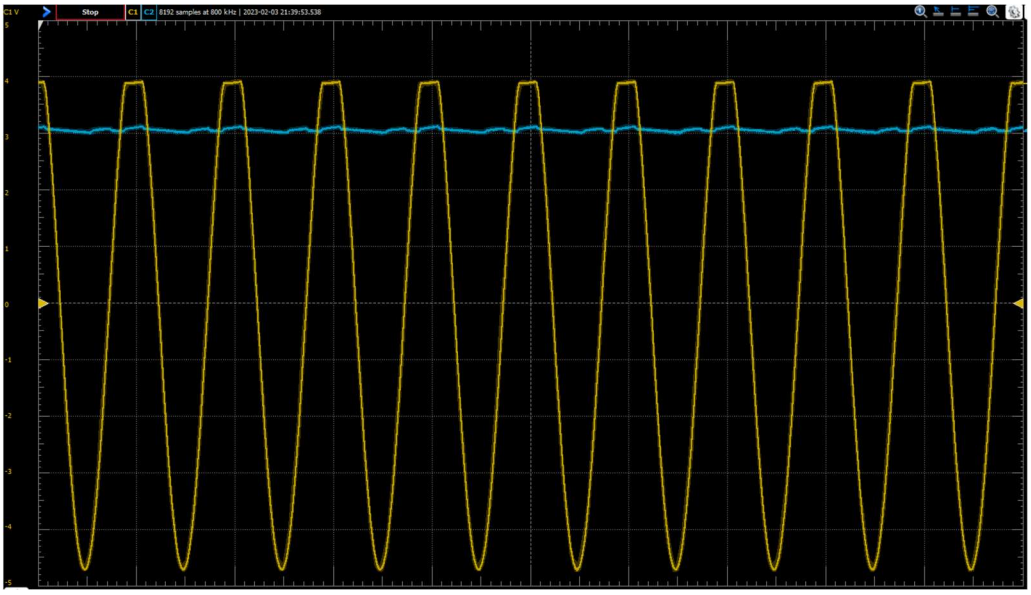
C2	Maximum	3.0825 V	M1	Maximum	10.423 mA
C2	Minimum	2.9935 V	M1	Minimum	9.9784 mA

Oscilloscope:

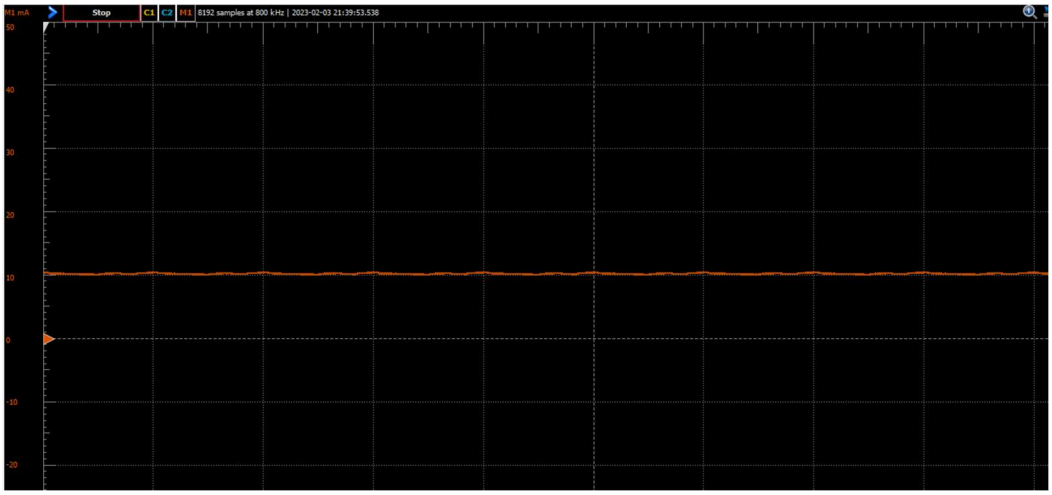
Input Waves:



DC wave (blue) with Input Wave (yellow):

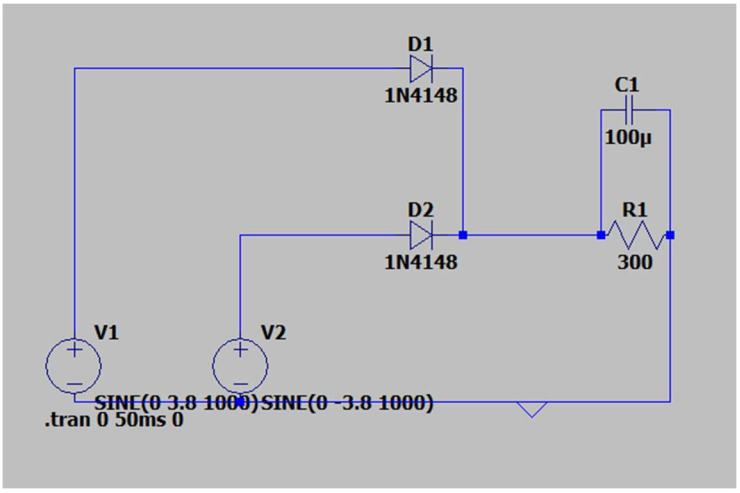


Current:



Simulation:

Circuit Schematic:



Netlist:

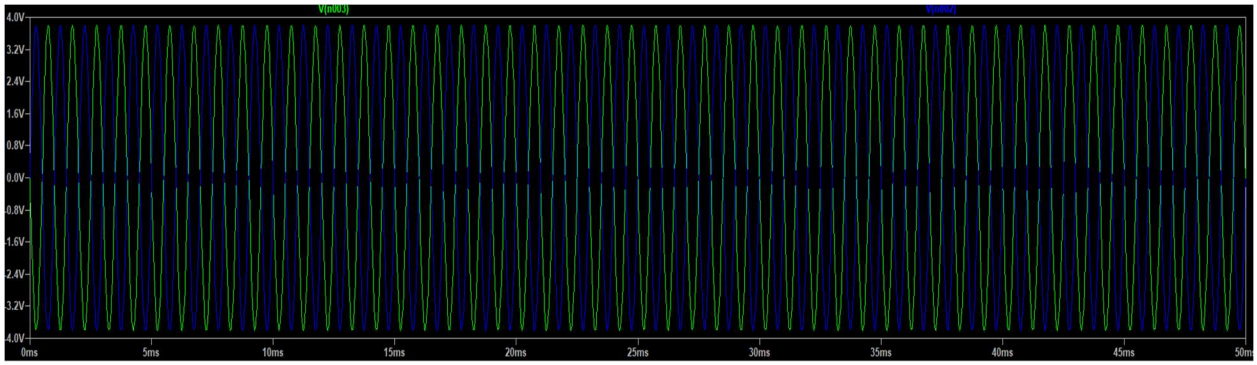
```
* C:\Users\brent\OneDrive\Desktop\2EI4\project 1.asc
V1 N002 0 SINE(0 3.8 1000)
V2 N003 0 SINE(0 -3.8 1000)
D1 N002 N001 1N4148
D2 N003 N001 1N4148
R1 N001 0 300
C1 0 N001 100µ
.model D D
.lib C:\Users\brent\AppData\Local\LTspice\lib\cmp\standard.dio
.tran 0 50ms 0
.backanno
.end
```

Simulation Conditions:

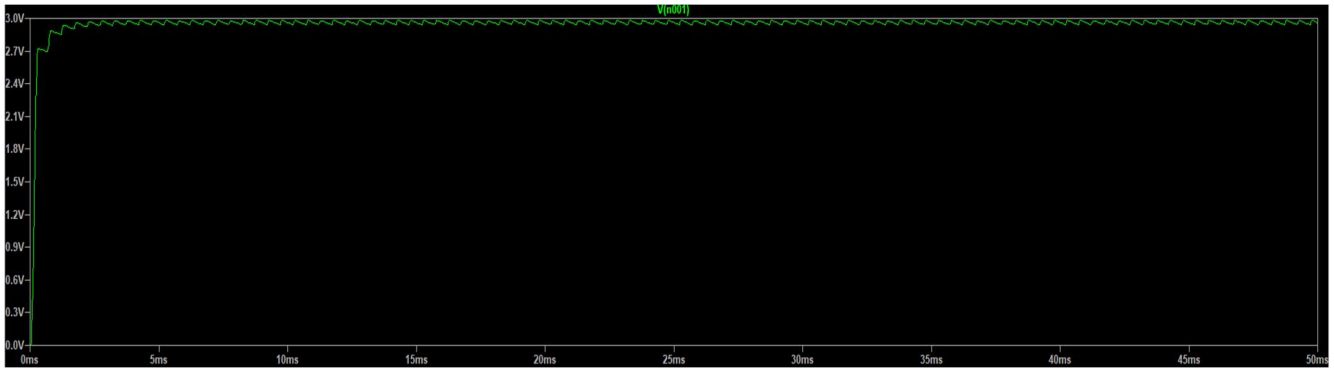
A transient simulation was run in the LTSpice software. The simulation parameters were chosen to be a 50 ms stop time and data to be saved at 0 s. The stop time was chosen to be 50 ms since it produced a graph that showed an appropriate amount of detail in the waves.

Simulation Output:

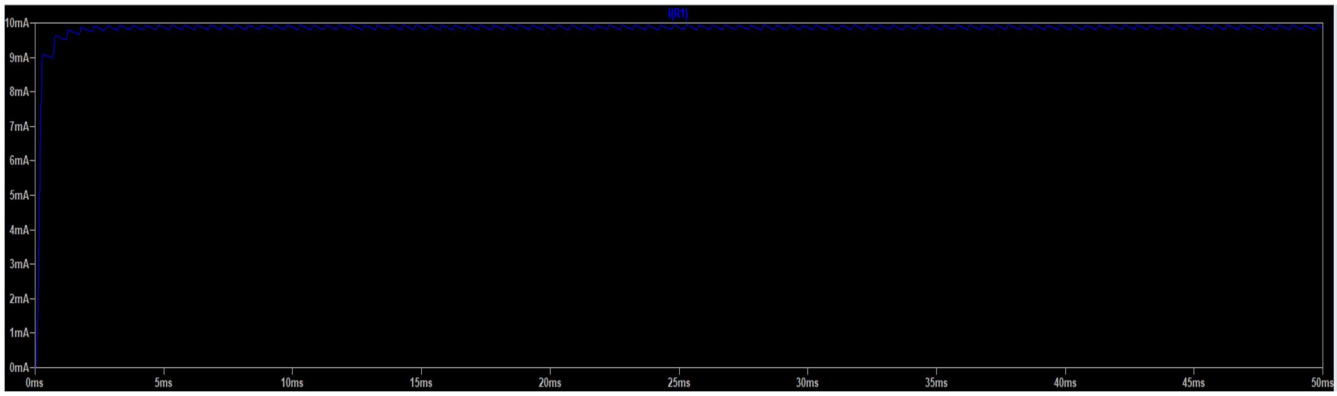
Input Voltages:



Output Voltage:



Output Current (blue line, a little tough to see but its there!):



Discussion:

Comparison:

In the original design, the input voltage was chosen to be 8 V, which was then split into to two 4 V sources because of the nature of the center-tapped transformer. When the design was implemented on the LTSpice simulation, 4 V for each source produced an output voltage slightly too high. Which led to the simulated voltage to be changed to 3.8 V each, which produced an ideal DC output voltage. After the design was deemed to be safe and functional on a simulation, it was implemented into a physical circuit. Originally the AD2 was set to the same parameters as the simulation, however this produced an output voltage far too low. After trial and error, the ideal input voltage for each of the sources was chosen to be 4.7 V. The current measured or calculated in any of the steps tended to be consistently around 10 mA.

Discrepancies Observed:

All discrepancies observed in this project are to be expect when comparing theoretical, simulated, and experimental results together. The initial chosen voltage of 4 V per source was purely chosen as a starting point to create simulation calculations. Once implemented into LTSpice it was expected that the input voltage would change slightly. Along with this, the discrepancy between the simulated and experimental voltage is expected when using physical electrical components. A common source for experimental error in experiments like this one is unaccounted for resistance.

Limitations:

The biggest limitation of this design is that it can not be used in this configuration to output a DC voltage much larger than the one we currently output. At the moment, the physical implementation of this design takes in two 4.7 V sources to produce a 3 V DC output, however the max voltage that we can input into our design's sources from the AD2 is 5 V. This limits our output around 3 V. If we were to obtain another source that was capable of outputting more than 5 V, we would then have issues with the components of the design. The capacitor used is rated for a max voltage of 6.3 volts. Any voltage greater than this would pose a potential safety hazard and could destroy the circuit.

Problems Encountered:

During the physical implementation of the converter design, I encountered an issue where my DC output voltage had a larger than acceptable amplitude of almost 1 V. After lots of trouble shooting, which included changing values and rebuilding the circuit multiple times, I had come to the conclusion that my circuit was not consistently grounded. My connections were not full touching in some places. To fix this issue, I minimized the use of jumper wires to mitigate the chances of faulty connections. Where jumper wires were used, I held them down to ensure contact while taking measurements.