W65C51N
Asynchronous Communications Interface Adapter (ACIA)

DOCUMENT REVISION HISTORY

Version	Date	Author	Description
1.0	26-May-17	Bill Mensch and David Gray	Initial Document Entry
1.1	7-June-17	Bill Mensch and David Gray	Simplified functional explanation and reduced figures based on actual operation of the device. Added Table of Contents.
1.1	16-June-17	Bill Mensch and David Gray	Fixed typo on page 6 for package types replacing W65C51S with W65C51N
1.1	8-April-20	Bill Mensch and David Gray	Added 115.2K baud rate as 1.8432MHz/16 to communications frequencies for clarity.

Table of Contents

INTRODUCTION

The WDC CMOS W65C51N Asynchronous Communications Interface Adapter (ACIA) provides an easily implemented, program controlled interface between 8-bit microprocessor based systems and serial communication data sets and modems.

The ACIA has an internal baud rate generator. This feature eliminates the need for multiple component support circuits, a crystal being the only other part required. The Transmitter baud rate can be selected under program control to be either 1 of 16 different rates from 50 to 115.2K at 1/16 times a clock rate with 1.8432MHz XTLI. The Receiver baud rate may be selected under program control to be either the Transmitter rate or at 1/16 times the external clock rate. The ACIA has programmable word lengths of 5, 6, 7 or 8 bits no parity, and 1, 1½ or 2 bit stops.

The ACIA is designed for maximum-programmed control from the microprocessor (MPU) to simplify hardware implementation. Three separate registers permit the MPU to easily select the W65C51N operating modes and data checking parameters and determine operational status.

The Command Register controls receiver echo mode, the state of the RTSB line, receiver interrupt control and the state of the DTRB line.

The Control Register controls the number of stop bits, word length, and receiver clock source and baud rate.

The Status Register indicates the states of the IRQB, DSRB, and DCDB lines, Transmitter and Receiver Data Registers and Overrun, Framing and Parity Error conditions.

When the Transmitter Data Register (TDR) is written to it also writes to the Transmitter Shift Register (TSR). This function is different than previous 6551 ACIAs. The Receiver Shift Register (RSR) is transferred to the Receiver Data Register (RDR) after completing the shifting in of a word. A new word can begin shifting in thus providing one byte of data buffering. If the RDR is not read before the next byte is transferred to the RDR, an overrun condition is flagged.

FEATURES

- Low power CMOS N-well silicon gate technology
- Full duplex operation with buffered receiver, transmitter is not buffered
- Data set/modem control functions
- Internal baud rate generator with 16 programmable baud rates (50 to 115..2K)
- Program-selectable internally or externally controlled receiver rate
- Programmable word lengths, number of stop bits and parity bit generation and detection
- Programmable interrupt control
- Program reset
- Program-selectable serial echo mode
- Two chip selects
- 5.0 VDC ± 5% supply requirements
- 28 pin plastic DIP package
- 28 pin PLCC package end of life package type and not suggested for new designs
- 32 pin QFP package SMT package type suggested for new designs
- Full TTL compatibility
- Compatible with 65xx and 68xx microprocessors

PACKAGE PIN OUT DIAGRAMS

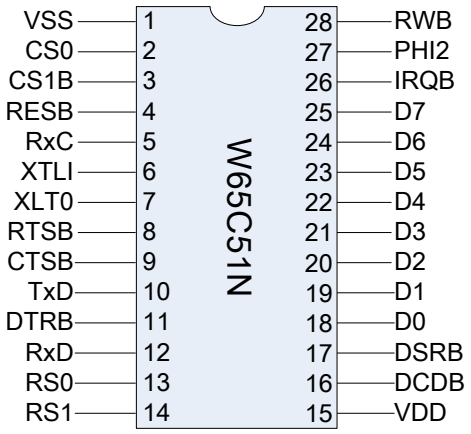


Figure 1a. 28 Pin PDIP Pin out

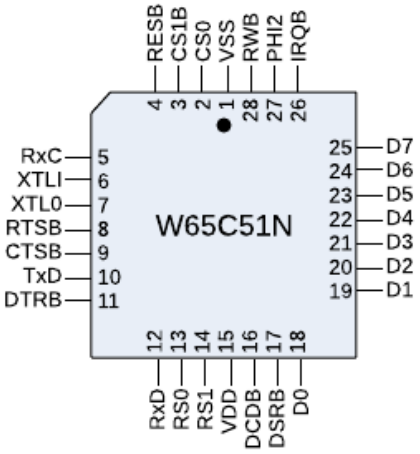


Figure 1b. 28 Pin PLCC Pin Out
(EOL use QFP)

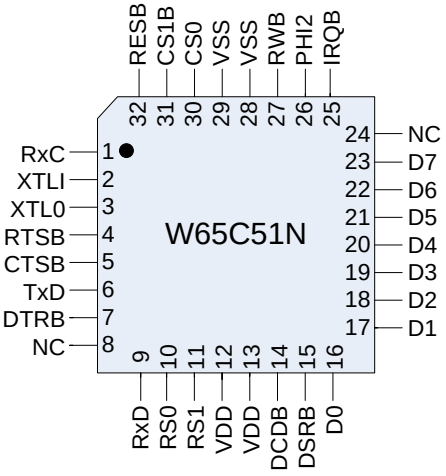


Figure 1c. 32 Pin LQFP Pin Out

W65C51N6T PACKAGE TYPES:

The current production tested parts are provided in a PDIP28, PLCC28, and QFP32 packages. The PLCC28 package is only available in very limited quantities due to packaging obsolescence from our supplier.

ACIA INTERNAL ORGANIZATION

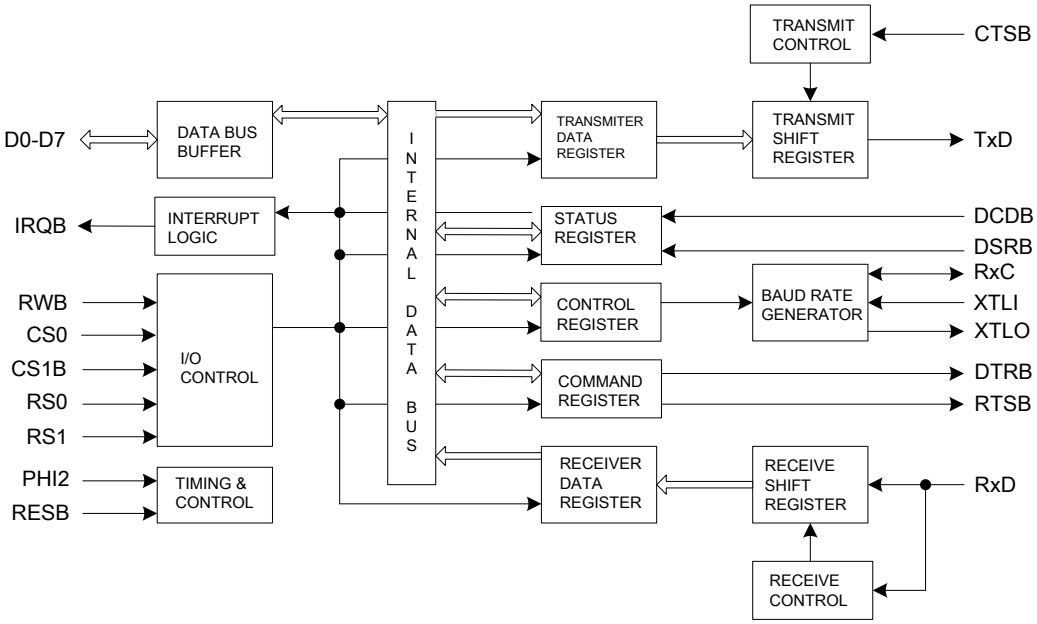


Figure 2. ACIA Internal Organization

FUNCTIONAL DESCRIPTION

The internal organization of the ACIA is presented in Figure 2 followed by a description of each functional element of the device.

DATA BUS BUFFERS

The Data Bus Buffer interfaces the system data lines to the internal data bus. The Data Bus Buffer is bi-directional. When the RWB line is high and the chip is selected, the Data Bus Buffer passes the data from the system data lines to the ACIA internal data bus. When the RWB line is low and the chip is selected, the Data Bus Buffer writes the data from the internal data bus to the system data bus.

INTERRUPT LOGIC

The Interrupt Logic will cause the IRQB line to the microprocessor to go low when conditions are met that require the attention of the microprocessor. The conditions which can cause an interrupt will set bit 7 and the appropriate bit of bits 3 through 6 in the Status Register, if enabled. Bits 5 and 6 correspond to the Data Carrier Detect (DCDB) logic and the Data Set Ready (DSRB) logic with bit 3 corresponding to the Receiver Data Register full. These conditions can cause an interrupt request if enabled by the Command Register Bit 4 indicates a Transmitter Data Register empty condition. The Transmitter Interrupt should never be enabled because the Transmitter Shift Register (TSR) is written when the TDR is written.

I/O CONTROL

The I/O Control Logic controls the selection of internal registers in preparation for a data transfer on the internal data bus and the direction of the transfer to or from the register. The registers are selected by the Register Select (RS1, RS0) and Read/Write (RWB) lines as described later in Table 1.

TIMING AND CONTROL

The Timing and Control logic controls the timing of data transfers on the internal data bus and the registers, the Data Bus Buffer and the microprocessor data bus and hardware reset features.

Timing is controlled by the system PHI2 clock input. The chip will perform data transfers to or from the microcomputer data bus during the PHI2 high period when selected.

The Timing and Control Logic will initialize all registers when the Reset (RESB) line goes low. See the individual register description for the state of the registers following a hardware reset.

TRANSMITTER AND RECEIVER DATA REGISTERS

Both the Transmitter and Receiver are selected by a Register Select 0 (RS0) and Register Select 1 (RS1) low condition. The Read/Write (RWB) line determines which actually uses the internal data bus; the Transmitter Data Register is write only and the Receiver Data Register is read only.

Bit 0 is the first bit to be transmitted from the Transmitter Shift Register (least significant bit first). The higher order bits follow in order. Unused bits in this register are “don’t care”.

The Receiver Data Register holds the first received data bit in bit 0 (least significant bit first). Unused high-order bits are “0”. The W65C51N does not offer parity for transmission or reception.

STATUS REGISTER

The Status Register indicates the state of interrupt conditions and other non-interrupt status lines. The interrupt conditions are the Data Set Ready, Data Carrier Detect, Transmitter Data Register Empty (see note below) and Receiver Data Register Full as reported in bits 6 through 3, respectively. If any of these bits are set the interrupt (IRQ) indicator (bit 7) is also set. Overrun, Framing Error and Parity Error are also reported (bits 2 through 0 respectively).

7	6	5	4	3	2	1	0
IRQ	DSRB	DCDB	TDRE	RDRF	OVRN	FE	PE

Bit 7	Interrupt (IRQ)
0	No Interrupt
1	Interrupt has occurred
Bit 6	**Data Set Ready (DSRB)**
0	DSR low (ready)
1	DSR high (not ready)
Bit 5	**Data Carrier Detect (DCDB)**
0	DCD low (detected)
1	DCD high (not detected)
Bit 4	**Transmitter Data Register Empty***
0	Never 0 During transmission
1	Empty
Bit 3	**Receiver Data Register Full**
0	Not full
1	Full
Bit 2	**Overrun**
0	No overrun
1	Overrun has occurred
Bit 1	**Framing Error**
0	No framing error
1	Framing error detected
Bit 0	**Parity Error**
0	No parity error
1	Parity error detected

Reset Initialization

7	6	5	4	3	2	1	0	
0	-	-	1	0	0	0	0	Hardware reset
-	-	-	-	-	0	-	-	Program reset

***Note:**
The W65C51N loads the Transmitter Data Register (TDR) and Transmitter Shift Register (TSR) at the same time. A delay should be used to insure that the shift register is empty before the TDR/TSR is reloaded. This feature of the W65C51N works different from earlier 6551 designs. The Command and Control Registers should be set up first before transmission begins when writing the TDR/TSR.

STATUS REGISTER BIT DESCRIPTION

Parity is never enabled (Bit 0) Framing Error (Bit 1) and Overrun (Bit 2)

None of these bits causes a processor interrupt to occur but, they are normally checked at the time the Receiver Data Register is read so that the validity of the data can be verified. These bits are self-clearing (i.e., they are automatically cleared after a read of the Receiver Data Register).

Receiver Data Register Full (Bit 3)

This bit goes to a 1 when the ACIA transfers data from the Receiver Shift Register to the Receiver Data Register and goes to a 0 (is cleared) when the processor reads the Receiver Data Register.

Transmitter Data Register Empty (Bit 4)

The Transmitter Data Register Empty (TDRE) bit is always a 1 because the TSR is loaded when the TDR is written to. TDRE bit cannot be polled to determine when to write the next byte to the TDR/TSR. A delay loop should be used to gate the writing to the TDR/TSR. Transmitter Interrupts should never be enabled.

Data Carrier Detect (Bit 5) and Data Set Ready (Bit 6)

These bits reflect the levels of the DCDB and DSRB inputs to the ACIA. A 0 indicates a low level (true condition) and a 1 indicates a high level (false). Whenever either of these inputs change state, an immediate processor interrupt (IRQ) occurs, unless bit 1 of the Command Register (IRD) is set to a 1 to disable IRQB. When the interrupt occurs, the status bits indicate the levels of the inputs immediately after the change of state occurred. Subsequent level changes will not affect the status bits until the Status Register is interrogated by the processor. At that time, another interrupt will immediately occur and the status bits reflect the new input levels. These bits are not automatically cleared (or reset) by an internal operation.

Interrupt (Bit 7)

This bit goes to a 1 whenever an interrupt condition occurs and goes to a 0 (is cleared) when the Status Register is read.

CONTROL REGISTER

The Control Register selects the desired baud rate, frequency source, word length and the number of stop bits.

7	6	5	4	3	2	1	0
SBN	WL1	WL0	RSC	SBR3	SBR2	SBR1	SBR0

Bit 7	Stop Bit Number (SBN)
0	1 Stop bit
1	2 Stop bits
1	1 ½ Stop bits For WL = 5

Bit 6	Bit 5	Word Length (WL) No. Bits
0	0	8
0	1	7
1	0	6
1	1	5

Bit 4	Receiver Clock Source (RCS)
0	External receiver clock
1	Baud rate

Bit 3-0 Selected Baud Rate(SBR)				
3	2	1	0	Baud
0	0	0	0	115.2K (1.8432MHz/16)
0	0	0	1	50
0	0	1	0	75
0	0	1	1	109.92
0	1	0	0	134.58
0	1	0	1	150
0	1	1	0	300
0	1	1	1	600
1	0	0	0	1200
1	0	0	1	1800
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200

Reset Initialization

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Hardware reset (RESB)
-	-	-	-	-	-	-	-	Program reset

CONTROL REGISTER BIT DESCRIPTION

Selected Baud Rate (Bits 0, 1, 2, 3)

These bits select the Transmitter baud rate, which can be at XTLI/16 or one of 15 other rates controlled by the internal baud rate generator.

If the Receiver clock uses the same baud rate at the transmitter, then RxC becomes an output and can be used to slave other circuits to the ACIA.

Receiver Clock Source (Bit 4)

This bit controls the clock source to the Receiver. A 0 causes the Receiver to operate at a baud rate of 1/16 an XTLI external clock. A 1 causes the Receiver to operate at the same baud rate as is selected for the transmitter.

Word Length (Bits 5, 6)

These bits determine the word length to be used (5, 6, 7 or 8 bits).

Stop Bit Number (Bit 7)

This bit determines the number of stop bits used. A 0 always indicates one stop bit. A 1 indicates 1½ stop bits if the word length is 5 and 2 stop bits in all other configurations.

COMMAND REGISTER

The Command Register controls specific modes and functions

7	6	5	4	3	2	1	0
PMC1	PMC0	PME	REM	TIC1	TIC0	IRD	DTR

Bit 7	Bit 6	Parity Mode Control (PMC)
0	0	Use but no parity
0	1	Use but no parity
1	0	Use but no parity
1	1	Use but no parity

Bit 5	Parity Mode Enabled (PME)
0	Parity disabled
1	Do not enable parity

Bit 4	Receiver Echo Mode (REM)
0	Receiver normal mode
1	Receiver echo mode bits 2 and 3 Must be zero, RTS will be low

Bit 3	Bit 2	Transmitter Interrupt Control (TIC)
0	0	RTSB = High, transmit interrupt disabled
0	1	Do not use
1	0	RTSB = Low, transmit interrupt disabled
1	1	RTSB = Low, transmit interrupt disabled Transmit break on TxD

Bit 1	Receiver Interrupt Request Disabled (IRD)
0	IRQB enabled
1	IRQB disabled

Bit 0	Data Terminal Ready (DTR)
0	Data terminal not ready (DTRB high)
1	Data terminal ready (DTRB low)

Reset Initialization

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	**Hardware reset (RESB)**
-	-	-	0	0	0	0	0	**Program reset**

COMMAND REGISTER BIT DESCRIPTION

Data Terminal Ready (Bit 0)

This bit enables all selected interrupts and controls the state of the Data Terminal Ready (DTRB) line. A 0 indicates the microcomputer system is not ready by setting the DTRB line high. A 1 indicates the microcomputer system is ready by setting the DTRB line low.

Receiver Interrupt Control (Bit 1)

This bit disables the Receiver from generating an interrupt when set to a 1. The Receiver interrupt is enabled when this bit is set to a 0 and Bit 0 is set to a 1.

Transmitter Interrupt Control (Bits 2, 3)

These bits control the state of the Ready to Send (RTSB) line.

Receiver Echo Mode (Bit 4)

A 1 enables the Receiver Echo Mode and a 0 enables the Receiver Echo Mode. When bit 4 is a 1 bits 2 and 3 must be 0. In the Receiver Echo Mode, the Transmitter returns each transmission received by the Receiver delayed by one-half bit time.

Parity Mode Enable (Bit 5)

This bit should always be 0 on the W65C51N disabling parity bit generation by the Transmitter and parity bit checking by the Receiver.

Parity Mode Control (Bits 6, 7)

Parity should always be disabled on the W65C51N so any combination of these bits is acceptable.

INTERFACE SIGNALS

Figure 3 shows the ACIA interface signals associated with the microprocessor and the modem.

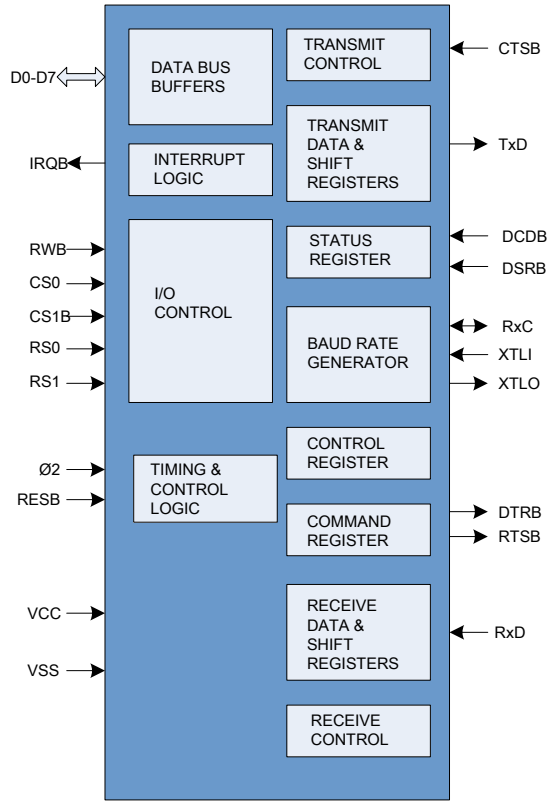


Figure 3 ACIA Interface Diagram

MICROPROCESSOR INTERFACE

Reset (RESB)

During System initialization a low on the RESB input causes a hardware reset to occur. Upon reset, the Command Register and the Control Register are cleared (all bits set to 0). The Status Register is cleared with the exception of the indications of Data Set Ready and Data Carrier Detect, which are externally controlled by the DSRB and DCDB lines, and the transmitter Empty bit, which is set. RESB must be held low for one PHI2 clock cycle for a reset to occur.

Input Clock (PHI2)

The input clock is the system PHI2 clock and clocks all data transfers between the system microprocessor and the ACIA.

Read/Write (RWB)

The RWB input, generated by the microprocessor controls the direction of data transfers. A high on the RWB pin allows the processor to read the data supplied by the ACIA, a low allows a write to the ACIA.

Interrupt Request (IRQB)

The IRQB pin is an interrupt output from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common IRQB microprocessor input. Normally a high level, IRQB goes low when an interrupt occurs.

Data Bus (D0-D7)

The eight data line (D0-D7) pins transfer data between the processor and the ACIA. These lines are bi-directional and are normally high-impedance except during Read cycles when the ACIA is selected.

Chip Selects (CS0, CS1B)

The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The ACIA is selected when CS0 is high and CS1B is low. When the ACIA is selected, the internal registers are addressed in accordance with the register select lines (RS0, RS1).

Register Selects (RS0, RS1)

The two register select lines are normally connected to the processor address lines to allow the processor to select the various ACIA internal registers. Table 1 shows the internal register select coding.

RS1	RS0	Register Operation	
		RWB = Low	RWB = High
L	L	Write Transmit Data/Shift Register	Read Receiver Data Register
L	H	Programmed Reset (Data is “Don’t Care”)	Read Status Register
H	L	Write Command Register	Read Command Register
H	H	Write Control Register	Read Control Register

Table 1 ACIA Register Selection

Only the Command and Control registers can both be read and written. The programmed Reset operation does not cause any data transfer, but is used to clear bits 4 through 0 in the Command Register and bit 2 in the Status Register. The Control Register is unchanged by a programmed Reset. It should be noted that the programmed Reset is slightly different from the hardware Reset (RESB); refer to the register description.

ACIA/MODEM INTERFACE

Crystal Pins (XTLI, XTLO)

These pins are normally directly connected to the external crystal (1.8432 MHz) to derive the various baud rates. Alternatively, an externally generated clock can drive the XTLI pin, in which case the XTLO pin must float. XTLI is the input pin for the transmit clock.

Transmit Data (TxD)

The TxD output line transfers serial non-return-to-zero (NRZ) data to the modem. The least significant bit (LSB) of the Transmit Data/Shift Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected or under control of an external clock. This selection is made by programming the Control Register.

Receive Data (RxD)

The RxD input line transfers serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or under the control of an externally generated receiver clock. The selection is made by programming the Control Register.

Receive Clock (RxC)

The RxC is a bi-directional pin which is either the receiver 16x clock input or the receiver 16x clock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking. When Bit 4 of the Control Register selects the baud rate generator as the Receiver clock source RxC becomes an output.

Request to Send (RTSB)

The RTSB output pin controls the modem from the processor. The state of the RTSB pin is determined by the contents of the Command Register.

Clear to Send (CTSB)

The CTSB input pin controls the transmitter operation. The enable state is with CTSB low. The transmitter is automatically disabled if CTSB is high.

Data Terminal Ready (DTRB)

This output pin indicates the status of the ACIA to the modem. A low on DTRB indicates the ACIA is enabled, a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

Data Set Ready (DSRB)

The DSRB input pin indicates to the ACIA the status of the modem. A low indicates the “ready” state and a high, “not-ready”

Data Carrier Detect (DCDB)

The DCDB input pin indicates to the ACIA the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high that it is not.

Table 2 Divisor Selection

Control Register Bits 3 2 1 0	Divisor Selected for the Internal Counter	Baud Rate Generated With 1.8432MHz Crystal	Baud Rate Generated With a Crystal of Frequency (F)
0 0 0 0	16	$\frac{1.8432 \times 10^6}{16} = 115200$	$\frac{F}{16}$
0 0 0 1	36,864	$\frac{1.8432 \times 10^6}{36,864} = 50$	$\frac{F}{36,864}$
0 0 1 0	24,576	$\frac{1.8432 \times 10^6}{24,576} = 75$	$\frac{F}{24,576}$
0 0 1 1	16,769	$\frac{1.8432 \times 10^6}{16,769} = 109.92$	$\frac{F}{16,769}$
0 1 0 0	13,704	$\frac{1.8432 \times 10^6}{13,704} = 134.51$	$\frac{F}{13,704}$
0 1 0 1	12,288	$\frac{1.8432 \times 10^6}{12,288} = 150$	$\frac{F}{12,288}$
0 1 1 0	6,144	$\frac{1.8432 \times 10^6}{6,144} = 300$	$\frac{F}{6,144}$
0 1 1 1	3,072	$\frac{1.8432 \times 10^6}{3,072} = 600$	$\frac{F}{3,072}$
1 0 0 0	1,536	$\frac{1.8432 \times 10^6}{1,536} = 1,200$	$\frac{F}{1,536}$
1 0 0 1	1,024	$\frac{1.8432 \times 10^6}{1,024} = 1,800$	$\frac{F}{1,024}$
1 0 1 0	768	$\frac{1.8432 \times 10^6}{768} = 2,400$	$\frac{F}{768}$
1 0 1 1	512	$\frac{1.8432 \times 10^6}{512} = 3,600$	$\frac{F}{512}$
1 1 0 0	384	$\frac{1.8432 \times 10^6}{384} = 4,800$	$\frac{F}{384}$
1 1 0 1	256	$\frac{1.8432 \times 10^6}{256} = 7,200$	$\frac{F}{256}$
1 1 1 0	192	$\frac{1.8432 \times 10^6}{192} = 9,600$	$\frac{F}{192}$
1 1 1 1	96	$\frac{1.8432 \times 10^6}{96} = 19,200$	$\frac{F}{96}$

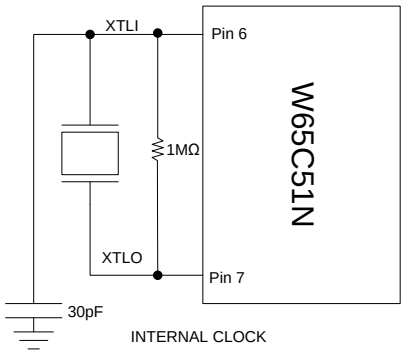


Figure 4a Clock Generation (Internal Clock Option)
Pin Numbers for PDIP and PLCC only

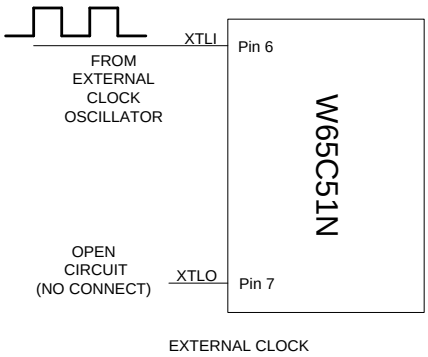


Figure 4b Clock Generation (External Clock Option)
Pin Numbers for PDIP and PLCC only

CRYSTAL AND CLOCK OPTIONS FOR XTLI/XTLO

The W65C51N has an internal baud rate generator that drives asynchronous communications. XTLI and XTLO are the crystal input/output pins that are using for providing the clock system to the baud rate generator. Figure 4 shows two setup options for the baud rate generator clock. The Internal Clock setup (Figure 4a) is for a crystal with 1Mohm resistor and 30pF capacitor to drive the ACIA's internal oscillator circuit. The external clock setup (Figure 4b) is for using an external clock oscillator output hooked to XTLI and XTLO is not connected.

Test and Crystal Specifications

1. Temperature stability ± 0.01% (-40° C to +85° C)
2. Characteristics at 25° C ± 2° C
   a. Frequency (MHz) 1.8432
   b. Frequency tolerance (± %) 0.02
   c. Resonance mode Series
   d. Equivalent resistance (ohm) 400 max.
   e. Drive level (mW) 2
   f. Shunt capacitance (pF) 7 max.
   g. Oscillation mode Fundamental

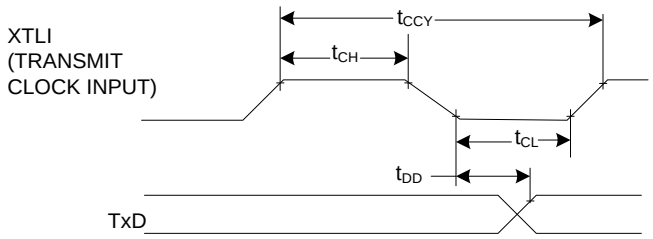
TIMING DIAGRAMS AND CHARACTERISTICS

Timing diagrams for transmit with external clock, receive with external clock and IRQB generation are shown in Figures 5, 6 and 7 respectively. The corresponding timing characteristics are listed in Table 3.

Table 3 Transmit/Receive Characteristics

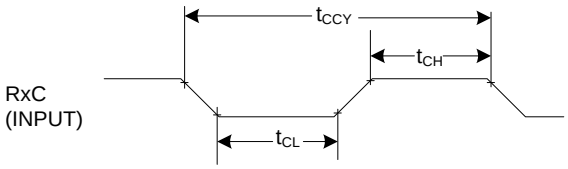
Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Transmit/Receive Clock Rate	t_{CCY}	400*	-	400*	-	nS
Transmit/Receive Clock High Time	t_{CH}	175	-	175	-	nS
Transmit/Receive Clock Low Time	t_{CL}	175	-	175	-	nS
XTLI to TxD Propagation Delay	t_{DD}	-	500	-	500	nS
RTS Propagation Delay	t_{DLY}	-	500	-	500	nS
IRQB Propagation Delay (Clear)	t_{IRQ}	-	500	-	500	nS

Notes:
1. (t_R, t_F = 10 to 30 nS)
*The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times t_{CCY}}$



NOTE: TxD RATE IS 1/16 TxC RATE

Figure 5 Transmit Timing with External Clock



NOTE: RxD RATE IS 1/16 RxC RATE

Figure 6 Receive External Clock Timing

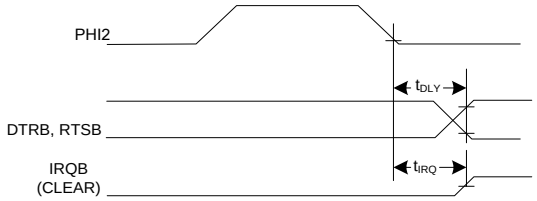


Figure 7 Interrupt and Output Timing

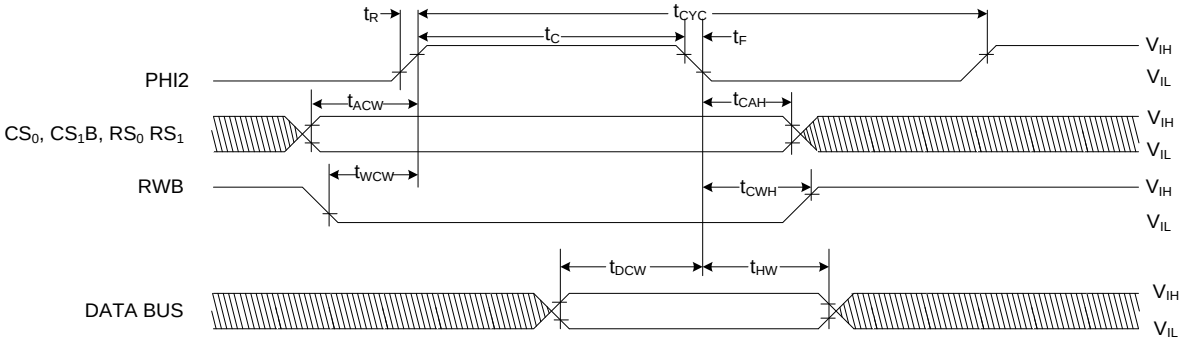


Figure 8 Write Timing Diagram

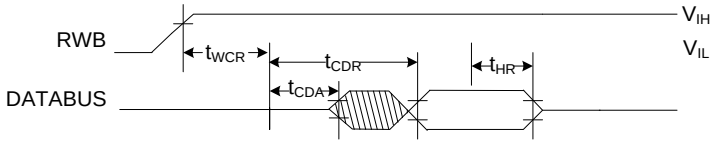


Figure 9 Read Timing Characteristics

Parameter	Symbol	2 MHz		4 MHz		Units
		Min	Max	Min	Max	
PHI2 Cycle Time	t_{CYC}	500	-	250	-	nS
PHI2 Pulse Width	t_C	200	-	100	-	nS
Address Set-Up Time	t_{AC}	60	-	30	-	nS
Address Hold Time	t_{CAH}	0	-	0	-	nS
RWB Set-Up Time	t_{WC}	60	-	30	-	nS
RWB Hold Time	t_{CWH}	0	-	0	-	nS
Data Bus Set-Up time	t_{DCW}	60	-	35	-	nS
Data Bus Hold Time	t_{HW}	10	-	5	-	nS
Read Access Time (Valid Data)	t_{CDR}	-	150	-	50	nS
Read Hold Time	t_{HR}	10	-	10	-	nS
Bus Active Time (Invalid Data)	t_{CDA}	20	-	10	-	nS

Notes:
1. V_{CC} = 5.0V ± 5%
2. $T_A = T_L$ to T_H
3. t_R and t_F = 10 to 30 nSs.

Table 4 AC Characteristics

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0V	Vdc
Input Voltage	V_{IN}	-0.3 to V_{CC} +0.3	Vdc
Output Voltage	V_{OUT}	-0.3 to V_{CC} +0.3V	Vdc
Operating Temp. Commercial Industrial	T_A	 0 to +70 -40 to +85	°C
Storage Temp.	T_{STG}	-55 to +150	°C

Table 5 DC Ratings

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	VCC	5V ± 5%
Operating Temp. Commercial Industrial	T_A	 0 to +70°C -40°C to +85°C

Table 6 Operating Conditions

* NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	2.0	--	V_{CC}	V	
Input Low Voltage	V_{IL}	-0.3	--	+0.8	V	
Input Leakage Current CS0, CS1B, CTSB, DCDB, DSRB, PHI2, RESB, RS0, RS1, RWB, RxD	I_{IN}	--	±1	±2.5	µA	V_{IN} = 0V to V_{CC} V_{CC} = 5.25V
Leakage Current (Three State Off) D0-D7	I_{TSI}	--	±2	±10	µA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Output High Voltage D0-D7, DTRB, RTSB, RxC, TxD	V_{OH}	2.4	--	--	V	V_{CC} = 4.75V I_{LOAD} = -100 µA
Output Low Voltage D0-D7, DTRB , IRQB, RTSB, RxC, TxD,	V_{OL}	--	--	0.4	V	V_{CC} = 4.75V I_{LOAD} = 1.6 mA
Output High Current (Sourcing) D0-D7, DTRB, RTSB, RxC, TxD	I_{OH}	-200	-400	--	µA	V_{OH} = 2.4V
Output Low Current (Sinking) D0-D7, DTRB , IRQB, RTSB, RxC, TxD,	I_{OL}	1.6	--	--	mA	V_{OL} = 0.4V
Output Leakage Current (off state): IRQB	I_{OFF}	--		10	µA	V_{OUT} = 5.0V
Power Dissipation	P_D	--	7	10	mW/MHz	
Input Capacitance All except PHI2 PHI2	C_{CLK} C_{IN}	-- --		20 10	pF pF	V_{CC} = 5.0V V_{IN} = 0V f = 2 MHz T_A = 25° C
Output Capacitance	C_{OUT}	--		10	pF	

Notes:
1. All units are direct current (dc) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values are shown for V_{CC} = 5.0V and TA = 25° C

Table 7 DC Characteristics

PACKAGE DIMENSIONS

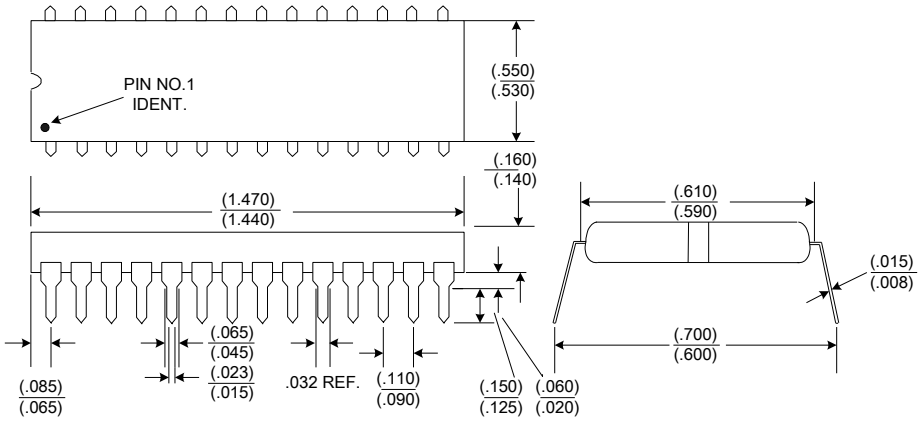


Figure 10 28Pin Plastic Dip Package Dimensions

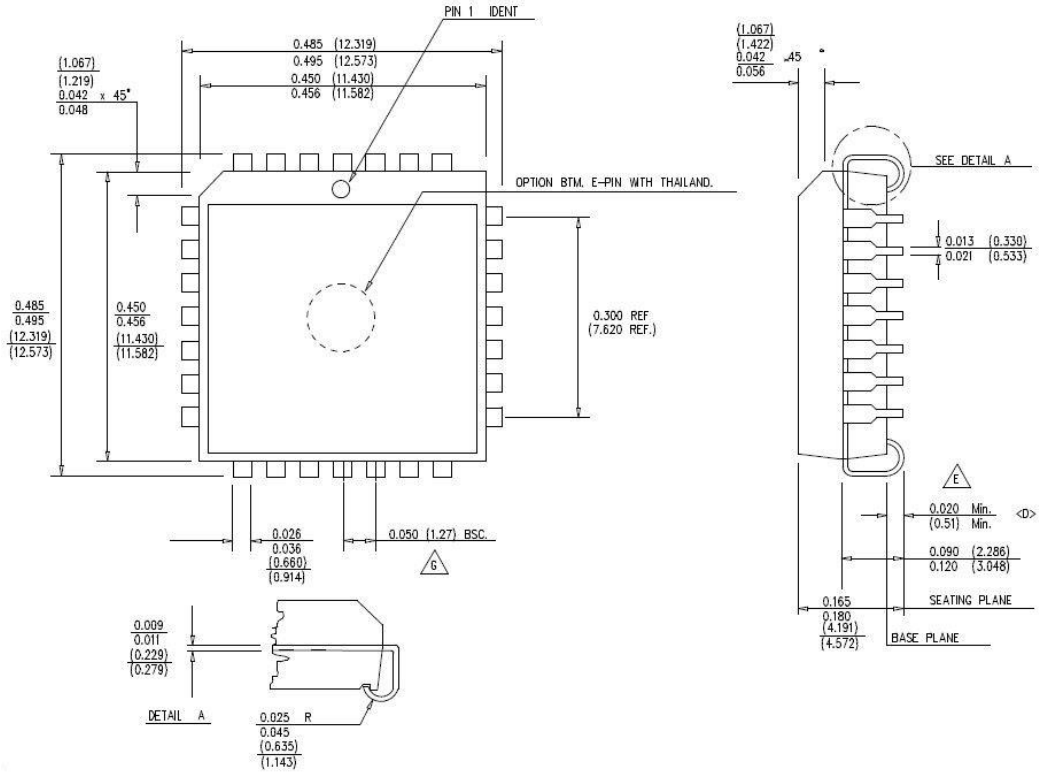


Figure 11 28 Pin PLCC Package Dimensions

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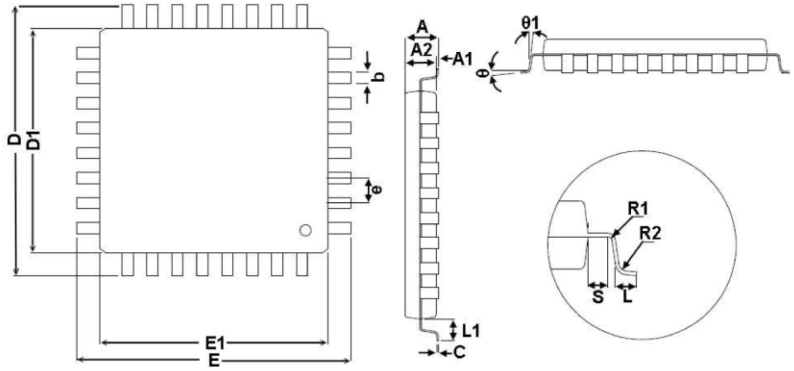

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
D	—	9.00 BSC	—
D1	—	7.00 BSC	—
E	—	9.00 BSC	—
E1	—	7.00 BSC	—
θ	0°	3.5°	7°
θ1	0°	—	—
S	0.20	—	—
R1	0.08	—	—
R2	0.08	—	0.20
L	0.45	0.60	0.75
L1	—	1.00 REF	—
b	0.30	—	0.45
e	—	0.80 BSC	—
c	0.09	—	0.20

Figure 12 32 Pin Low-Profile Quad Flat Pack (LQFP) Package Dimensions

ORDERING INFORMATION

Example: W65C51N6TPG-14	
Description W65C = standard product	W65C
Product Identification Number	51N
Foundry Process 6T = 0.6u TSMC Process	6T
Package P = Plastic Dual-In-Line, 28 pins PL = Plastic Lead Chip Carrier, 28 pins Q = Quad Flat Pack, 32 pins	P
RoHS/Green Compliance G = RoHS/Green Compliant (Wafer and Packaging)	G
Speed Designator -14 = 14MHz	-14

To receive general sales or technical support on standard product or information about our module library licenses, contact us at:

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2166 East Brown Road
Mesa, Arizona85213USA
Phone: 480-962-4545 Fax: 480-835-6442
e-mail: Info@WesternDesignCenter.com
www.WesternDesignCenter.com
www.WDC65xx.com

WARNING: MOS CIRCUITS ARE SUBJECT TO DAMAGE FROM STATIC ELECTRICAL CHARGE BUILDUPS. Industry established recommendations for handling MOS circuits include:

1. Ship and store product in conductive shipping tubes or conductive foam plastic. Never ship or store product in non-conductive plastic containers or non-conductive plastic foam material.
2. Handle MOS parts only at conductive workstations.
3. Ground all assembly and repair tools.