Zoxnoxious 3340 VCO

FEATURES

- Alfa Rpar AS3340 VCO
- Microcontroller interface via I^2C and SPI
- DAC control for all VCO parameters
- Switching controls for signal routing
- External signal inputs allow for modulation, controlled via VCA
- Two VCO outputs with VCA control for pulse, sawtooth, triangle waveforms
- Four modes of sync with phase modulation
- Board identifier via ROM
- Eurorack power levels

APPLICATIONS

- Electronic music
- Hardcore techno
- Ambient electronica
- Beyond obnoxious noise
- Folding laundry or space

GENERAL DESCRIPTION

Built around an Alfa Rpar AS3340 VCO, the Zonxoxious 3340 provides a digital interface over Serial Peripheral Interface (SPI) and Inter-Integrated Circuit (I^2C) for all control elements. A 2x20 header includes power, digital control, analog inputs, and analog outputs. The 2x20 header is common among Zoxnoxious devices.

VCO control signals are genereated via an Analog Devices AD5328 12-bit DAC. Control signals include exponential frequency control (1 V/octave), linear frequency control, pulse width, VCA levels for both external input modulation and triangle output, and sync phase are controlled by the DAC. Switched control elements interface with a On Semicon PCA9555 GPIO. Switched controls include external signal selection, routing the external signal to posiive sync, negative sync, exponential frequency modulation, linear frequency modultion, output signals and levels.

A M24C02 ROM allows query and identification of the Zoxnoxious 3340 over I^2C.

A dedicated output pin for the pulse is provided. The is intended to be read back to a microcontroller to allow for tuning.

Functions controlled via 12-bit DAC over SPI:

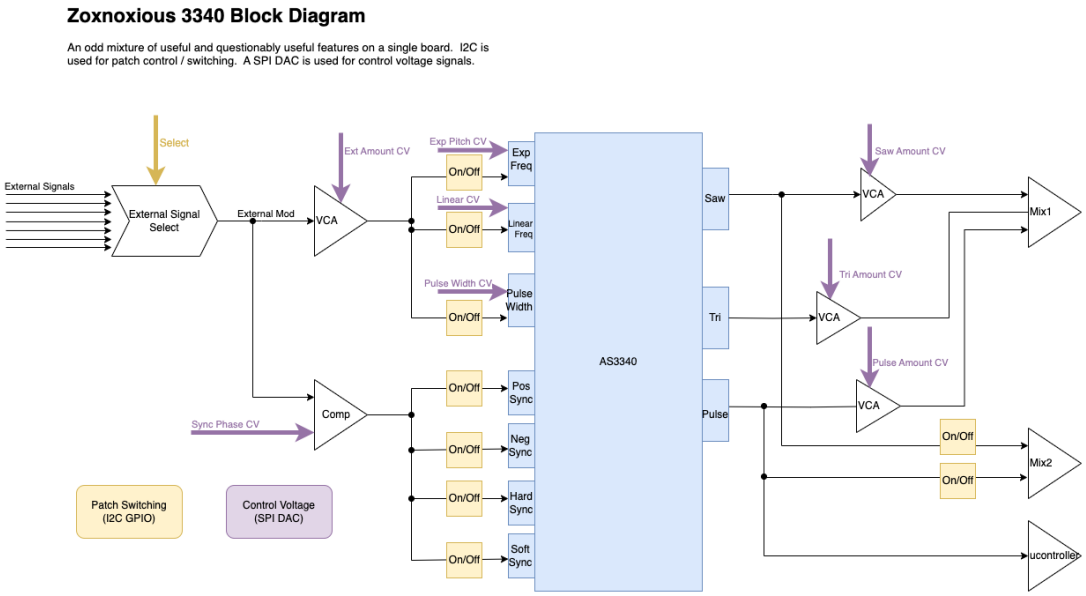
- Exponential frequency @ 1V/oct
- Linear control voltage
- Pulse Width
- Sync phase
- External modulation attenuation
- Mix1 Triangle output level
- Mix1 Sawtooth output level
- Mix1 Pulse output level

Functions controlled via GPIO over I^2C:

- External signal select from 13 inputs
- External signal to exponential frequency
- External signal to linear frequency
- External signal to pulse width
- Traditional hard sync
- Soft sync
- Positive hard sync
- Negative hard sync
- Mix2 Pulse output on/off
- Mix2 Saw output on/off

FUNCTIONAL DIAGRAM

The significant blocks of the Z3340 is shown below highlighting functions controlled for SPI and I^2C.

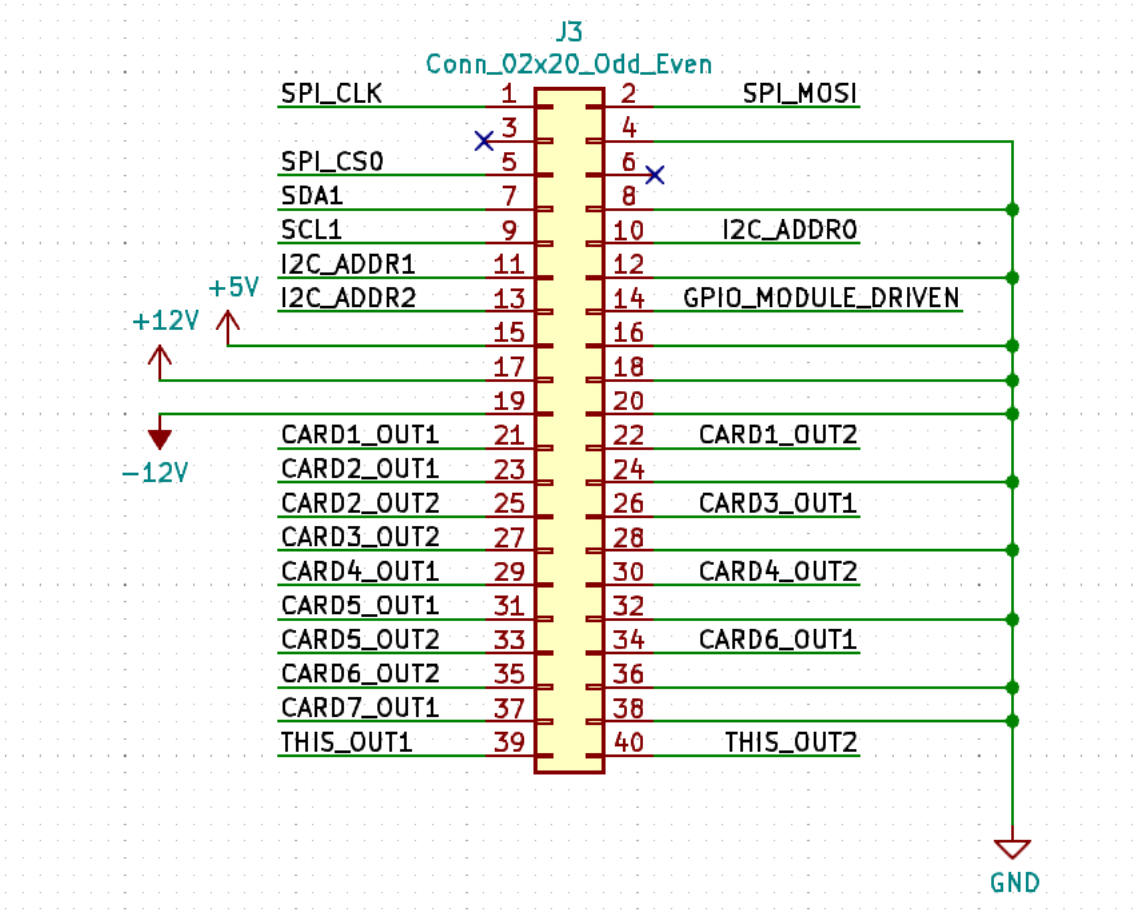


SPECIFICATIONS

V_{CC} +12V, V_{DD} +5V, V_{EE} -12V		
Parameter	Typical	Units
Power		
V_{CC}	34	mA
V_{DD}	5	mA
V_{EE}	35	mA
Digital Input[1]		
Logic levels	5V logic	
I^2C frequency	400	kHz
SPI frequency	12	MHz
Digital Output		
GPIO Module Output Upper Level	5.0	V
GPIO Module Output Lower Level	0.0	V
Analog Input		
External Signal Recommended High Voltage	5.0	V
External Signal Recommended Low Voltage	-5.0	V
External Signal Input Impedance (selected)	100k	Ω
External Signal Input Impedance (unselected)	High	Ω
Analog Output[2]		
Frequency	27.5 – 7040	Hz
Mix1 Pulse	-2.7 – +2.7	V
Mix1 Saw	-1.8 – +1.8	V
Mix1 Triangle	-2.0 – +2.0	V
Mix2 Pulse	0.0 – +3.6	V
Mix2 Saw	0.0 – +3.7	V
Mix1 Output Impedance	51	Ω
Mix2 Output Impedance	51	Ω

[1] I^2C: refer to PCA9555 and M24C02 specs for detailed info. SPI: refer to AD5328 spec for detailed info.
[2] Mix1 is AC coupled; Mix2 is unipolar.

PIN CONFIGURATION AND DESCRIPTION



Pin	Mnemonic	Description
1	SPI_CLK	Serial (SPI) clock for AD5328
2	SPI_MOSI	Serial (SPI) serial in for AD5328
3	SPI_MISO	Not used / no connect for Zoxnoxious 3340
4	GND	Ground
5	SPI_CS0	Active low chip select for AD5328
6	SPI_CS1	Not used / no connect for Zoxnoxious 3340
7	SDA1	I^2C data for PCA9555 and M24C02
8	GND	Ground
9	SCL1	I^2C clock for PCA9555 and M24C02
10	I2C_ADDR0	I^2C address bit for PCA9555 and M24C02
11	I2C_ADDR1	I^2C address bit for PCA9555 and M24C02
12	GND	Ground
13	I2C_ADDR2	I^2C address bit for PCA9555 and M24C02

14	GPIO_MODULE_DRIVEN	AS3340 Pulse wave
15	V_{DD}	+5V power
16	GND	Ground
17	V_{CC}	+12V power
18	GND	Ground
19	V_{EE}	-12V power
20	GND	Ground
21	CARD1_OUT1	Input signal selectable as a modulation source
22	CARD1_OUT2	Input signal selectable as a modulation source
23	CARD2_OUT1	Input signal selectable as a modulation source
24	GND	Ground
25	CARD2_OUT2	Input signal selectable as a modulation source
26	CARD3_OUT1	Input signal selectable as a modulation source
27	CARD3_OUT2	Input signal selectable as a modulation source
28	GND	Ground
29	CARD4_OUT1	Input signal selectable as a modulation source
30	CARD4_OUT2	Input signal selectable as a modulation source
31	CARD5_OUT1	Input signal selectable as a modulation source
32	GND	Ground
33	CARD5_OUT2	Input signal selectable as a modulation source
34	CARD6_OUT1	Input signal selectable as a modulation source
35	CARD6_OUT2	Input signal selectable as a modulation source
36	GND	Ground
37	CARD7_OUT1	Input signal selectable as a modulation source
38	GND	Ground
39	THIS_OUT1	Output signal Mix1
40	THIS_OUT2	Output signal Mix2

THEORY OF OPERATION

I²C Addresses and SPI Chip Enable

Both I²C chips, the M24C02 and PCA9555, take the last 3 bits their I²C address from the J3 2x20 connection header. Provided cards are given unique addresses, this allows up to 8 instances of the same Zoxnoxious 3340 VCO card or other Zoxnoxious compatible cards to be used together. The I²C addresses for the M24C02 and PCA9555 are shown below based on J3 pins 13, 11, 10.

Pins 13, 11, 10	M24C02 Addr	PCA9555 Addr
000	0x50	0x20
001	0x51	0x21
010	0x52	0x22
011	0x53	0x23
100	0x54	0x24
101	0x55	0x25
110	0x56	0x26
111	0x57	0x27

Changing the state of J3 pins 13, 11, or 10 during operation is undefined behavior.

ROM Query

The Zoxnoxious 3340 VCO can be distinctly identified from other Zoxnosious boards by querying an 8-bit value at byte address zero on the M24C02 ROM. A factory value of "0x02" is set at byte address zero by the Zoxnoxious elves. For normal operation the read of byte address zero is the only action ever required from the ROM. Refer to the M24C02 datasheet for I²C protocol.

Writes are disabled without a jumper. Jumpering J2 enables writes.

GPIO Setup and Operation

On startup, two I²C writes should be issued to configure outputs on both the PCA9555 ports.

Set Port 0 as output	`<i2c addr> 0x06 0x00`
Set Port 1 as output	`<i2c addr> 0x07 0x00`

Patch setup is then a matter of an I²C command for the desired switching shown below.

Switch	Port	Bit(s)
Traditional Hard Sync	Port 0	`XXXXXXX1`
Ext Mod to PW	Port 0	`XXXXXX1X`
LED (active low)	Port 0	`XXXX0XXX`
Sync Negative	Port 0	`XXX1XXXX`
Soft Sync	Port 0	`X1XXXXXX`
Sync Positive	Port 0	`1XXXXXXX`
Ext Mod to Linear Freq	Port 1	`XXXXXXX1`
Mix2 Saw	Port 1	`XXXXXX1X`
Mix2 Pulse	Port 1	`XXXXX1XX`
Ext Mod to Exp Freq	Port 1	`XXXX1XXX`
Card A Out1	Port 1	`0000XXXX`
Card A Out2	Port 1	`0001XXXX`
Card B Out1	Port 1	`0010XXXX`
Card B Out2	Port 1	`0011XXXX`
Card C Out1	Port 1	`0100XXXX`
Card C Out2	Port 1	`0101XXXX`
Card D Out1	Port 1	`0110XXXX`
Card D Out2	Port 1	`0111XXXX`
Card E Out1	Port 1	`1000XXXX`
Card E Out2	Port 1	`1001XXXX`
Card F Out1	Port 1	`1010XXXX`
Card F Out2	Port 1	`1011XXXX`
Card G Out1	Port 1	`1100XXXX`

Value "`X`" implies don't care; in this instance the meaning should be "maintain state" with the previous value. Details on PCA9555 commands are available in the PCA9555 datasheet.

DAC Setup and Operation

The AD5328 enable is active low through SPI_CS0 chip select. SPI mode 1 is used for data transfer. On power up, two SPI writes should be issued to initialize the DAC. The first write is for a full reset of device, sending `0xF0 0x00` via SPI. A second SPI command to power on all

DACs with 1x gain and use Vref is sent with a payload of `0x80 0x00`.

Setting DAC lines on the AD5328 via SPI is two bytes of data with the upper four bits being the address of the DAC line and the lower 12 bits being the data bits to convert to analog.

Supporting DAC circuitry is designed around a 4 kHz sampling rate. A simple RC filter is used for low pass filtering DAC outputs with the approximate corner frequencies listed below.

Description	DAC Addr	Cutoff (Hz)
Sync level	0x0	1600
Exp Freq control	0x1	1600
Mix1 Pulse VCA	0x2	400
External Mod VCA	0x3	400
Mix1 Triangle VCA	0x4	400
Mix1 Saw VCA	0x5	400
Pulse Width	0x6	700
Linear Freq control	0x7	1300

GPIO Module Output

The AS3340's pulse wave drives a switch with a high level of V_{DD}. The intent with this output is to allow a microcontroller to read the pulse wave for frequency counting or tuning. This may be best done in an offline tuning routine so that the pulse width can be set to a fixed 50% values.

EXTERNAL MODULATION

The Zoxnoxious bus provides thirteen signals from seven cards. The Zoxnoxious 3340 gives access to any of these signals; one may be selected as a modulation source via an I^2C transaction to the GPIO. The modulation destinations can also be enabled/disabled via I^2C transactions to the GPIO.

TEST POINTS

The following test points are available on the Zoxnoxious 3340 board:

Test Point	Description
TP1	High Freq Tracking
TP2	Soft Sync Input
TP3	VCO Saw Out
TP4	Hard Sync Input
TP5	Sync Comparator
TP6	VCI Tri Out
TP7	External Mod Post-VCA

TUNING

As a reference, the CEM3340 datasheet provides info on tuning. The AS3340 does not provide tuning info. For the Zoxnoxious 3340, the steps are:

1. Adjust RV2 such that High Freq Tracking reads 0 Volts
2. Set exponential frequency control DAC to (VALUE: 2VOLTS)
3. Note frequency
4. Set exponential frequency control DAC to (VALUE: 3VOLTS)
5. Note frequency
6. Adjust RV1 towards 1 Volt per octave
7. Repeat DAC setting, adjusting RV1 to 1 Volt per octave
8. Increase frequency to UPPER FREQ
9. Note frequency
10. Set exponential frequency control DAC to (EVEN HIGHER)
11. Repeat DAC setting and adjust RV2 to achieve 1 Volt per octave

BOARD INFORMATION

Todo: dimensions, pic, layout