Zoxnoxious 3372 Analog Signal Processor

FEATURES

- Alfa Rpar AS3372 Analog Signal Processor
- 4-pole lowpass filter with resonance
- White noise source available pre-filter
- Two selectable sources for mixing and modulation
- Panning control over output
- Microcontroller interface via I²C and SPI
- DAC control over eight parameters
- Switching controls for signal routing
- Board identifier via ROM
- Eurorack power levels

APPLICATIONS

- Electronic music
- Detroit techno
- Ambient electronica
- Beyond obnoxious noise

GENERAL DESCRIPTION

Built around the Alfa Rpar AS3372 Analog Signal Processor, the Zonxoxious Z3372 provides a digital interface over Serial Peripheral Interface (SPI) and InterIntegrated Circuit (I 2 C) for all control elements. A 2x20 header includes power, digital control, analog inputs, and analog outputs. The 2x20 header is common among Zoxnoxious devices and plugs into the Zoxnoxious Signal Bus.

The Z3372 control signals are generated via an Analog Devices AD5328 12-bit DAC. Control signals include filter cutoff frequency, resonance amount, VCA control for two inputs, VCA control for modulation amount,

noise level, output level, and pan control. Switched control elements interface with a On Semicon PCA9555 GPIO. Switched controls include selection of two different input signal from the Zoxnoxious Signal Bus, and enable/disabling modulation routing to filter cutoff, resonance, output level, and panning.

A M24C02 ROM allows query and identification of the Zoxnoxious Z3372 over ${\rm I}^2{\rm C}$.

A digital output is provided to allow for calibration.

Functions controlled via 12-bit DAC over SPI:

- Signal one input VCA
- Signal two input VCA
- White noise level
- Filter cutoff
- Resonance amount
- Modulation amount
- Output VCA
- Panning mix1/mix2

Functions controlled via GPIO over I²C:

- Input Signal one select from 8 inputs
- Input Signal two select from 8 inputs
- Filter cutoff modulation
- Resonance modulation
- Output VCA modulation
- Panning modulation

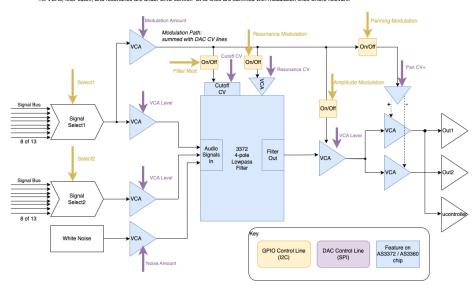
FUNCTIONAL DIAGRAM

The significant blocks of the Z3372 is shown below highlighting functions controlled for SPI and I²C.

Zoxnoxious Z3372 Block Diagram

The Zoxnoxious 3372 is a voltage controlled 4-pole lowpass filter with voltage controlled resonance, amplifier control, and stereo panning to provide analog signal processing for audio signals. Two muxes on the frontend allow for signal selection to mix two signals from the Zoxnoxious audio bus. The first signal is available both on the audio path and can also be used as a modulation source. Modulation destinations include filter cutoff, resonance, amplitude modulation, and panning modulation. A white noise source with its own VCA is included as an additional audio source, pre-filter.

All VCAs, filter cutoff, and resonance are under DAC control. DAC lines are summed with modulation lines where relevant.

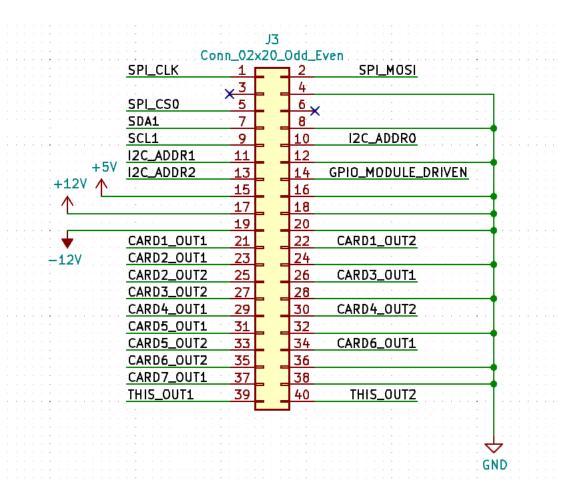


SPECIFICATIONS

$\rm V_{CC}$ +12V, $\rm V_{DD}$ +5V, $\rm V_{EE}$ -12V			
Parameter	Typical	Units	
Power			
$ m V_{CC}$	TBD	mA	
$ m V_{DD}$	TBD	mA	
$ m V_{EE}$	TBD	mA	
Digital Input ¹			
Logic levels	5V logic		
I ² C frequency	400	kHz	
SPI frequency	12	MHz	
Digital Output			
GPIO Module Output Upper Level	5.0	V	
GPIO Module Output Lower Level	0.0	V	
Analog Input			
External Signal Recommended High Voltage	5.0	V	
External Signal Recommended Low Voltage	-5.0	V	
External Signal Input Impedance (selected)	100k	Ω	
External Signal Input Impedance (unselected)	High	Ω	
Analog Output			
Frequency control range	10	Octaves	
Frequency at min control	< 13.75	$_{\mathrm{Hz}}$	
Frequency at max control	> 14080	$_{\mathrm{Hz}}$	
Resonance control for oscillation	OxOCFF	DAC Value	
Mix1 Output Impedance	51	Ω	
Mix2 Output Impedance	51	Ω	

 $^{^{1}\}mathrm{I}^{2}\mathrm{C}$: refer to PCA9555 and M24C02 data sheets for detailed info. SPI: refer to AD5328 data sheet for detailed info.

PIN CONFIGURATION AND DESCRIPTION



Pin	Mnemonic	Description
1	SPI_CLK	Serial (SPI) clock for AD5328
2	SPI_MOSI	Serial (SPI) serial in for AD5328
3	SPLMISO	Not used / no connect
4	GND	Ground
5	SPLCS0	Active low chip select for AD5328
6	SPLCS1	Not used / no connect
7	SDA1	$\mathrm{I}^{2}\mathrm{C}$ data for PCA9555 and M24C02
8	GND	Ground
9	SCL1	${ m I^2C}$ clock for PCA9555 and M24C02
10	I2C_ADDR0	${ m I^2C}$ address bit for PCA9555 and M24C02
11	I2C_ADDR1	I ² C address bit for PCA9555 and M24C02
12	GND	Ground
13	I2C_ADDR2	${ m I^2C}$ address bit for PCA9555 and M24C02

14	GPIO_MODULE_DRIVEN	logic switched from Out1
15	$ m V_{DD}$	+5V power
16	GND	Ground
17	$ m V_{CC}$	+12V power
18	GND	Ground
19	$ m V_{EE}$	-12V power
20	GND	Ground
21	CARD1_OUT1	Input selectable as Source1 or Source2
22	CARD1_OUT2	Input selectable as Source1 or Source2
23	CARD2_OUT1	Input selectable as Source2
24	GND	Ground
25	CARD2_OUT2	Input selectable as Source1 or Source2
26	CARD3_OUT1	Input selectable as Source1
27	CARD3_OUT2	Input selectable as Source2
28	GND	Ground
29	CARD4_OUT1	Input selectable as Source2
30	CARD4_OUT2	Input selectable as Source1
31	CARD5_OUT1	Input selectable as Source1
32	GND	Ground
33	CARD5_OUT2	Input selectable as Source2
34	CARD6_OUT1	Input selectable as Source2
35	CARD6_OUT2	Input selectable as Source1
36	GND	Ground
37	CARD7_OUT1	Input selectable as Source1
38	GND	Ground
39	THIS_OUT1	Output signal Left
40	THIS_OUT2	Output signal Right

THEORY OF OPERATION

I²C Addresses and SPI Chip Enable

Both I²C chips, the M24C02 and PCA9555, take the last 3 bits their I²C address from the J3 2x20 connection header. Provided cards are given unique addresses, this allows up to multiple instances of the same Zoxnoxious Z3372 card or other Zoxnoxious compatible cards to be used together. The I²C addresses for the M24C02 and PCA9555 are shown below based on J3 pins 13, 11, 10.

Pins 13, 11, 10	M24C02 Addr	PCA9555 Addr
000	0x50	0x20
001	0x51	0x21
010	0x52	0x22
011	0x53	0x23
100	0x54	0x24
101	0x55	0x25
110	0x56	0x26
111	0x57	0x27

Changing the state of J3 pins 13, 11, or 10 during operation is undefined behavior.

ROM Query

The Zoxnoxious Z3372 Analog Signal Processor can be distinctly identified from other Zoxnosious boards by querying an 8-bit value at byte address zero on the M24C02 ROM. A factory value of "0x03" is set at byte address zero by the Zoxnoxious elves. For normal operation the read of byte address zero is the only action ever required from the ROM. Refer to the M24C02 datasheet for $\rm I^2C$ protocol.

Writes are enabled via a jumper. Typical operation is expected to be read-only.

GPIO Setup and Operation

On startup, two I^2C writes should be issued to configure outputs on both the PCA9555 ports.

Set Port 0 as output <i2c addr> 0x06 0x00 Set Port 1 as output <i2c addr> 0x07 0x00

Patch setup is then a matter of an I²C command for the desired switching shown below.

Switch	Port	Bit(s)
LED (active low)	Port 0	XXXXXXXO
Signal1 to VCF mod	Port 0	XXXXX1XX
Signal1 to Resonance mod	Port 0	XXXX1XXX
Signal1 to VCA mod	Port 0	XXX1XXXX
Signal1 to Panning mod	Port 0	XX1XXXXX
Signal1 Enable	Port 1	XXXXXXX1
Card 1 Out1	Port 1	XXXX1111
Card 1 Out2	Port 1	XXXX1101
Card 2 Out2	Port 1	XXXX1011
Card 3 Out1	Port 1	XXXX1001
Card 4 Out2	Port 1	XXXX0111
Card 5 Out1	Port 1	XXXX0101
Card 6 Out2	Port 1	XXXX0011
Card 7 Out1	Port 1	XXXX0001
Signal2 Enable	Port 1	XXX1XXXX
Card 1 Out1	Port 1	1111XXXX
Card 1 Out2	Port 1	1101XXXX
Card 2 Out1	Port 1	1011XXXX
Card 2 Out2	Port 1	1001XXXX
Card 3 Out2	Port 1	0111XXXX
Card 4 Out1	Port 1	0101XXXX
Card 5 Out2	Port 1	0011XXXX
Card 6 Out1	Port 1	0001XXXX

Value "X" implies don't care; in this instance the meaning should be "maintain state" with the previous value. Details on PCA9555 commands are available in the PCA9555 datasheet.

DAC Setup and Operation

The AD5328 enable is active low through SPI_CS0 chip select. SPI mode 1 is used for data transfer. On power

up, two SPI writes should be issued to initialize the DAC. The first write is for a full reset of device, sending 0xF0 0x00 via SPI. A second SPI command to power on all DACs with 2X gain and use Vref is sent with a payload of 0x80 0x30.

Setting DAC lines on the AD5328 via SPI is two bytes of data with the upper four bits being the address of the DAC line and the lower 12 bits being the data bits to convert to analog.

Supporting DAC circuitry is designed assuming a 4 kHz sampling rate. A simple RC filter is used for low pass filtering DAC outputs with the approximate corner frequencies listed below.

Description	DAC Addr	Cutoff (Hz)
Noise VCA	0x0	285
Pan VCA	0x1	340
Resonance	0x2	400
Output VCA	0x3	360
VCF Cutoff	0x4	800
Signal1 VCA	0x5	1000
Signal2 VCA	0x6	1000
Modulation VCA	0x7	285

GPIO Module Output

The This_Out1 output is used to drive a transistor for digital output to GPIO_Module_Driven. The digital output will toggle with the input signal.

Frequency counting can be used as part of a tune routine for the VCF. With resonance set high and inputs signals muted (VCAs to zero), the cutoff frequency can be set to characterize the frequency response.

EXTERNAL INPUT

The Z3372 card allows two inputs to be tapped from the thirteen signals the Zoxnoxious signal bus provides. The Signal1 input can be used for filtering and/or modulation. The Signal2 input can be used for filtering only. Two 8:1 muxes front each input, so a limited number of the Zoxnoxious signal bus is available to each input. See the GPIO section of how to set each input. The modulations available are described below.

VCF mod Signal1 is added to the VCF cutoff. This modulates the filter cutoff point at an audio rate from Signal1.

Resonance mod Signal1 is inverted and added to the resonance amount. This will be out of phase from VCF mod, as that produces the most interesting results.

VCA mod Signal1 is added to VCA4 for amplitude modulation. Given the function is addition, this may work best with the output VCA tuned down a bit.

Panning mod Signal1 is added to Panning signal. This has a similar effect to amplitude modulation, but for each left/right channel and in opposite phases.

The Modulation VCA controls the modulation amount for all destinations. All modulations are DC-coupled.

TEST POINTS

The following test points are available on the Zoxnoxious Z3372 board:

Test Point	Description
TP1	Resonance CV
TP2	White Noise
TP3	VCA 1/2 Out
TP4	Pan CV
TP5	VCF Out Post-Cap
TP6	VCF CV
TP7	VCA4 Out
TP8	Modulation VCA Out
TP9	VCA4 CV
TP10	GPIO Out Transistor Base
TP11	Input to Resonance VCA

BOARD INFORMATION

Todo: dimensions, pic, layout