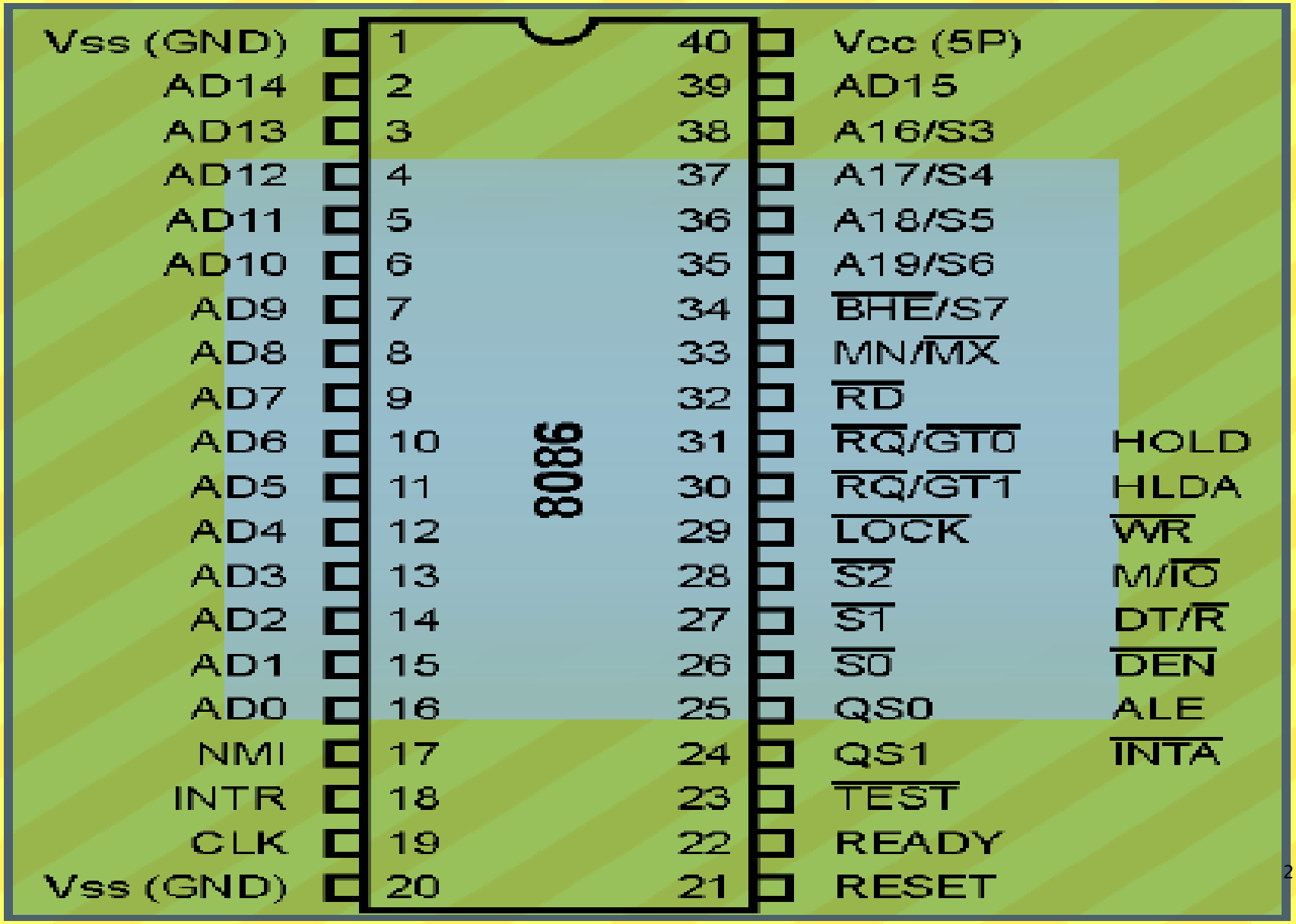
Chapter 3

Hardware Features of 8086/8088 and Memory Interfacing

- **Pin details**
- **Interfacing and address decoding**

Features of 8086/8088 -Pin details



AD0 – AD15
Pin 16-2, 39 (Bi-directional)

- These lines are multiplexed bidirectional address/data bus.
- During T1, they carry lower order 16-bit address.
- In the remaining clock cycles, they carry 16-bit data.
- AD0-AD7 carry lower order byte of data.
- AD8-AD15 carry higher order byte of data.

A19/S6, A18/S5, A17/S4, A16/S3
Pin 35-38 (Unidirectional)

- These lines are multiplexed unidirectional address and status bus.
- During T1, they carry higher order 4-bit address.
- In the remaining clock cycles, they carry status signals.

BHE / S7
Pin 34 (Output)

- BHE stands for Bus High Enable.
- BHE signal is used to indicate the transfer of data over higher order data bus (D8 – D15).
- 8-bit I/O devices use this signal.
- It is multiplexed with status pin S7.

RD (Read)
Pin 32 (Output)

- It is a read signal used for read operation.
- It is an output signal.
- It is an active low signal.

READY Pin 22 (Input)

- This is an acknowledgement signal from slower I/O devices or memory.
- It is an active high signal.
- When high, it indicates that the device is ready to transfer data.
  - When low, then microprocessor is in wait state.

RESET
Pin 21 (Input)

- It is a system reset.
- It is an active high signal.
- When high, microprocessor enters into

reset state and terminates the current activity.

- It must be active for at least four clock cycles to reset the microprocessor.
- **INTR Pin 18 (Input)**
- It is an interrupt request signal.
- It is active high.
- It is level triggered.

NMI
Pin 17 (Input)

- It is a non-maskable interrupt signal.
- It is an active high.
- It is an edge triggered interrupt.

- **TEST Pin 23 (Input)**
- It is used to test the status of coprocessor 8087.
- The BUSY pin of 8087 is connected to the pin of 8086.
- If low, execution continues else microprocessor is in wait state.

CLK
Pin 19 (Input)

- This clock input provides the basic timing for processor operation.
- It is symmetric square wave.
- The range of frequency of different versions is 5 MHz, 8 MHz and 10 MHz.

- **VCC and VSS**

Pin 40 and Pin 20 (Input)

- VCC is power supply signal.
- +5V DC is supplied through this pin.
- VSS is ground signal.

MN / MX
Pin 33 (Input)

- 8086 works in two modes:
- Minimum Mode
- Maximum Mode
- If MN/MX is high, it works in minimum mode.
- If MN/MX is low, it works in maximum mode.
- Pins 24 to 31 issue two different sets of signals.
- One set of signals is issued when CPU operates in minimum mode.
- Other set of signals is issued when CPU operates in maximum mode.

Pin Description for Minimum Mode

- **INTA Pin 24 (Output)**
- This is an interrupt acknowledge signal.
- When microprocessor receives INTR signal, it acknowledges the interrupt by generating this signal.
- It is an active low signal.
- **ALE Pin 25 (Output)**
- This is an Address Latch Enable signal.
- It indicates that valid address is available on bus AD0 – AD15.
- It is an active high signal and remains high during T1 state.
- It is connected to enable pin of latch 8282.

DEN
Pin 26 (Output)

- This is a Data Enable signal.
- This signal is used to enable the transceiver 8286.
- Transceiver is used to separate the data from the address/data bus.
- It is an active low signal.

• DT / R Pin 27 (Output)

- This is a Data Transmit/Receive signal.
- It decides the direction of data flow through the transceiver.
- When it is high, data is transmitted out.
- When it is low, data is received in.

M / IO
Pin 28 (Output)

- This signal is issued by the microprocessor to distinguish memory access from I/O access.
- When it is high, memory is accessed.
- When it is low, I/O devices are accessed.

• WR Pin 29 (Output)

- It is a Write signal.
- It is used to write data in memory or output device depending on the status of M/IO signal.
- It is an active low signal.

HLDA
Pin 30 (Output)

- It is a Hold Acknowledge signal.
- It is issued after receiving the HOLD signal.
- It is an active high signal.

- **HOLD Pin 31 (Input)**
- When DMA controller needs to use address/data bus, it sends a request to the CPU through this pin.
- It is an active high signal.
- When microprocessor receives HOLD signal, it issues HLDA signal to the DMA controller.

Pin Description for Maximum Mode

- **QS1 and QS0 Pin 24 and 25 (Output)**
- These pins provide the status of instruction queue.

QS_1	QS_0	Status
0	0	No operation
0	1	1st byte of opcode from queue
1	0	Empty queue
1	1	Subsequent byte from queue

S0, S1, S2
Pin 26, 27, 28 (Output)

- These status signals indicate the operation

being done by the microprocessor.

- This information is required by the Bus Controller 8288.
- Bus controller 8288 generates all memory and I/O control signals.

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Status
0	0	0	Interrupt Acknowledge
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	Halt
1	0	0	Opcode Fetch
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	Passive

LOCK, Pin 29 (Output)

- This signal indicates that other processors should not ask CPU to relinquish the system bus.
- When it goes low, all interrupts are masked and

HOLD request is not granted.

- This pin is activated by using LOCK prefix on any instruction

- **RQ/GT1, RQ/GT0 Pin 30 and 31 (Bi-dxn)**
- These are Request/Grant pins.
- Other processors request the CPU through these lines to release the system bus.
- RQ/GT0 has higher priority than RQ/GT1

Clock Generator

- 8284A Clock Generator provides the proper clock signal of the microprocessor.
- An 18-pin chip.
- Not only provide the clock and synchronization that provides the READY signal for the insertion of WAIT states into the CPU bus cycle.

- Clock generator uses clock signal for the 8086 through execution of its instructions in an orderly manner.
- The 8284A also synchronizes the RESET signal with the clock so that this signal is applied to the 8086 at the proper times.
- **The clock speed supported by the 80X86 family are:**
- Standard 8086 operate at 5 MHz clock speed, whereas 8086-2 and 8086-1 processors operate at 8-MHz and 10 MHz clock speed, respectively.
- Standard 8088 operate at 5 MHz, whereas 8088-2 processor operates at 8 MHz clock speed.

- The CLK signal is externally generated by 8284A clock generator and feed into the processor using Pin number 19.

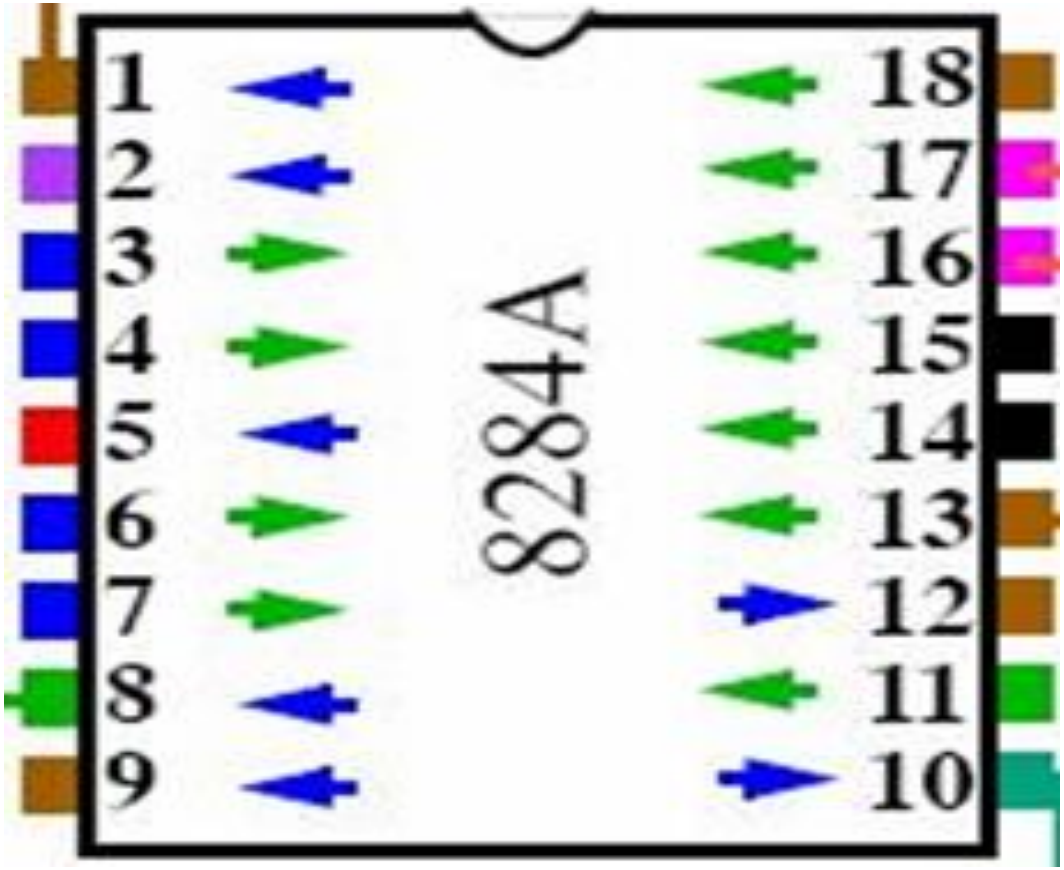


Fig. of 8284A clock generator

- The first instruction of the system start-up program is usually located at this address, so asserting this signal is a way to boot or start the system.

Bus buffering

- Buffering (boosting) of the control, data, and address busses to provide sufficiently strong signals to drive various IC chips.
- bus buffering = boosting the signals travelling on the busses.
- – unidirectional bus **74LS244.**
- – bidirectional bus **74LS245.**

- Buffers used on the data bus must be bidirectional because the 8086 sends data out on the data bus and also reads data in on the data bus.
- The DT/R from the 8086 sets the direction in which data will pass through the buffers.
- When DT/R becomes high, the buffers will be set up to transmit data from the 8086 to ROM, RAM or Ports.
- When DT/R becomes low, the buffers will be setup to allow data to come into the 8086 from ROM, RAM or Ports.

•Bus Cycle and Time States

- A bus cycle (machine cycle) defines the basic operation that a microprocessor performs to communicate with external devices.
- **Such as,** memory read bus-cycle, where data stored in main memory is read into the internal registers of the CPU (such as AX).
- There are **four** basic types of bus cycles:
- Read, Write, Interrupt acknowledge and Halt.
- The bus-cycle of the 8086 and 8088 processors consist of **four** clock cycles or pulses. Thus, duration of a bus-cycle is = '**4*T'.**

- Interrupt acknowledge and halt bus cycles define special bus operations.
- Read bus cycles include memory, I/O and instruction prefetch bus operations.
- Write bus cycles include memory and I/O bus operations.
- During these operations, a series of control signals are also produced by the MPU to control the direction and timing of the bus.

- Each bus cycle consists of at least **four** clock periods: T1, T2, T3, and T4.These clock periods are also called the **T-States**.
- **T- States**
- Why are there T states?
  - In the 8086/8088, the address and data lines are multiplexed.
  - The MP needs time to change the signals during each bus cycle.
  - Memory devices need time to decipher the address value and then read/write the data (**access time**).
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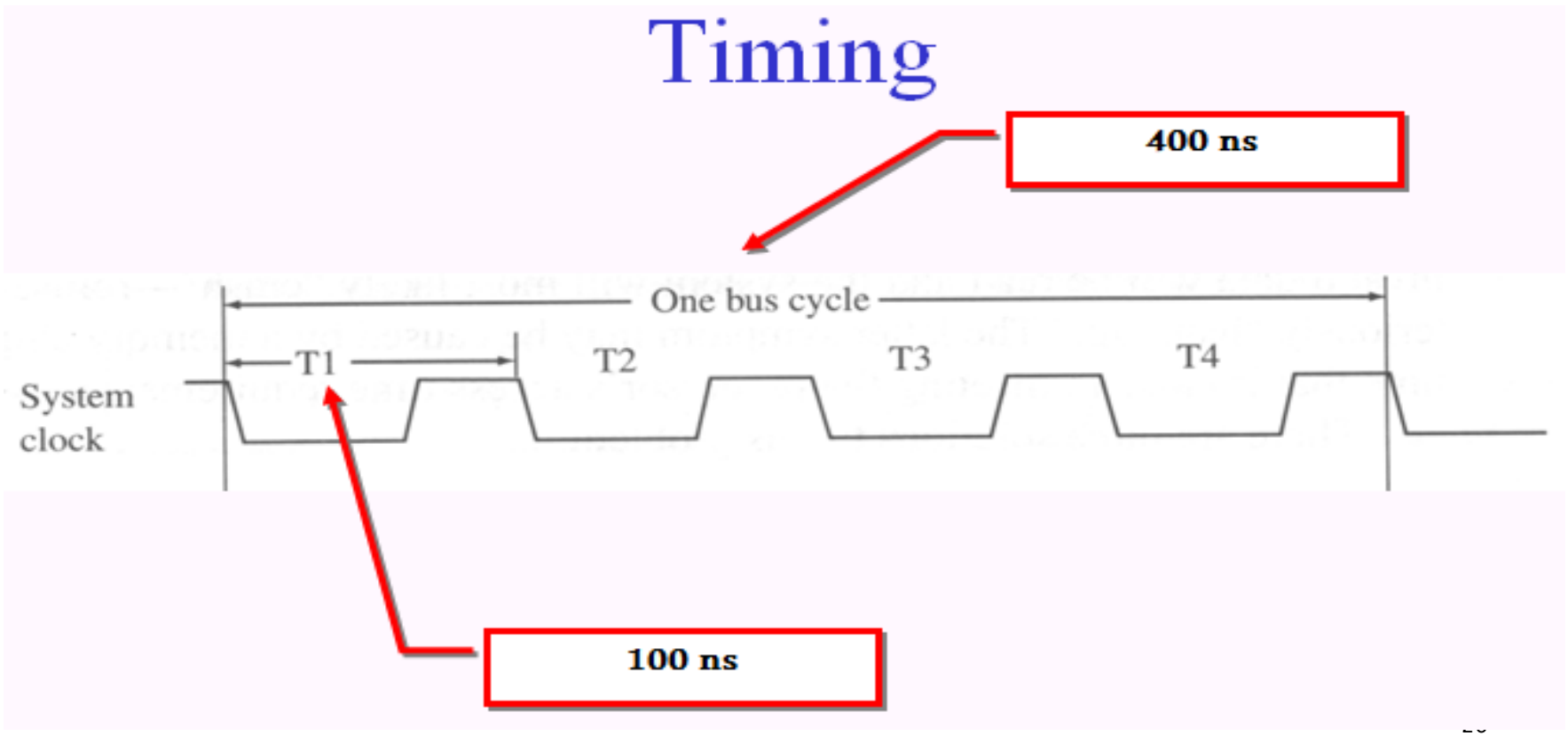
○Timing

- 10-MHz 8086 CPU.
- Each clock cycle has a period of 100ns.
- Machine cycle period is 400ns.



- **T1** - Start of bus cycle. Actions include setting control signals (or S0-S2status lines) to give the required values for ALE, DT/R and IO/M putting a valid address onto the address bus.
- **T2** - The RD or WR control signals are issued, DEN is asserted and in the case of a write, data is put onto the data bus. The DEN turns on the data bus buffers to connect the CPU to the external data bus. The READY input to the CPU is sampled at the end of T2 and if READY is low, a wait state TW before T3 begin.
- **T3** - This clock period is provided to allow memory to access the data. If the bus cycle is a read cycle, the data bus is sampled at the end of T3.

- **T4** - all bus signals are deactivated in preparation for the next clock cycle.
- For the write cycle, the WR signal transfers data to the memory or I/O, which activates and write when WR returns to logic 1 level.

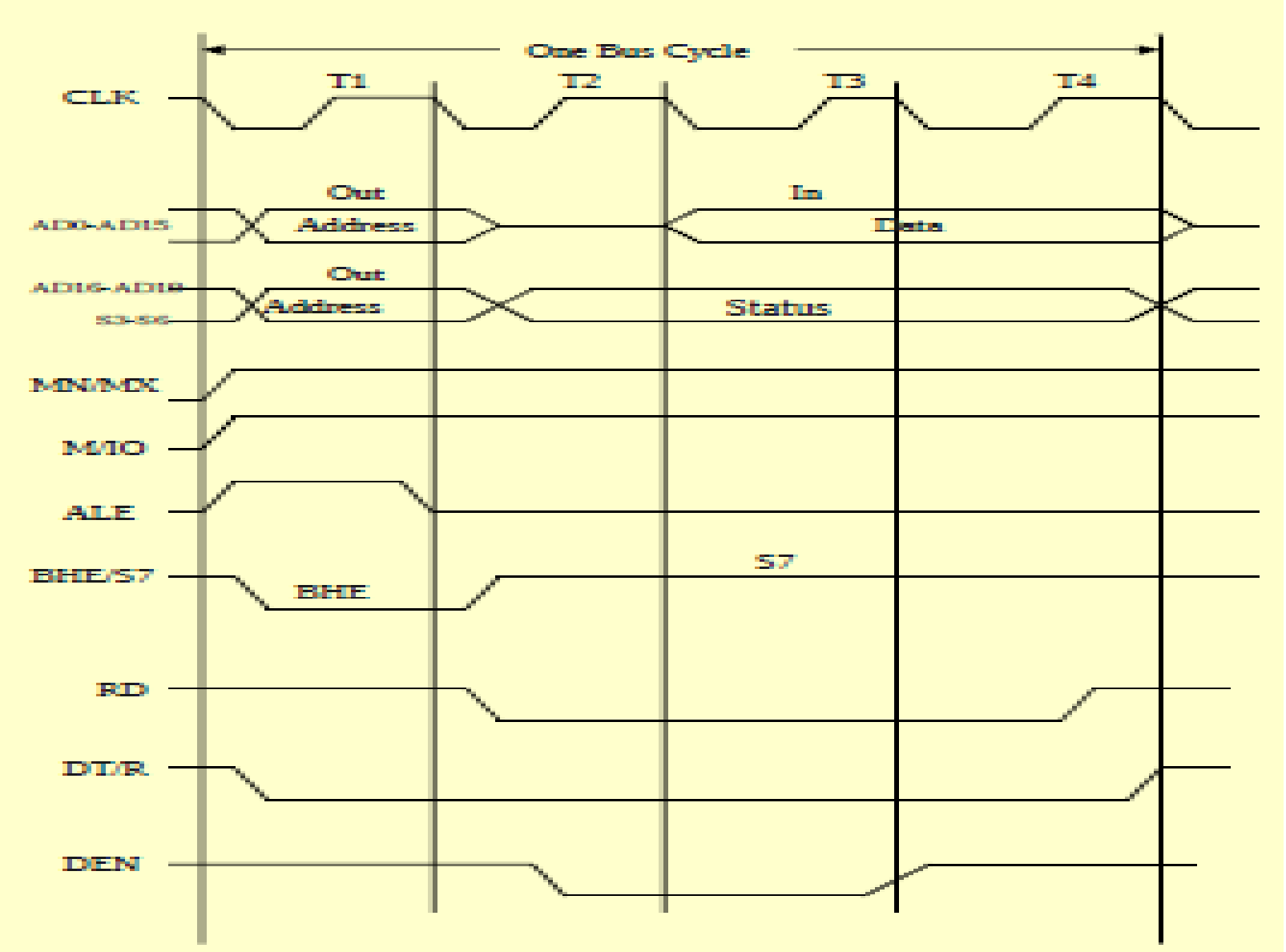
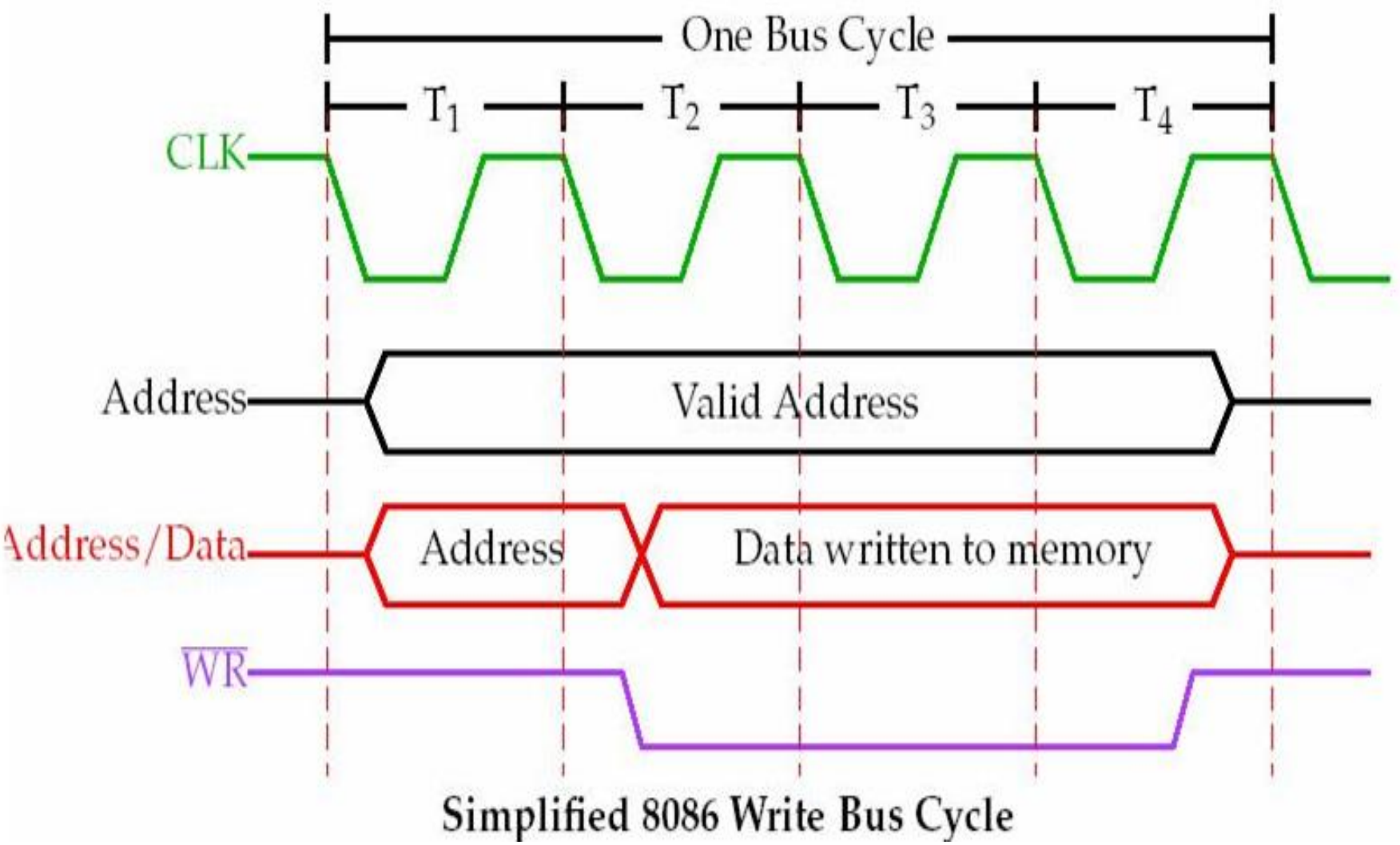


Figure . Timing Diagram for Read operation

•Write Cycle



Simplified 8086 Write Bus Cycle

8086 Memory Interfacing & address decoding

Memory interfacing

- The 8086 has 20- bit address bus.
- It can address up to 2^{20} bytes = 1 MB.
- A memory location stores 1 byte of information.
- A word (2 bytes) is stored in two consecutives memory locations.
- For ex:

  MOV [3245], 3BH

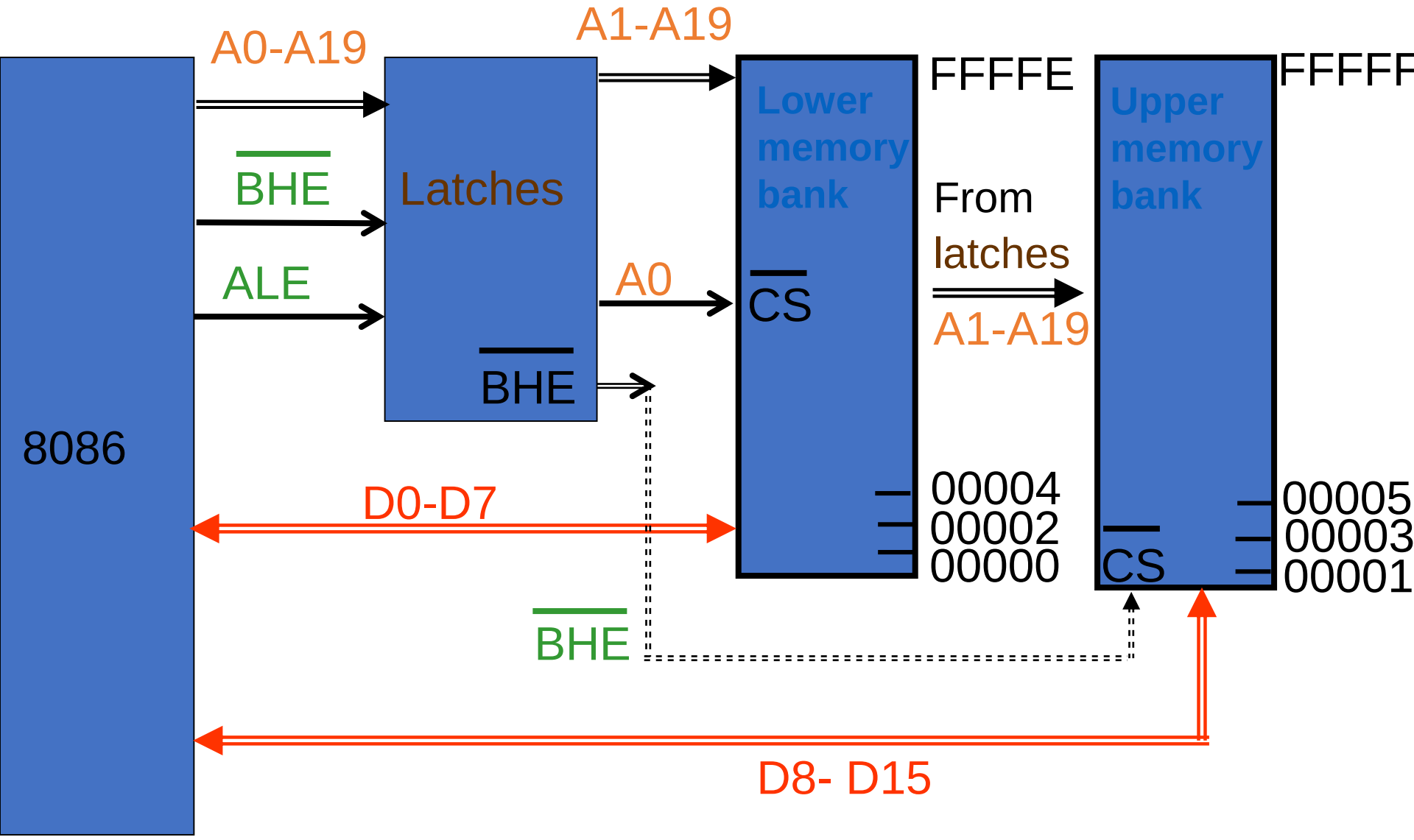
  MOV [3246],763BH

To make it possible to read or write a word With one machine cycle, the memory of 8086 is set up as two banks:

- Lower bank contain all the bytes which have even addresses 00000, 00002, 00004H, ……, FFFFEH connecting to data lines D0 throughD7

- Upper bank contain all bytes with odd addresses 00001, 00003H, 00005H, ……, FFFFH connecting to data lines D8- D15.

Memory interfacing…



- A0 is used as chip select for lower bank.
- BHE used as chip select for upper bank.
- One bus cycle is required to read or write a data word starting from even address.

- To read or write a data word starting from odd address, it requires two bus cycles.
- One bank is enabled for writing a byte into memory location. why?
  - To prevent the writing of an unwanted byte into an adjacent memory location.

Ex:

Determine the logical level(0 or 1), number of bus cycles and data bus lines used when the following instructions are executed:

1. MOV AX, [1000H].
2. MOV AX, [1001H].
3. MOV [1000H], AL.

Assume DS = 2000H.

MOV AX, [1000]

one bus cycle is required to execute this instruction? (even address)

- When the instruction MOV AX, [1000H] is executed; both A0 and $\overline{BHE}$ will go low and both lower and upper memory banks are enabled: (in one bus cycle)

- The low byte of the word is transferred from memory location 21000H to AL on D0-D7.

- The high byte of the word is transferred from memory location 21001H to AH on D8-D15.

MOV AX, [1001]

Two bus cycles are required to execute this instruction? (odd address)

- During the first bus cycle, the 8086:
  - Sends out address 21001H.(odd address)
  - Makes $\overline{BHE}$ low and A0 high.
  - Low byte of the word is transferred from memory location 21001H to AL on D8-D15.
- During the 2nd bus cycle, the 8086:
  - Sends out address 21002H.(even address)
  - A0 is made low and BHE high.
  - 2nd byte is read from 21002H on D0-D7 and put in AH.

MOV [1000H], AL

For executing this instruction, the 8086 mp:

- Sends out address 21000H.(even address)
- Makes $\overline{\text{BHE}}$ low and A0 high.
- The data is transferred from AL to memory location 21000H on data lines D0-D7 (in a lower bank as required).
- Since 8086 makes $\overline{\text{BHE}}$ high, any data available on D8-D15 will not be written in the memory location 21001H

Address decoder

- Several memory and I/O devices are required in computer system.
- They are connected to mp through decoders. The address of memory location or I/O device is sent out by the mp.
- It is the function of the decoder to:
  - produce a signal which will enables the ROM, RAM or port device.
  - make sure that only one device at a time is enabled to put data on the data lines.

Address decoding methods

- Every memory chip and I/O port have one pin by which it can be enabled (sometimes called chip selects (CS)).
- No data can be written into or read from the memory chips or I/O ports unless this pin is enabled.
- The pin input is normally low and can be activated using one of the following methods

Simple logic gates:

Using a combination of logic gates, one Can decode any address range.

The disadvantages of this method:

1.The excessive cost of the gates.

2. limited number of inputs.

PROM:

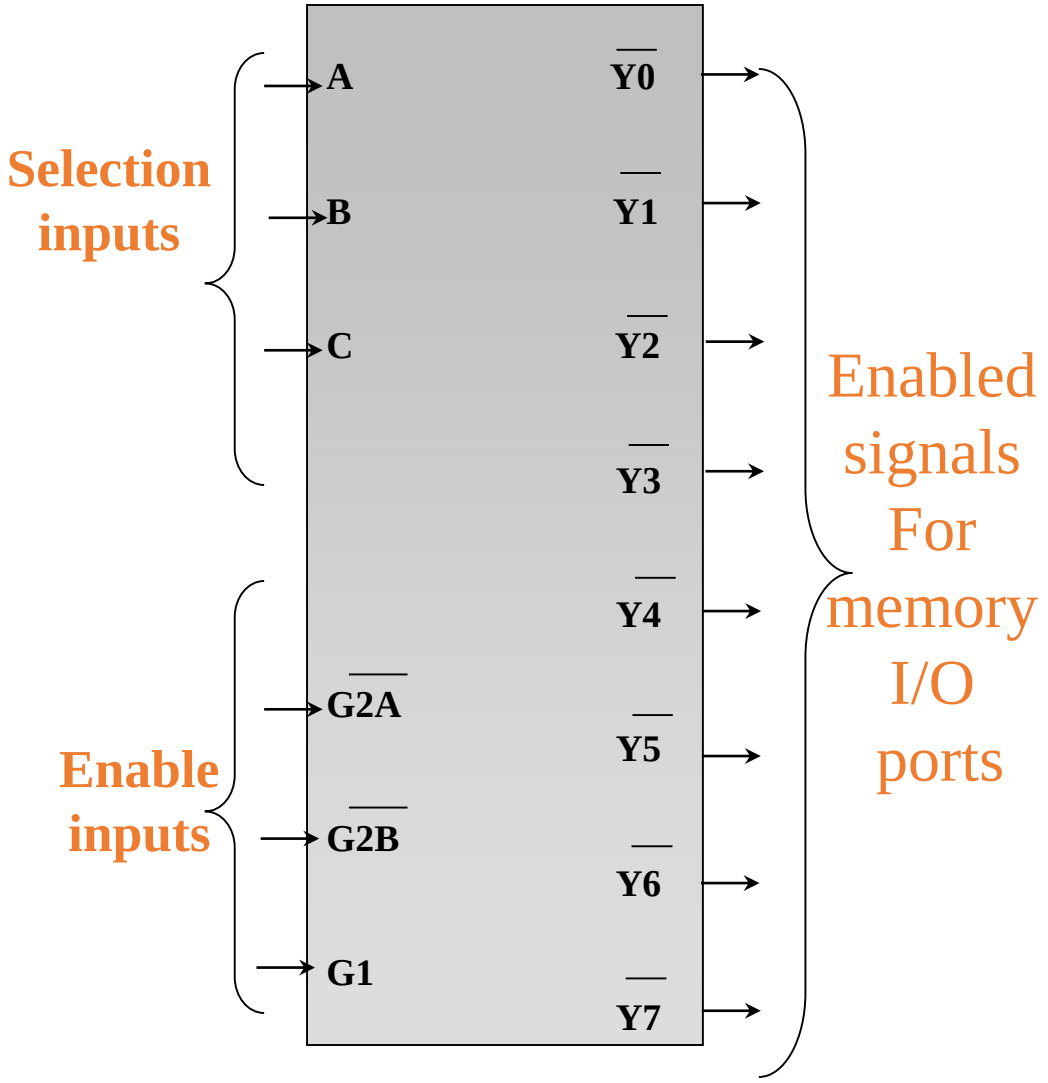
- PROM has a larger number of input connections which permit to select a specific area of memory without using additional electronic circuitry.
- As PROM is programmable, it can simply move the memory device to new address by programming a new PROM.

Decoder 74LS138:

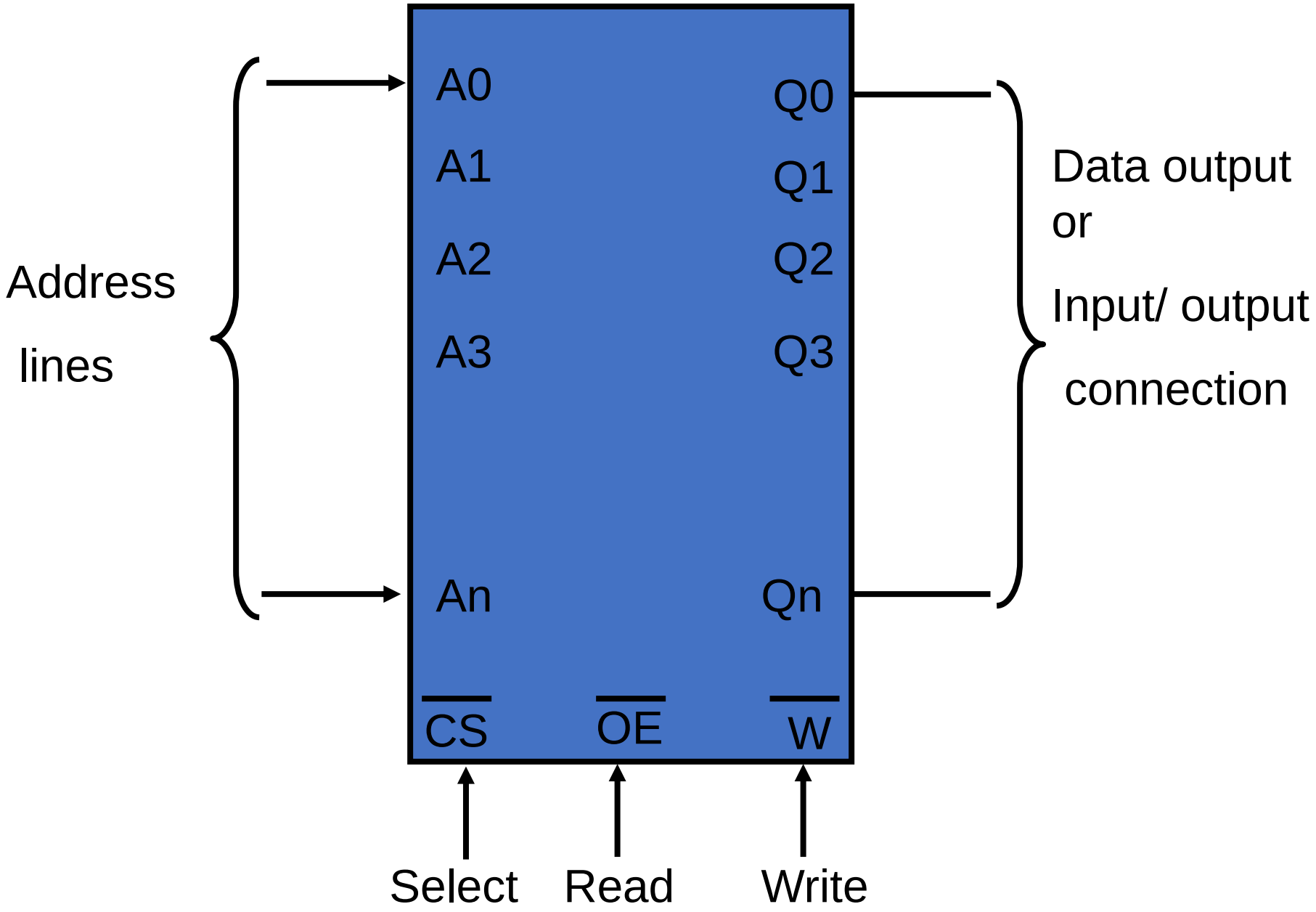
This is one of the most widely used address decoders. 74LS138 is enabled by making:

G2A & G2B inputs Low. G1 input high, then only one output of the decoder will be low at a time.

The output that will be low is determined by inputs: A, B and C.



Memory control connections:



- RAM memory generally has at least one $\overline{CS}$ or $\overline{S}$ input and ROM at least one $\overline{CE}$.
- If the $\overline{CE}$, $\overline{CS}$, $\overline{S}$ input is active, the memory device can perform read or write operation.
- If it is inactive the memory device cannot perform read or write operation.

ROM control connections:

- ROM usually has only one control input

Which is the output enable ($\overline{OE}$) or gate ($\overline{G}$), this allows data to flow out of the output data pins of the ROM.

- If $\overline{OE}$ and the selected input are both active, then the output is enable, if $\overline{OE}$ is inactive, the output is disabled at its high- impedance state.

- If the RAM has two control inputs, they are usually labelled $\overline{WE}$ and $\overline{OE}$ or $\overline{G}$.

- $\overline{WE}$: write enable must be active to Perform a memory write operation.
- $\overline{OE}$: must be active to perform a memory read operation.
- When these two controls $\overline{WE}$ and $\overline{OE}$ are present, they must never be active at the same time.

The memory systems "sees" the 8086 as a device with:

- *20 address connections (A19 to A0).*
- *16 data bus connections (D15 to D0).*
- *3 control signals, $\overline{M/IO}$, $\overline{RD}$, and $\overline{WR}$.*
- *A0 to select the lower bank.*
- *$\overline{BHE}$ to select the upper bank.*

ROM (EPROM) decoder example:

Use the decoder 74LS138 to select one of eight 2K byte starting address FF000H **to FFFFFH.**

Solution:

- 2K byte = 2 x 1024 = 2048 bytes

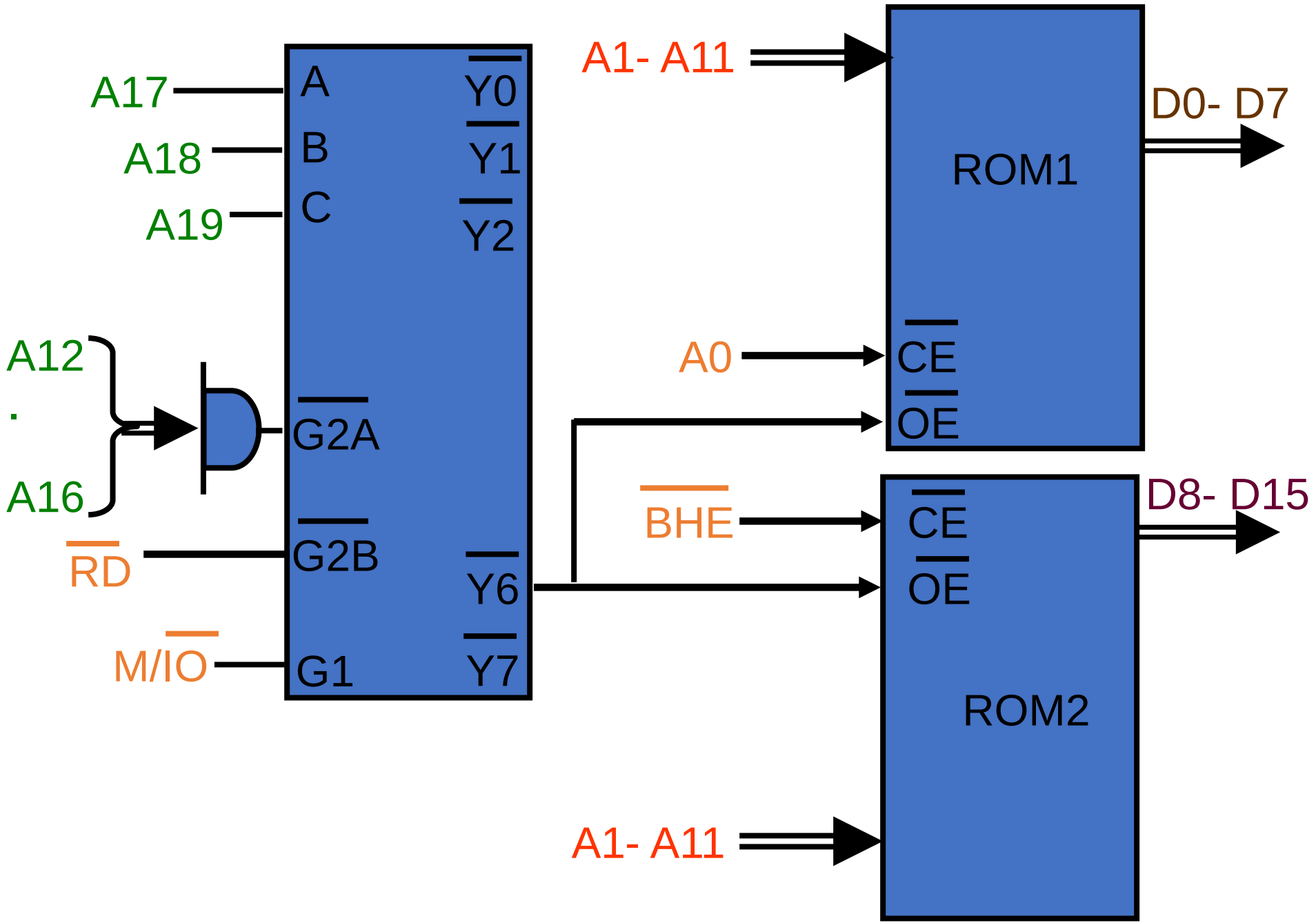
- 2^{11}= 2048 ⟶ 11 address lines …….A1- A11 are connecting to each ROM

- **A0** is connected to $\overline{CE}$ to select the lower bank.

- $\overline{\textbf{BHE}}$ is connected to $\overline{CE}$ to select the upper bank.

- $M/\overline{IO}$ is connected to G1 to enable memory chips.
- $\overline{RD}$ is connected to $\overline{G2A}$ to read ROM contents.
- A12- A16 are connected through NAND gate to $\overline{G2B}$.
- Address lines A17- A19 are applied to A, B and C pins.

ROM interfacing using 74LS 138 decoder.



Address Range

A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Addre s rang
1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	FF00
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF

RAM address decoding:

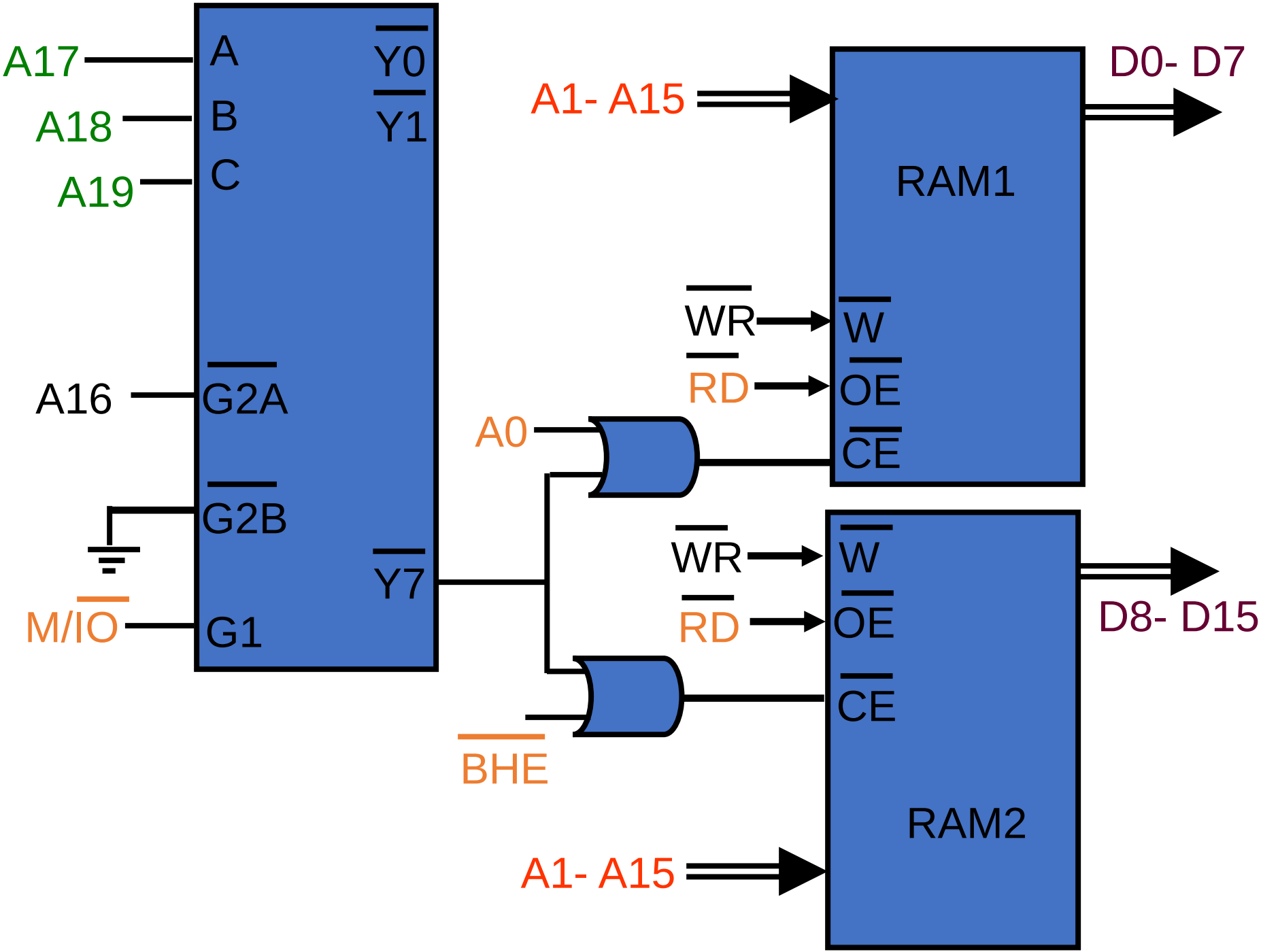
Use the decoder 74LS138 to select one of eight 32K byte. The starting address is E0000H.

Solution:

- 2^n = 32 x 1024 = 32768 bytes.

n = 15 address lines must be assigned to the RAM.

- A0 for selecting lower bank & $\overline{BHE}$ for upper bank.
- M/$\overline{IO}$ is connected to G1 of the decoder.
- $\overline{RD}$ is connected to $\overline{OE}$ pin of the RAM.
- $\overline{WR}$ is connected to $\overline{W}$ pin of the RAM.


A17
A18
A19
A16
M/IO
A
B
C
G2A
G2B
G1
Y0
Y1
Y7
A1- A15
D0- D7
RAM1
WR
RD
W
OE
CE
A0
BHE
D8- D15
RAM2

Memory interfacing in 8088 based system:

- **8088** is a 16-bit mp that communicate with the outside via 8- bit bidirectional data bus.
- This requires the 8088 to perform two m/c cycles to read or write a word.

- 8088 have 20 address bus to access 1M Byte of Memory.

& 8086 instruction set are identical and the registers are the same.

8088 Vs 8086 mp:

1) 8088 mp is 8 bit data bus D0-D7.
   All memory devices and ports system are connected onto D0-D7 lines. Address lines A0 through A19 are used to select a desired byte in memory.

2) 8088 does not produce the BHE signal, because 8088 read or write only a byte at a time (does not need it).
3) 8088 do two m/c cycle to read or write a word.

4) 8088 memory is not divided into two banks as 8086, it consist of a single bank

5) 8086 has an M/$\overline{IO}$ pin, but 8088 has an IO/$\overline{M}$ pin.

6) 8088 instruction byte queue is 4- byte long instead of 6.

8088 memory address decoding:

EX1:

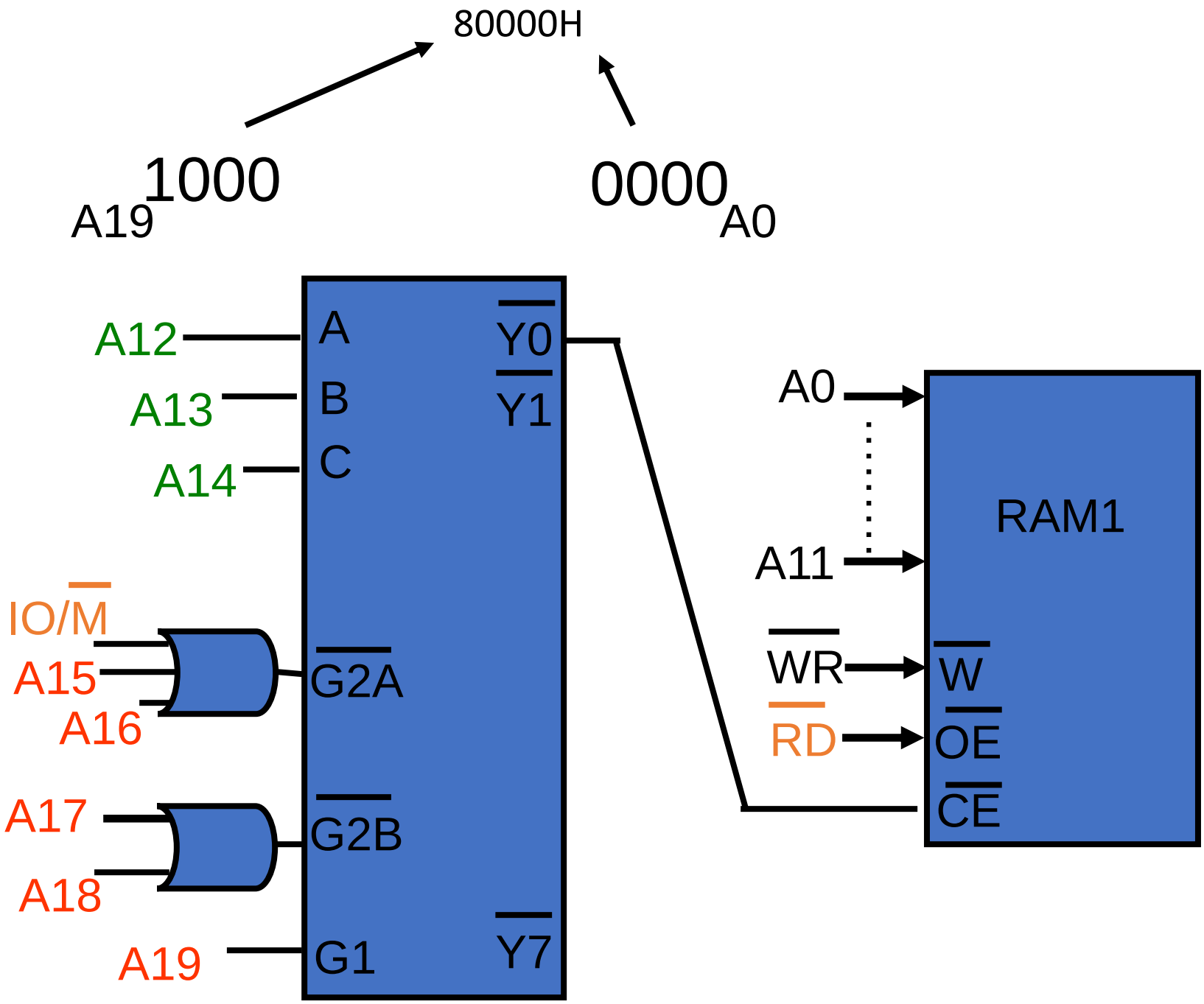
Use address decoder to show how decoder 74LS138 can be connected to select one of 8x 4Kbyte RAMs starting address 80000H.

How many address lines required for 4K bytes?

4 K = 4 x 1024 = 4096 $2^{12} = 4096$

12 address lines required A0 to A11 must be connected to the RAM.

A12 , A13 & A14 to select one of the 8 RAMs.


80000H
A19
1000
0000
A0
A12
A13
A14
A
B
C
Y0
Y1
IO/M
A15
A16
G2A
A17
A18
G2B
A19
G1
Y7
A0
A11
RAM1
WR
W
RD
OE
CE

EX2:

Map a 16Kx8RAM chip to an 8088 based system, beginning at B8000H using decoder 74LS138.

Solution:

16K byte = 16 x1024

2^{14} = 16x 1024 n = 14 address lines decoded on the chip (A0– A13).The remaining 6(A14-A19) must be decoded externally (using 74LS138).

B8000H = 1011 1000 0000 0000 0000B

The remaining 6 are 1011 10 B

Last address is: 1011 1011 1111 1111 1111 B

B B F F F H