Features of 80186, 80286, 80386, 80486

80186 Basic Features

- The 80186 contains 16 – bit data bus
- The internal register structure of 80186 is virtually identical to the 8086
- About the only difference is that the 80186 contain additional reserved interrupt vectors and some very powerful built-in I/O features

Clock Generator:

- The internal clock generator replaces the external 8284A clock generator used with the 8086 microprocessors. This reduces the component count in a system

Programmable Interrupt Controller:

- The PIC arbitrates all internal and external interrupts and controls up to two external 8259A PICs. When an external 8259 is attached, the 80186 microprocessors function as the master and the 8259 functions as the slave

Timers:

- The timer section contains three fully programmable 16-bit timers
- The timers 0 and 1 generate wave-forms for external use and driven by either the master clock of the 80186 or by an external clock
- The third timer, timer 2 is internal and clocked by the master clock

Programmable DMA Unit:

- The programmable DMA unit contains two DMA channels, or four DMA channels in some models

- Each channel can transfer data between memory locations, between memory and IO, or between IO devices

Programmable chip selection unit:

- The chip selection is a built-in programmable memory and I/O decoder
- It has 6 output lines to select memory, 7 lines to select I/O

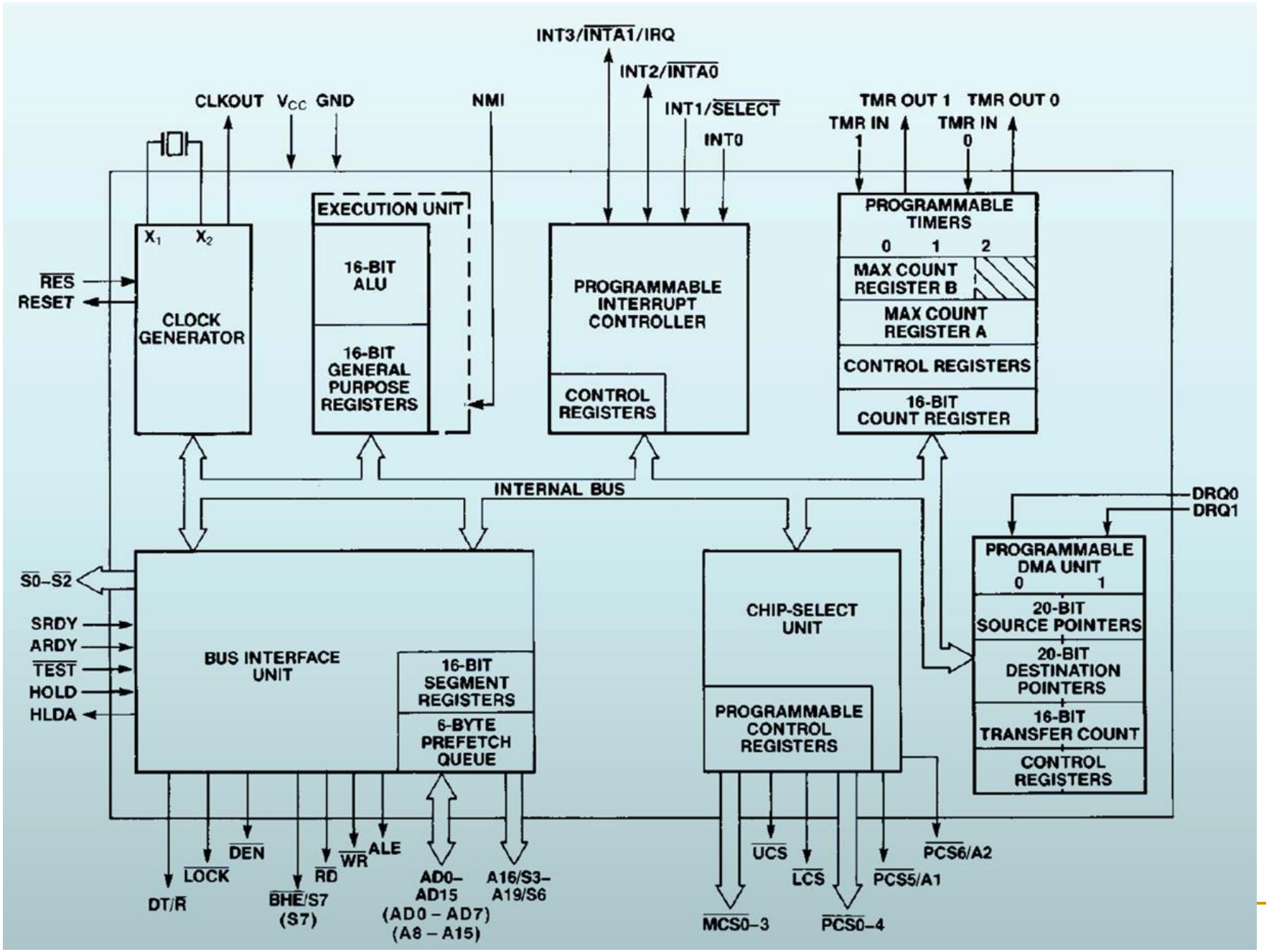
Power save/Power Down Feature:

- The power save feature allows the system clock to be divided by 4, 8, or 16 to reduce power consumption

- The power saving feature is started by software and exited by a hardware event such as an interrupt

Refresh Control Unit:

- The refresh control unit generates the refresh row address at the interval programmed


INT3/INTA1/IRQ
INT2/INTA0
INT1/SELECT
INT0
CLKOUT
VCC
GND
NMI
TMR OUT 1
TMR OUT 0
TMR IN 1
TMR IN 0
EXECUTION UNIT
16-BIT ALU
16-BIT GENERAL PURPOSE REGISTERS
X1
X2
CLOCK GENERATOR
RES
RESET
PROGRAMMABLE INTERRUPT CONTROLLER
CONTROL REGISTERS
PROGRAMMABLE TIMERS
0 1 2
MAX COUNT REGISTER B
MAX COUNT REGISTER A
CONTROL REGISTERS
16-BIT COUNT REGISTER
INTERNAL BUS
DRQ0
DRQ1
PROGRAMMABLE DMA UNIT
0 1
20-BIT SOURCE POINTERS
20-BIT DESTINATION POINTERS
16-BIT TRANSFER COUNT
CONTROL REGISTERS
S0–S2
SRDY
ARDY
TEST
HOLD
HLDA
BUS INTERFACE UNIT
16-BIT SEGMENT REGISTERS
6-BYTE PREFETCH QUEUE
CHIP-SELECT UNIT
PROGRAMMABLE CONTROL REGISTERS
DEN
LOCK
DT/R
RD
BHE/S7
(S7)
WR
ALE
AD0–AD15
(AD0 – AD7)
(A8 – A15)
A16/S3–A19/S6
UCS
LCS
PCS6/A2
PCS5/A1
MCS0–3
PCS0–4

Instruction set of 80186

- **The 80186 instruction set is divided into seven types**
  1. **Data transfer**
  2. **Arithmetic**
  3. **Shift/rotate**
  4. **String**
  5. **Control transfer**
  6. **High level instructions**
  7. **Processor control**
- **80186 includes 10 new instructions beyond the 8086**

Additional Instructions

- Data Transfer
  - PUSHA - Push all registers onto stack
  - POPA -Pop all registers from stack
  - PUSH immediate - Push immediate numbers into stack
- Arithmetic
  - IMUL destination register, source, immediate data
    - {immediate data * source -> destination }
- Logical
  - SHIFT/ROTATE destination, immediate data shifts/rotates register or Memory contents by the number of times specified in Immediate data

Additional Instructions....

- String Instructions
  - INS - Input string byte or string word
  - OUTS - Output string byte or string word

- High Level Instructions
  - ENTER - Format stack for procedure entry
  - LEAVE - Restore stack for procedure exit
  - BOUND - Detect values outside predefined range

80286 Basic Features

- The 80286 microprocessor is an advanced version of the 8086 microprocessor that is designed for multi user and multitasking environments
- The 80286 addresses 16 M Byte of physical memory and 1G Bytes of virtual memory by using its memory-management system
- The 80286 is basically an 8086 that is optimized to execute instructions in fewer clocking periods than the 8086

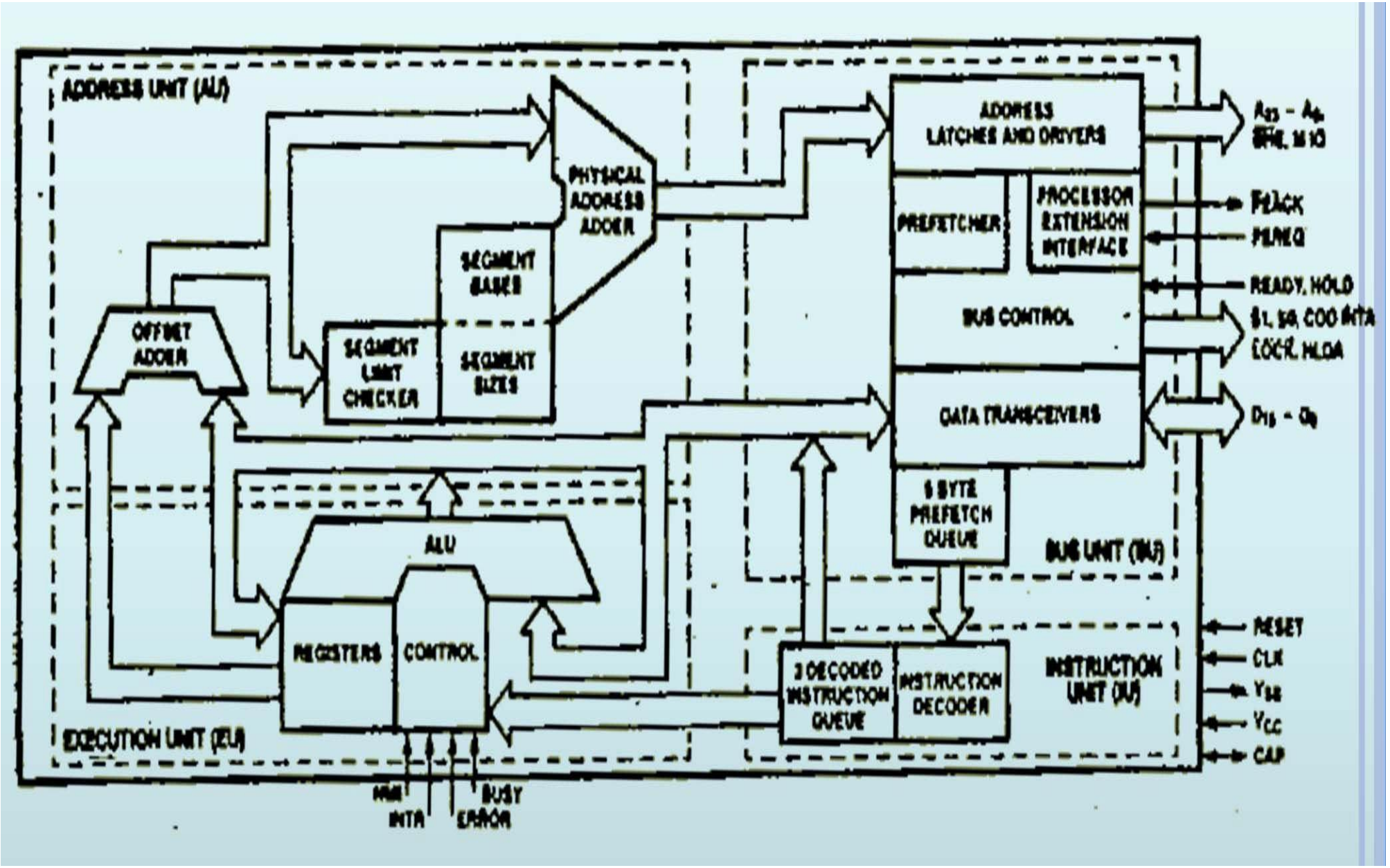
- Like the 80186, the 80286 doesn't incorporate internal peripherals; instead it contains a memory-management unit (MMU)

- The 80286 operates in both the real and protected modes
- In the real mode, the 80286 addresses a 1MByte memory address space and is virtually identical to 8086, fully object-code compatible with the 8086 and 8088

- In the protected mode, the 80286 addresses a 16MByte physical memory space, but can access 1GB of Virtual memory

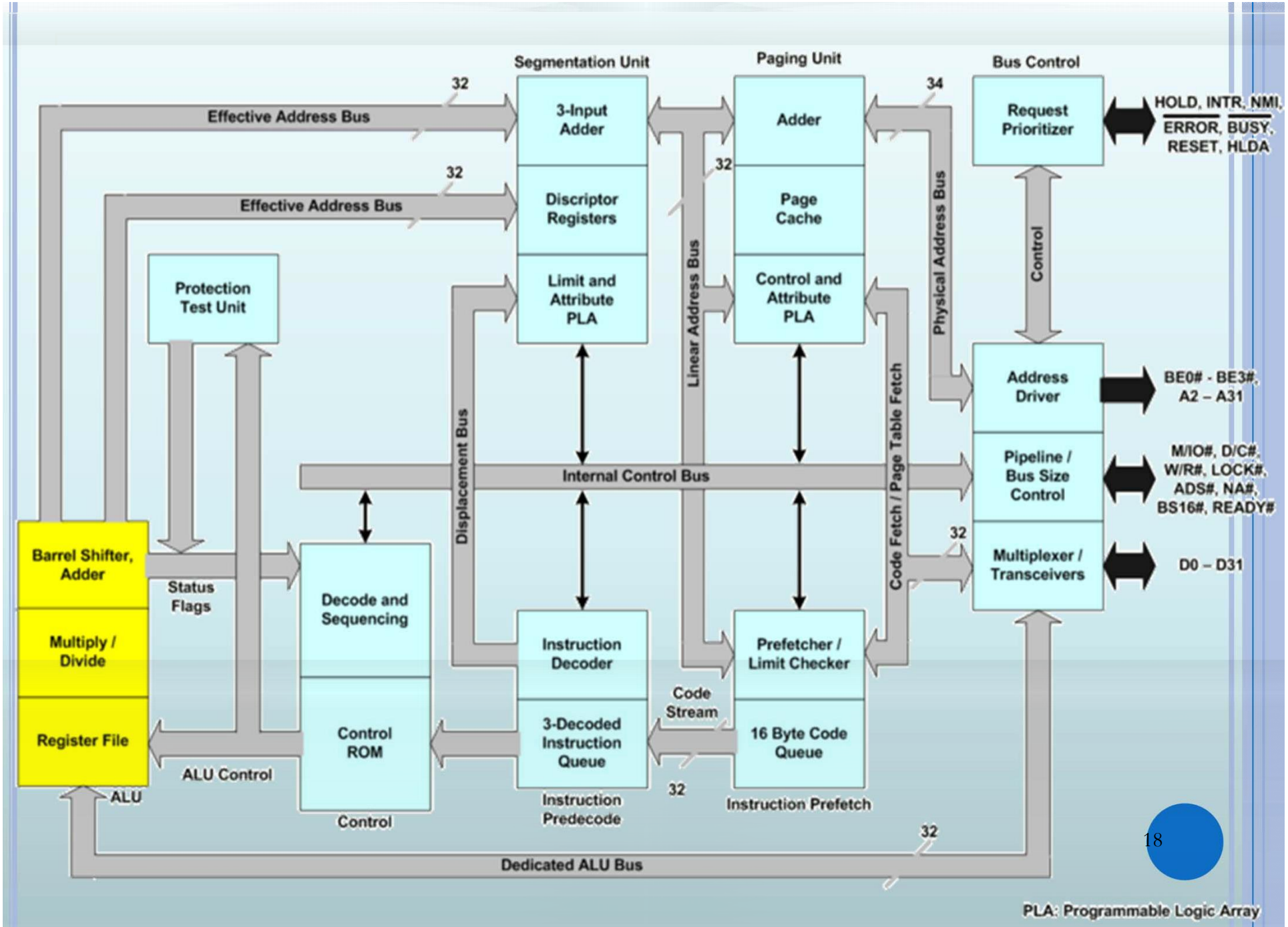
- The clock is provided by the 82284 clock generator, and the system control signals are provided by the 82288 system bus controller

- The 80286 contains the same instructions except for a handful of additional instructions that control the memory-management nit


ADDRESS UNIT (AU)
PHYSICAL ADDRESS ADDER
SEGMENT BASES
SEGMENT LIMIT CHECKER
SEGMENT SIZES
OFFSET ADDER
ADDRESS LATCHES AND DRIVERS
PREFETCHER
PROCESSOR EXTENSION INTERFACE
BUS CONTROL
DATA TRANSCEIVERS
6 BYTE PREFETCH QUEUE
BUS UNIT (BU)
ALU
REGISTERS
CONTROL
EXECUTION UNIT (EU)
3 DECODED INSTRUCTION QUEUE
INSTRUCTION DECODER
INSTRUCTION UNIT (IU)
INTA
BUSY
ERROR
RESET
CLK
CAP

80386 Microprocessor

- The Internal Architecture of 80386 is divided into 3 sections.
- Central processing unit
- Memory management unit
- Bus interface unit
- Central processing unit is further divided into Execution unit and Instruction unit
- Execution unit has 8 General purpose and 8 Special purpose registers which are either used for handling data or calculating offset addresses.


Segmentation Unit
Paging Unit
Bus Control
32
34
Effective Address Bus
3-Input Adder
Adder
Request Prioritizer
HOLD, INTR, NMI,
ERROR, BUSY,
RESET, HLDA
32
Effective Address Bus
Discriptor Registers
Page Cache
Protection Test Unit
Limit and Attribute PLA
Control and Attribute PLA
Linear Address Bus
Physical Address Bus
Control
Address Driver
BE0# - BE3#,
A2 – A31
Displacement Bus
Internal Control Bus
Pipeline / Bus Size Control
M/IO#, D/C#,
W/R#, LOCK#,
ADS#, NA#,
BS16#, READY#
Code Fetch / Page Table Fetch
32
Barrel Shifter, Adder
Multiply / Divide
Register File
Status Flags
Decode and Sequencing
Multiplexer / Transceivers
D0 – D31
Instruction Decoder
Prefetcher / Limit Checker
Code Stream
Control ROM
3-Decoded Instruction Queue
16 Byte Code Queue
ALU Control
ALU
Control
Instruction Predecode
32
Instruction Prefetch
32
Dedicated ALU Bus
PLA: Programmable Logic Array

FEATURES OF 80386

- Two versions of 80386 are commonly available:

- 80386DX
  - 32 Bit Address and 32 Bit Data Bus
  - 132 Pin PGA
  - Address 4GB Memory
- 80386SX
  - 24-bit Address Bus
  - 16-Bit Data Bus
  - 16 MB of memory

80386 Basic Features

- The 80386 microprocessor is an enhanced version of the 80286 microprocessor and includes a memory-management unit is enhanced to provide memory paging

- The 80386 also includes 32-bit extended registers and a 32-bit address and data bus

- The 80386 has a physical memory size of 4GBytes that can be addressed as a virtual memory with up to 64TBytes

- The 80386 is operated in the pipelined mode, it sends the address of the next instruction or memory data to the memory system prior to completing the execution of the current instruction

- This allows the memory system to begin fetching the next instruction or data before the current is completed

- This increases access time, thus reducing the speed of the memory

- The I/O structure of the 80386 is almost identical to the 80286, except that I/O can be inhibited when the 80386 is operated in the protected mode through the I/O bit protection map

- The register set of the 80386 contains extended versions of the registers introduced on the 80286 microprocessor. These extended registers include EAX, EBX, ECX, EDX, EBP, ESP, EDI, ESI, EIP and EFLAGS

- The instruction set of the 80386 is enhanced to include instructions that address the 32-bit extended register set

- Interrupts, in the 80386 microprocessor, have been expanded to include additional predefined interrupts in the interrupt vector table
- The 80386 memory manager is similar to the 80286, except the physical addresses generated by the MMU are 32 bits wide instead of 24-bits
- The 80386 is also capable of paging
- The 80386 is operated in the real mode (i.e. 8086 mode) when it is reset

- The real mode allows the microprocessor to address data in the first 1MByte of memory

- In the protected mode, 80386 addresses any location in its 4G bytes of physical address space

80486 Basic Features

- The 80486 microprocessor is an improved version of the 80386 microprocessor that contains an 8K-byte cache and an 80387 arithmetic co processor; it executes many instructions in one clocking period

- The 80486 microprocessor executes a few new instructions that control the internal cache memory

- A new feature found in the 80486 in the BIST (built-in self-test) that tests the microprocessor, coprocessor, and cache at reset time
- If the 80486 passes the test, EAX contains a zero
- Additional test registers are added to the 80486 to allow the cache memory to be tested
- These new test registers are TR3 (cache data), TR4 (cache status), and TR5 (cache control)