

DAY 2 Lab report:

The README file contains information about the parameters in various steps of characterization

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Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
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vsc
vsdtotal 12
-rw-rwxr-x 5 vsduser docker 4096 Jun 28 2021 pkds
-rw-rwxr-x 5 vsduser docker 4096 Jun 29 2021 openlane_old
-rw-rwxr-x 1 vsduser docker 31784 Jun 29 2021 openlane
-rw-rwxr-x 1 vsduser docker 1288 Jun 29 2021 openlane.tcl
-rw-rwxr-x 1 vsduser docker 2359 Jun 29 2021 general.tcl
-rw-rwxr-x 1 vsduser docker 1527 Jun 29 2021 fluorolan.tcl
-rw-rwxr-x 1 vsduser docker 808 Jun 29 2021 cts.tcl
-vsc-rwrxr-xr-x 1 vsduser docker 1113 Jun 29 2021 checkers.tcl
-vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ ls -ltr
-rw-rwxr-x 14 vsduser docker 4096 Jun 29 2021 scripts
drwxrwxr-x 1 vsduser docker 2078 Jun 29 2021 flowdesigns.py
drwxrwxr-x 1 vsduser docker 1024 Jun 29 2021 report_generation_wrapper.py
drwxrwxr-x 3 vsduser docker 4096 Jun 29 2021 regression_results
drwxrwxr-x 1 vsduser docker 25599 Jun 29 2021 README.md
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-rw-rw-r--r-- 1 vsduser docker 1612 Jun 29 2021 LICENSE
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drwxrwxr-x 1 vsduser docker 1285 Jun 29 2021 CONTRIBUTING.md
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drwxrwxr-xr-x 1 vsduser vsduser 963 May 20 2023 default.cvcrc
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drwsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ cd configurations
vsduser@vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ cd configurations
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-vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ ls -ltr
-rwxrwxr-x 1 vsduser docker 1117 Jun 29 2021 synthesis.tcl
-rw-rwxr-x 1 vsduser docker 1897 Jun 29 2021 routing.tcl
drwxrwxr-xr-x 1 vsduser docker 31784 Jun 29 2021 README.md
-rw-rwxr-xr-x 1 vsduser docker 1288 Jun 29 2021 placement.tcl
-rw-rwxr-xr-x 1 vsduser docker 2359 Jun 29 2021 general.tcl
-rw-rwxr-xr-x 1 vsduser docker 1527 Jun 29 2021 fluorolan.tcl
-vsc-rwrxr-xr-x 1 vsduser docker 808 Jun 29 2021 cts.tcl
-vsc-rwrxr-xr-x 1 vsduser docker 1113 Jun 29 2021 checkers.tcl
-vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/configuration$ less README.md
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All of these are the switches

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vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/15-12_22-23/reports/synthesis
vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/configuration

# Variables Information
## Required variables
| Variable | Description |
|-----|-----|
| 'DESIGN_NAME' | The name of the top level module of the design |
| 'VERILOG_FILES' | The path of the design's verilog files |
| 'CLOCK_PERIOD' | The clock period used in simulation. |
| 'CLOCK_NET' | The name of the Net Input to Root clock buffer used in Clock Tree Synthesis. |
| 'CLOCK_PORT' | The name of the design's clock port used in Static Timing Analysis. |

## Optional variables
These variables are optional that can be specified in the design configuration file.

### Synthesis
| Variable | Description |
|-----|-----|
| 'LIS_SYNTH' | The library used for synthesis by yosys. <br> (Default: $:env(PDK)/libs.ref$/:env(STD_CELL_LIBRARY)/lib/sky130_fd_sc_hd_tt_02SC_1v00.lib) |
| 'SYNTH_BIN' | The yosys binary used in the flow. <br> (Default: 'yosys') |
| 'SYNTH_DRIVING_CELL' | The cell to drive the input ports. <br>(Default: 'sky130_fd_sc_hd_inv_8') |
| 'SYNTH_DRIVING_CELL_PIN' | The name of the SYNTH_DRIVING_CELL output pin. <br>(Default: 'Y') |
| 'SYNTH_CAP_LOAD' | The capacitive load on the output ports in fentofarads. <br> (Default: '17.65' ff) |
| 'SYNTH_EQUIV_OUTPUT' | The equivalent output of the design in fentofarads. <br> (Default: '17.65' ff) |
| 'SYNTH_MAX_TRANS' | The max transition time (slow from high to low or low to high on cell inputs in ns. Used in synthesis) <br> (Default: Calculated at runtime as '10% of the provided clock period, unless this exceeds a set DEFAULT_MAX_TRAN, in which case it will be used as is.) |
| 'SYNTH_STRATEGY' | Strategies for abc logic synthesis and technology mapping <br> Possible values are 'DELAY_AREA 0-3/0-2'; the first part refers to the optimization target of the synthesis strategy (area vs. delay) and the second one is an index. <br> (Default: 'AREA 0') |
| 'SYNTH_BUFFERING' | Enables abc cell buffering <br> Enabled = 1, Disabled = 0 <br> (Default: '1') |
| 'SYNTH_EQUIV_IN' | Enables abc cell static (non-dynamic) buffering <br> Enabled = 1, Disabled = 0 <br> (Default: '0') |
| 'SYNTH_READ_BLACKBOX_LIB' | A flag that enable reading the full(untrimmed) liberty file as a blackbox for synthesis. Please note that this is not used in technology mapping. This should only be used when trying to preserve gate instances in the rtl of the design. <br> Enabled = 1, Disabled = 0 <br> (Default: '0') |
| 'SYNTH_NO_FLAT' | A flag that disables flattening the hierarchy during synthesis, only flattening it after synthesis, mapping and optimizations. <br> Enabled = 1, Disabled = 0 <br> (Default: '0') |
| 'SYNTH_SHARE_RESOURCES' | A flag that enables yosys to reduce the number of cells by distributing shareable resources and merging them. <br> Enabled = 1, Disabled = 0 <br> (Default: '0') |
| 'SYNTH_ADDER_TYPE' | Adder type to which the $add and $sub operators are mapped to. <br> Possible values are 'YOSYS/FA/RCA/CSA'; where 'YOSYS' refers to using Yosys internal adder definition, 'FA' refers to full-adder structure, 'RCA' refers to ripple carry adder structure, and 'CSA' refers to carry select adder. <br> (Default: 'YOSYS') |
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vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/configuration

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| 'VERILOG_INCLUDE_DIRS' | Specifies the verilog includes directories. <br> Optional. |
| 'SYNTH_FLAT_TOP' | Specifies whether or not the top level should be flattened during elaboration. 1 = True, 0 = False <br> Default: '0'. |
| 'IO_PCT' | Specifies the percentage of the clock period used in the input/output delays. Ranges from 0 to 1.0. <br> (Default: '0.2') |

### Floorplanning
| Variable | Description |
|-----|-----|
| 'FP_CORE_UTIL' | The core utilization percentage. <br> (Default: '50 percent') |
| 'FP_ASPECT_RATIO' | The core's aspect ratio (height / width). <br> (Default: '1') |
| 'FP_SIZING' | Whether to use relative sizing by making use of 'FP_CORE_UTIL' or absolute one using 'DIE_AREA'. <br> (Default: '"relative" - accepts "absolute" as well) |
| 'DIE_AREA' | Specific die area to be used in floorplanning. Specified as a 4-corner rectangle. Units in mm <br> (Default: unset) |
| 'FP_IO_Metal' | The metal layer on which to place the I/O pins horizontally (top and bottom of the die). <br> (Default: '4') |
| 'FP_IO_VMetal' | The metal layer on which to place the I/O pins vertically (sides of the die) <br> (Default: '3') |
| 'FP_PLACEMENT_MODE' | Selects the mode of random placement algorithm. Default mode <br> (Default: '1') |
| 'FP_WELTAP_CELL' | The name of the weltap cell during weltap insertion. |
| 'FP_ENDCAP_CELL' | The name of the endcap cell during endcap insertion. |
| 'FP_PDN_VOFFSET' | The offset of the vertical power stripes on the metal layer 4 in the power distribution network <br> (Default: '16.32') |
| 'FP_PDN_VPITCH' | The pitch of the vertical power stripes on the metal layer 4 in the power distribution network <br> (Default: '153.6') |
| 'FP_PDN_HOFFSET' | The offset of the horizontal power stripes on the metal layer 5 in the power distribution network <br> (Default: '16.65') |
| 'FP_PDN_HPITCH' | The pitch of the horizontal power stripes on the metal layer 5 in the power distribution network <br> (Default: '153.18') |
| 'FP_PDN_AUTO_ADJUST' | Decides whether to let the flow should attempt to re-adjust the power grid, in order for it to fit inside the core area of the design, if needed. <br> 1=enabled, 0=disabled (Default: '1') |
| 'FP_TAPCELL_DIST' | The horizontal distance between two tapcell columns <br> (Default: '14') |
| 'FP_IO_VEXTEND' | Extends the vertical I/O pins outside of the die by the specified units <br> (Default: '-1' Disabled) |
| 'FP_IO_HEXTEND' | Extends the horizontal I/O pins outside of the die by the specified units <br> (Default: '-1' Disabled) |
| 'FP_IO_VWIDTH' | The length of the vertical I/O pins in microns. <br> (Default: '4') |
| 'FP_IO_HLENGTH' | The length of the horizontal I/O pins in microns. <br> (Default: '4') |
| 'FP_IO_VTHICKNESS_MULT' | A multiplier for vertical pin thickness. Base thickness is the pins layer minwidth <br> (Default: '2') |
| 'FP_IO_HTHICKNESS_MULT' | A multiplier for horizontal pin thickness. Base thickness is the pins layer minwidth <br> (Default: '2') |
| 'BOTTOM_MARGIN_MULT' | The core margin, in multiples of site heights, from the bottom boundary. <br> (Default: '4') |
| 'TOP_MARGIN_MULT' | The core margin, in multiples of site heights, from the top boundary. <br> (Default: '4') |
| 'LEFT_MARGIN_MULT' | The core margin, in multiples of site widths, from the left boundary. <br> (Default: '12') |
| 'RIGHT_MARGIN_MULT' | The core margin, in multiples of site widths, from the right boundary. <br> (Default: '12') |
| 'FP_PDN_CORE_RING' | Enables adding a core ring around the design. More details on the control variables in the pdk configurations documentation. 0=Disable 1=Enable. <br> (Default: '0') |
| 'FP_PDN_ENABLE_RAILS' | Enables the creation of rails in the power grid. 0=Disable 1=Enable. <br> (Default: '1') |
| 'FP_PDN_CHECK_NODES' | Enables checking for unconnected nodes in the power grid. 0=Disable 1=Enable. <br> (Default: '1') |
| 'FP_HORIZONTAL_HALO' | Sets the horizontal halo around the tie-in and decap cells. The value provided is in microns. <br> Default: '10' |
| 'FP_VERTICAL_HALO' | Sets the vertical halo around the tie-in and decap cells. The value provided is in microns. <br> Default: set to the value of 'FP_HORIZONTAL_HALO' |
| 'DESIGN_IS_CORE' | Controls the layers used in the power grid. Depending on whether the design is the core or a macro inside the core. 1=is a Core, 0=is a Macro <br> (Default: '1') |
| 'FP_PIN_ORDER_CFG' | Points to the pin order configuration file to set the pins in specific directions (S, W, E, N). Check this [file][0] as an example. If not set, the
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| 'SYNTH_ADDER_TYPE' | Adder type to which the $add and $sub operators are mapped to. <br> Possible values are 'YOSYS/FA/RCA/CSA'; where 'YOSYS' refers to using Yosys internal adder definition, 'FA' refers to full-adder structure, 'RCA' refers to ripple carry adder structure, and 'CSA' refers to carry select adder. <br> (Default: 'YOSYS') |
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vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/configuration

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| 'VERILOG_INCLUDE_DIRS' | Specifies the verilog includes directories. <br> Optional. |
| 'SYNTH_FLAT_TOP' | Specifies whether or not the top level should be flattened during elaboration. 1 = True, 0 = False <br> Default: '0'. |
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### Floorplanning
| Variable | Description |
|-----|-----|
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| 'FP_ASPECT_RATIO' | The core's aspect ratio (height / width). <br> (Default: '1') |
| 'FP_SIZING' | Whether to use relative sizing by making use of 'FP_CORE_UTIL' or absolute one using 'DIE_AREA'. <br> (Default: '"relative" - accepts "absolute" as well) |
| 'DIE_AREA' | Specific die area to be used in floorplanning. Specified as a 4-corner rectangle. Units in mm <br> (Default: unset) |
| 'FP_IO_Metal' | The metal layer on which to place the I/O pins horizontally (top and bottom of the die). <br> (Default: '4') |
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| 'FP_PDN_HOFFSET' | The offset of the horizontal power stripes on the metal layer 5 in the power distribution network <br> (Default: '16.65') |
| 'FP_PDN_HPITCH' | The pitch of the horizontal power stripes on the metal layer 5 in the power distribution network <br> (Default: '153.18') |
| 'FP_PDN_AUTO_ADJUST' | Decides whether to let the flow should attempt to re-adjust the power grid, in order for it to fit inside the core area of the design, if needed. <br> 1=enabled, 0=disabled (Default: '1') |
| 'FP_TAPCELL_DIST' | The horizontal distance between two tapcell columns <br> (Default: '14') |
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| 'TOP_MARGIN_MULT' | The core margin, in multiples of site heights, from the top boundary. <br> (Default: '4') |
| 'LEFT_MARGIN_MULT' | The core margin, in multiples of site widths, from the left boundary. <br> (Default: '12') |
| 'RIGHT_MARGIN_MULT' | The core margin, in multiples of site widths, from the right boundary. <br> (Default: '12') |
| 'FP_PDN_CORE_RING' | Enables adding a core ring around the design. More details on the control variables in the pdk configurations documentation. 0=Disable 1=Enable. <br> (Default: '0') |
| 'FP_PDN_ENABLE_RAILS' | Enables the creation of rails in the power grid. 0=Disable 1=Enable. <br> (Default: '1') |
| 'FP_PDN_CHECK_NODES' | Enables checking for unconnected nodes in the power grid. 0=Disable 1=Enable. <br> (Default: '1') |
| 'FP_HORIZONTAL_HALO' | Sets the horizontal halo around the tie-in and decap cells. The value provided is in microns. <br> Default: '10' |
| 'FP_VERTICAL_HALO' | Sets the vertical halo around the tie-in and decap cells. The value provided is in microns. <br> Default: set to the value of 'FP_HORIZONTAL_HALO' |
| 'DESIGN_IS_CORE' | Controls the layers used in the power grid. Depending on whether the design is the core or a macro inside the core. 1=is a Core, 0=is a Macro <br> (Default: '1') |
| 'FP_PIN_ORDER_CFG' | Points to the pin order configuration file to set the pins in specific directions (S, W, E, N). Check this [file][0] as an example. If not set, the
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vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/configuration

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| 'SYNTH_USE_P0_PINS_DEFINES' | Specifies the power guard used in the verilog source code to specify the power and ground pins. This is used to automatically extract 'VDD_NETS' and 'GND_NET' variables from the verilog, with the assumption that they will be ordered 'inout vdd1, inout gnd1, inout vdd2, inout gnd2, ...'. |
### Placement
| Variable | Description |
|-----|-----|
| 'PL_TARGET_DENSITY' | The desired placement density of cells. It reflects how spread the cells would be on the core area. 1 = closely dense. 0 = widely spread <br> (Default: '0.55') |
| 'PL_TIME_DRIVEN' | Specifies whether the placer should use time driven placement. 0 = false, 1 = true <br> (Default: '0') |
| 'PL_DRIVEN' | Specifies the library for time driven placement <br> (Default: 'LIB_TYPICAL') |
| 'PL_BASIC_PLACEMENT' | Specifies whether the placer should run basic placement or not (by running initial placement, increasing the minimum overflow to 0.9, and limiting the number of iterations to 20). 0 = false, 1 = true <br> (Default: '0') |
| 'PL_SKIP_INITIAL_PLACEMENT' | Specifies whether the placer should run initial placement or not. 0 = false, 1 = true <br> (Default: '0') |
| 'PL_RANDOM_GLB_PLACEMENT' | Specifies whether the placer should run random placement or not. This is useful if the design is tiny (less than 100 cells). 0 = false, 1 = true <br> (Default: '0') |
| 'PL_REPLACE_INITIAL_PLACEMENT' | Specifies whether the placer should run random placement or not followed by replace's initial placement. This is useful if the design is tiny (less than 100 cells). 0 = false, 1 = true <br> (Default: '0') |
| 'PL_ROUTABILITY_DRIVEN' | Specifies whether the placer should use routability driven placement. 0 = false, 1 = true <br> (Default: '0') |
| 'PL_OPENPHYSYN_OPTIMIZATIONS' | Specifies whether OpenPhysyn should be used to perform timing optimizations or not. 0 = false, 1 = true <br> (Default: '0') |
| 'PSN_ENABLE_RESIZING' | Enables driver resizing by OpenPhysyn. 0 = Disabled, 1 = Enabled <br> (Default: '1') |
| 'PSN_ENABLE_PIN_SWAP' | Enables pin swapping for timing optimization by OpenPhysyn. 0 = Disabled, 1 = Enabled <br> (Default: '1') |
| 'PL_RESIZER_TIMING_OPTIMIZATIONS' | Specifies whether resizer timing optimizations should be performed or not. 0 = false, 1 = true <br> (Default: '1') |
| 'PL_RESIZER_MAX_WIRE_LENGTH' | specifies the maximum wire length cap used by resizer to insert buffers. If set to 0, no buffers will be inserted. Value in microns. <br> (Default: '0') |
| 'LIB_OPT' | Points to the lib file, corresponding to the slowest corner, for max delay calculation during OpenPhysyn optimizations. This is usually a trimmed version of 'LIB_SLOWEST'. <br> (Default: '$env(TMP_DIR)/opt.lib' ) |
| 'LIB_SLOWEST' | Points to the lib file, corresponding to the slowest corner, for max delay calculation during resizer optimizations. This is copy of 'LIB_SLOWEST'. <br> (Default: '$env(TMP_DIR)/resizer.lib' ) |
| 'DONT_USE_CELLS' | The list of cells to not use during resizer optimizations. <br> (Default: the contents of 'DRC_EXCLUDE_CELL_LIST' .) |
| 'PL_ESTIMATE_PARASITICS' | Specifies whether or not to run STA after global placement using OpenROAD's estimate_parasitics -placement and generates reports under 'logs/placement'. 1 = Enabled, 0 = Disabled. <br> (Default: '1') |
| 'PL_DIAMOND_SEARCH_HEIGHT' | Specifies the diamond search height used for legalizing the cells during detailed placement. The search width is calculated internally as 'Height * 2'. Design that contain big macros, increasing this value to above 400 will allow for more search space and more potential for successful legalization. <br> (Default: '100') |
| 'PL_OPTIMIZE_MIRRORING' | Specifies whether or not to run an optimize_mirroring pass whenever detailed placement happens. This pass will mirror the cells whenever possible to optimize the design. 1 = Enabled, 0 = Disabled. <br> (Default: '1') |
| 'PL_RESIZER_BUFFER_INPUT_PORTS' | Specifies whether or not to insert buffers on input ports whenever resizer optimizations are run. For this to be used, 'PL_RESIZER_DESIGN_OPTIMIZATIONS' must be set to 1. 1 = Enabled, 0 = Disabled. <br> (Default: '1') |
| 'PL_RESIZER_BUFFER_OUTPUT_PORTS' | Specifies whether or not to insert buffers on output ports whenever resizer optimizations are run. For this to be used, 'PL_RESIZER_DESIGN_OPTIMIZATIONS' must be set to 1. 1 = Enabled, 0 = Disabled. <br> (Default: '1') |
### CTS
:

```

The floorplan.tcl contains its default parameters

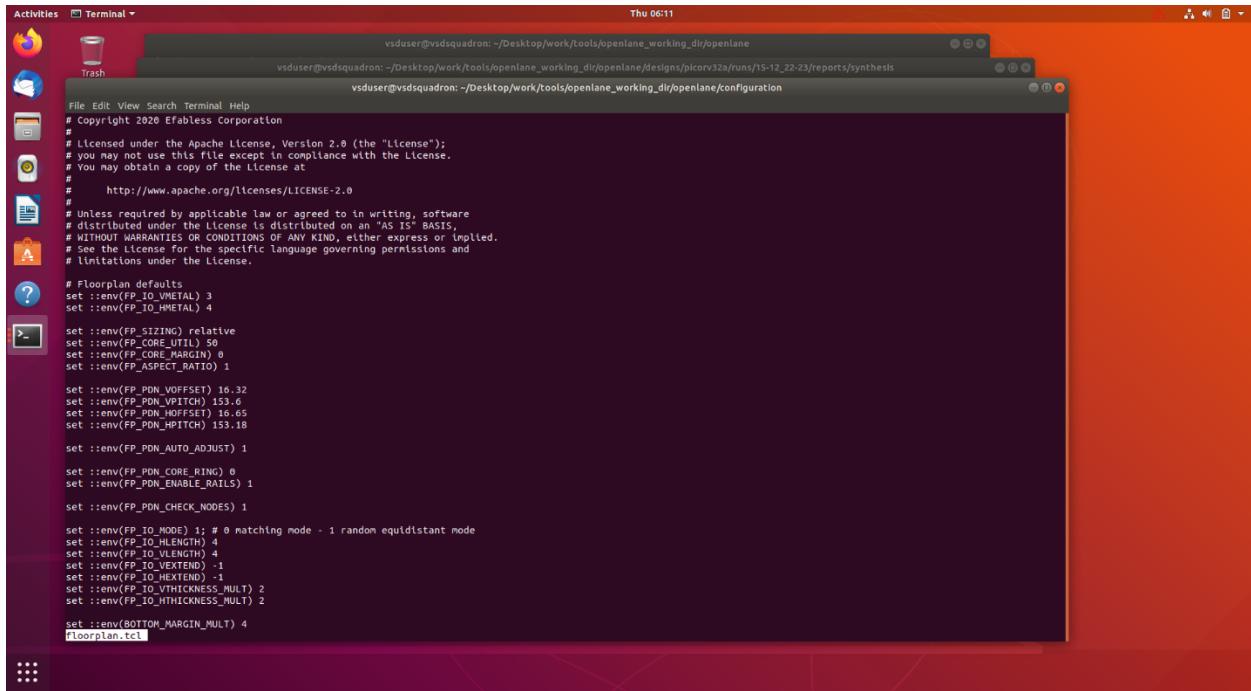
```

Thu 06:11
vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/15-12-22-23/reports/synthesis
vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/configuration

File Edit View Search Terminal Help
vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/15-12-22-23/reports/synthesis
vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/configuration

vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane$ cd openlane_working_dir
vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane$ ls -ltr
total 18
drwxr-xr-x  5 vsduser docker 4096 Jun 28 2021 pkts
drwxr-xr-x 10 vsduser docker 4096 Jun 29 2021 openlane_old
drwxr-xr-x 11 vsduser docker 4096 Oct 14 05:28 openlane
vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane$ cd openlane
vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane$ ls -ltr
total 18
drwxr-xr-x 15 vsduser docker 4096 Jun 29 2021 scripts
-rw-r--r--  1 vsduser docker 20787 Jun 29 2021 run_designs.py
drwxr-xr-x  1 vsduser docker 7898 Jun 29 2021 report_generation_wrapper.py
drwxr-xr-x  3 vsduser docker 4096 Jun 29 2021 regression_results
drwxr-xr-x  1 vsduser docker 2593 Jun 29 2021 results
drwxr-xr-x  1 vsduser docker 7273 Jun 29 2021 Rakefile
-rw-r--r--  1 vsduser docker 11350 Jun 29 2021 LICENSE
-rw-r--r--  1 vsduser docker 6519 Jun 29 2021 flow.tcl
drwxr-xr-x  5 vsduser docker 4096 Jun 29 2021 docs
drwxr-xr-x  5 vsduser docker 4096 Jun 29 2021 docker_build
drwxr-xr-x 40 vsduser docker 4096 Jun 29 2021 docker
drwxr-xr-x  1 vsduser docker 1285 Jun 29 2021 CONTRIBUTING.md
-rw-r--r--  1 vsduser docker 5514 Jun 29 2021 config.py
drwxr-xr-x  2 vsduser docker 4096 Jun 29 2021 configuration
-rwrxr-x  1 vsduser docker 966 Jun 29 2021 clean_runs.tcl
-rw-r--r--  1 vsduser docker 799 Jun 29 2021 AUTHORS.md
-rw-r--r--  1 vsduser docker 590 Jun 29 2021 default.cvcrc
drwxrwxr-x  0 vsduser docker 4096 Oct 14 05:37 metadata/design
vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane$ cd configurations
bash: cd: configurations: No such file or directory
vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane$ cd configurations
bash: cd: configurations: No such file or directory
vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane$ cd configuration
vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane$ cd configuration
vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane$ ls -ltr
total 64
-rwrxr-x  1 vsduser docker 1117 Jun 29 2021 synthesis.tcl
-rwrxr-x  1 vsduser docker 1897 Jun 29 2021 routing.tcl
-rw-r--r--  1 vsduser docker 31784 Jun 29 2021 README.md
-rw-r--r--  1 vsduser docker 1280 Jun 29 2021 placement.tcl
-rwrxr-x  1 vsduser docker 69 Jun 29 2021 vs.tcl
-rwrxr-x  1 vsduser docker 2358 Jun 29 2021 general.tcl
-rwrxr-x  1 vsduser docker 1527 Jun 29 2021 floorplan.tcl
-rwrxr-x  1 vsduser docker 809 Jun 29 2021 cts.tcl
-rwrxr-x  1 vsduser docker 1113 Jun 29 2021 checkers.tcl
vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/configuration$ less README.md
vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/configuration$ less floorplan.tcl

```



```

Activities Terminal Thu 06:11
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/15-12_22-23/reports/synthesis
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/configuration

File Edit View Search Terminal Help
# Copyright 2020 Efabless Corporation
#
# Licensed under the Apache License, Version 2.0 (the "License");
# you may not use this file except in compliance with the License.
# You may obtain a copy of the License at
#
#     http://www.apache.org/licenses/LICENSE-2.0
#
# Unless required by applicable law or agreed to in writing, software
# distributed under the License is distributed on an "AS IS" BASIS,
# WITHOUT WARRANTIES OR CONDITIONS OF ANY KIND, either express or implied.
# See the License for the specific language governing permissions and
# limitations under the License.

# Floorplan defaults
set ::env(FP_IO_VMETAL) 3
set ::env(FP_IO_HMETAL) 4

set ::env(FP_SIZEINO) relative
set ::env(FP_CORE_UTIL) 50
set ::env(FP_CORE_MARGIN) 0
set ::env(FP_ASPECT_RATIO) 1

set ::env(FP_PDN_VOFFSET) 16.32
set ::env(FP_PDN_VPITCH) 153.6
set ::env(FP_PDN_HOFFSET) 16.65
set ::env(FP_PDN_HPITCH) 153.18

set ::env(FP_PDN_AUTO_ADJUST) 1

set ::env(FP_PDN_CORE_RING) 0
set ::env(FP_PDN_ENABLE_RAILS) 1

set ::env(FP_PDN_CHECK_NODES) 1

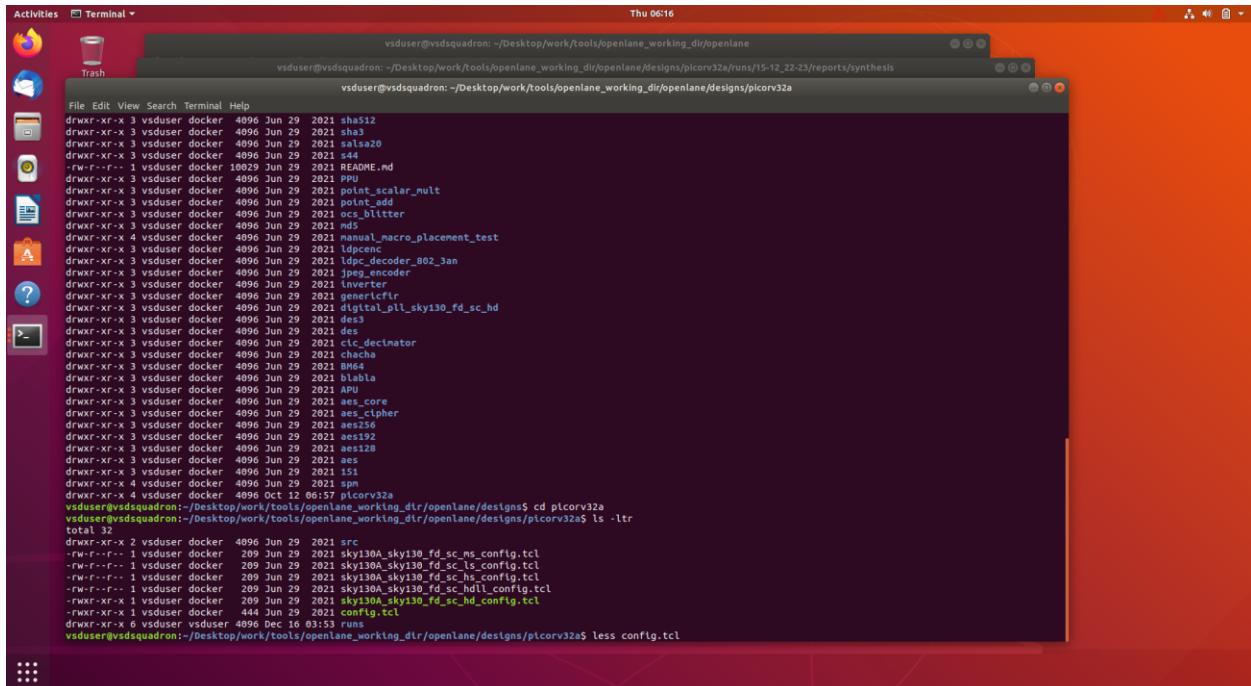
set ::env(FP_IO_MODE) 1; # 0 matching mode - 1 random equidistant mode
set ::env(FP_IO_HLENGTH) 4
set ::env(FP_IO_VLENGTH) 4
set ::env(FP_IO_VEXTEND) -1
set ::env(FP_IO_HEXTEND) 1
set ::env(FP_IO_VTHICKNESS_MULT) 2
set ::env(FP_IO_HTHICKNESS_MULT) 2

set ::env(BOTTOM_MARGIN_MULT) 4
floorplan.tcl

```

But the priority of setting is different. This is of the least priority.

The highest priority goes to the sky130A.....tcl followed by the config.tcl in the picorv32a directory.

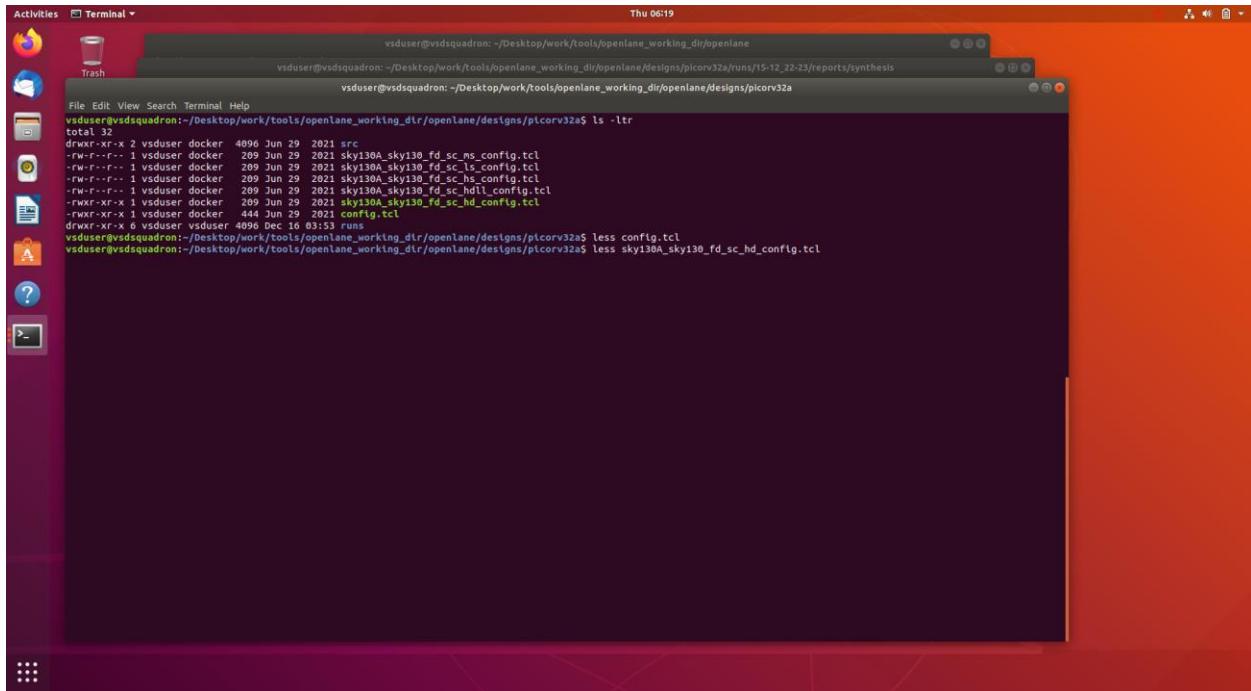


```

Activities Terminal Thu 06:16
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/15-12_22-23/reports/synthesis
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a

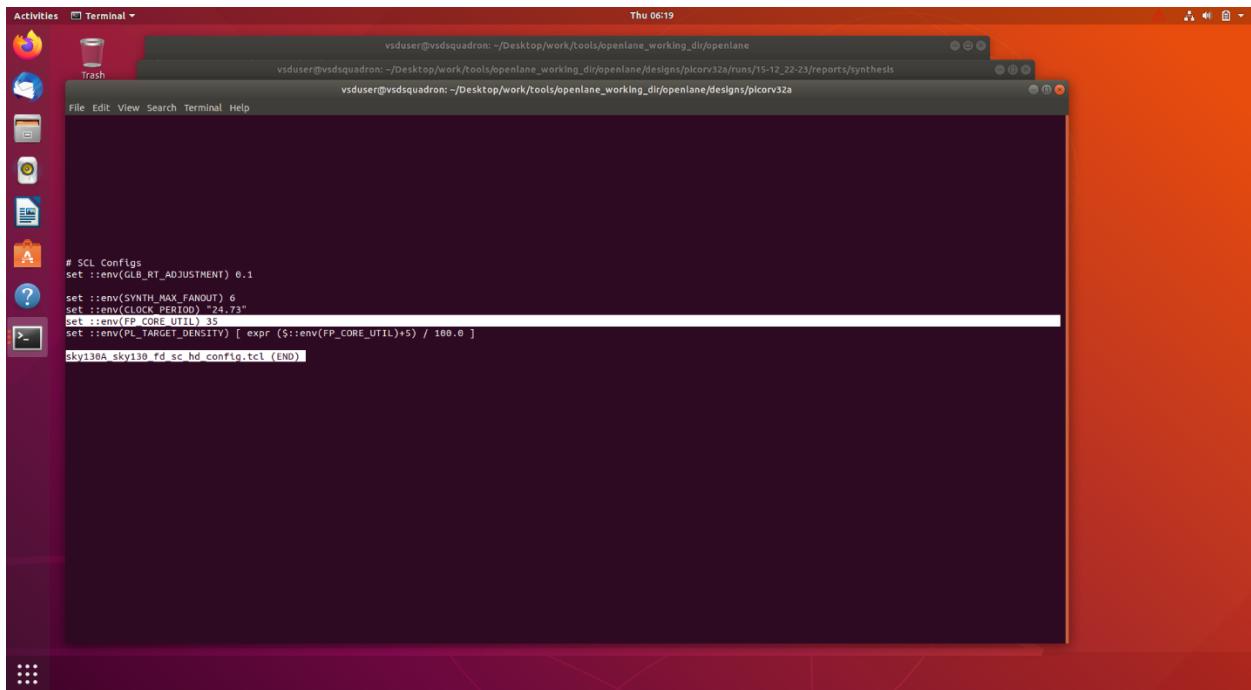
File Edit View Search Terminal Help
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 sha512
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 sha3
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 sha256
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 sha224
drwxr-xr-x 1 vsduser docker 10209 Jun 29 2021 README.md
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 PPUs
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 point_scalar_mult
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 point_add
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 oct_bititer
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 oct256s
drwxr-xr-x 4 vsduser docker 4096 Jun 29 2021 manual_macro_placement_test
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 ldpcenc
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 ldpc_decoder_802_3an
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 jpeg_encoder
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 inverter
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 nandcfir
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 digital_pll_sky130_fd_sc_hd
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 des3
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 des
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 cic_deictator
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 chacha
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 aes
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 blabla
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 APUs
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 aes_core
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 aes_cipher
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 aes_ecb
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 aes192
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 aes128
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 aes
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 i51
drwxr-xr-x 4 vsduser docker 4096 Jun 29 2021 spn
drwxr-xr-x 3 vsduser docker 4096 Oct 16 06:57 picorv32a
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a$ cd picorv32a
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a$ ls -ltr
total 32
drwxr-xr-x 2 vsduser docker 4096 Jun 29 2021 src
-rw-r--r-- 1 vsduser docker 209 Jun 29 2021 sky130_fd_sc_m5_config.tcl
-rw-r--r-- 1 vsduser docker 209 Jun 29 2021 sky130_fd_sc_hd_m5_config.tcl
-rw-r--r-- 1 vsduser docker 209 Jun 29 2021 sky130_fd_sc_hd_config.tcl
-rw-r--r-- 1 vsduser docker 209 Jun 29 2021 sky130_fd_sc_hd_hd_config.tcl
-rw-r--r-- 1 vsduser docker 209 Jun 29 2021 sky130_fd_sc_hd_hd_config.tcl
-rw-r--r-- 1 vsduser docker 444 Jun 29 2021 config.tcl
drwxr-xr-x 6 vsduser vsduser 4096 Dec 16 03:53 runs
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a$ less config.tcl

```



A screenshot of an Ubuntu desktop environment. A terminal window is open in the foreground, showing command-line output. The terminal title is "vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane". The command run is "ls -ltr", which lists several files in the directory, including "sky130_fd_sc_ms_config.tcl", "sky130_fd_sc_hd_config.tcl", and "sky130_fd_sc_hd_ll_config.tcl". The terminal window has a dark background and light-colored text. The desktop background is orange.

The core utilization is 35% over here



A screenshot of an Ubuntu desktop environment. A terminal window is open in the foreground, showing command-line output. The terminal title is "vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane". The command run is "less config.tcl", which displays a configuration script. The script includes commands like "set ::env(GLB_RT_ADJUSTMENT) 0.1", "set ::env(SYNTH_MAX_FANOUT) 6", "set ::env(CLOCK_PERIOD) "24.73\"", "set ::env(FP_CORE_UTIL) 35", and "set ::env(PL_TARGET_DENSITY) [expr { \$::env(FP_CORE_UTIL)*5 } / 100.0]". The terminal window has a dark background and light-colored text. The desktop background is orange.

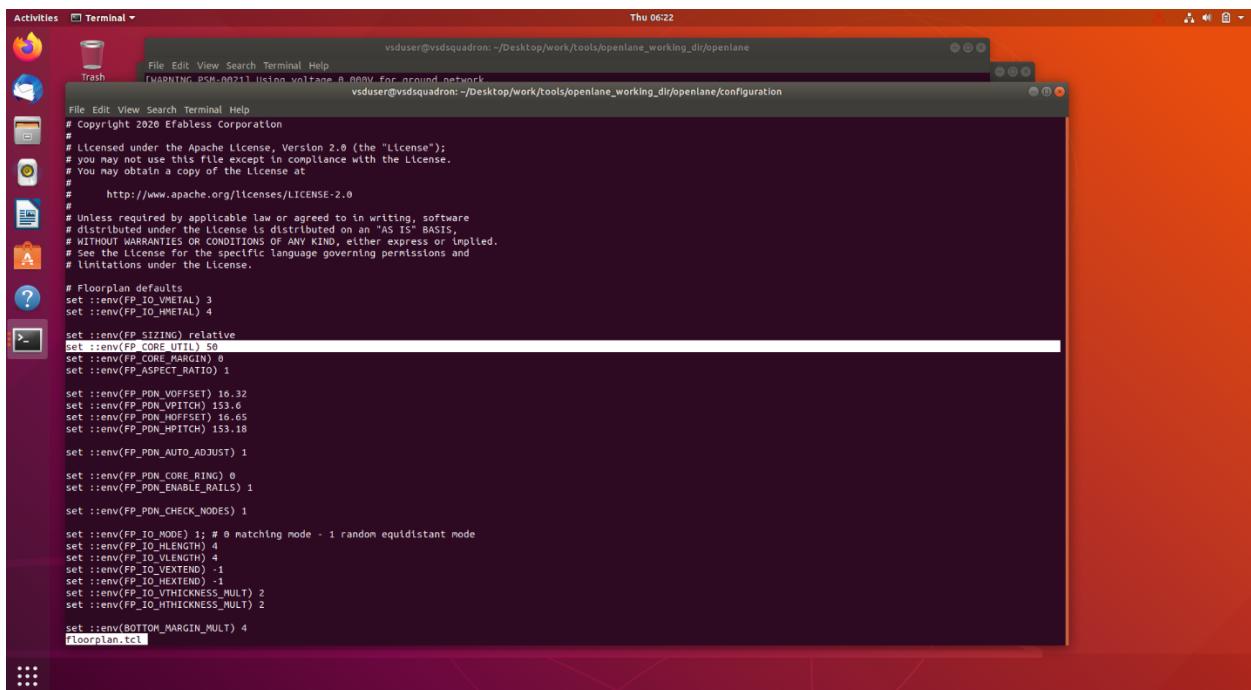
Let's compare it with what's default in the floorplan

```
Activities Terminal Thu 06:22
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane
WARNING_PSM-00211 Using voltage 0.000V for ground network

File Edit View Search Terminal Help
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/configuration

File Edit View Search Terminal Help
total 32
drwxr-xr-x 2 vsduser docker 4096 Jun 29 2021 src
-rw-r--r-- 1 vsduser docker 209 Jun 29 2021 sky130A_sky130_fd_sc_ms_config.tcl
-rw-r--r-- 1 vsduser docker 208 Jun 29 2021 sky130A_sky130_fd_sc_ls_config.tcl
-rw-r--r-- 1 vsduser docker 209 Jun 29 2021 sky130A_sky130_fd_sc_hd_config.tcl
-rw-r--r-- 1 vsduser docker 209 Jun 29 2021 sky130A_sky130_fd_sc_ll_config.tcl
-rw-r--r-- 1 vsduser docker 209 Jun 29 2021 sky130A_sky130_fd_sc_hd_config.tcl
-rw-r--r-- 1 vsduser docker 444 Jun 29 2021 config.tcl
drwxr-xr-x 6 vsduser vsduser 4096 Dec 16 03:53 runs
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/pkcorr32a less config.tcl
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/pkcorr32a less sky130A_sky130_fd_sc_hd_config.tcl
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/pkcorr32a cd ../..
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ ls -ltr
total 140
drwxr-xr-x 15 vsduser docker 4096 Jun 29 2021 scripts
-rw-r--r-- 1 vsduser docker 20787 Jun 29 2021 run_designs.py
-rw-r--r-- 1 vsduser docker 7898 Jun 29 2021 report_generation_wrapper.py
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 simulation_results
drwxr-xr-x 2 vsduser docker 25589 Jun 29 2021 README.md
-rw-r--r-- 1 vsduser docker 7273 Jun 29 2021 Makefile
-rw-r--r-- 1 vsduser docker 11350 Jun 29 2021 LICENSE
-rw-r--r-- 1 vsduser docker 6519 Jun 29 2021 flow.tcl
drwxr-xr-x 5 vsduser docker 4096 Jun 29 2021 docs
drwxr-xr-x 5 vsduser docker 4096 Jun 29 2021 docker_build
drwxr-xr-x 2 vsduser docker 4096 Jun 29 2021 docker_actions
-rw-r--r-- 1 vsduser docker 1285 Jun 29 2021 CONTRIBUTING.md
-rw-r--r-- 1 vsduser docker 5514 Jun 29 2021 conf.py
drwxr-xr-x 2 vsduser docker 4096 Jun 29 2021 configuration
-rw-r--r-- 1 vsduser docker 966 Jun 29 2021 clean_runs.tcl
-rw-r--r-- 1 vsduser docker 709 Jun 29 2021 AUTHORS.md
-rw-r--r-- 1 vsduser docker 960 Jun 29 2021 default.tcl
drwxr-xr-x 6 vsduser vsduser 4096 Oct 14 05:37 netstdtcldesign
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ cd configuration
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/configuration$ ls -ltr
total 64
-rwkr-xr-x 1 vsduser docker 1117 Jun 29 2021 synthesis.tcl
-rwkr-xr-x 1 vsduser docker 1897 Jun 29 2021 routing.tcl
-rwkr-xr-x 1 vsduser docker 3764 Jun 29 2021 placement.tcl
-rwkr-xr-x 1 vsduser docker 1288 Jun 29 2021 lvs.tcl
-rwkr-xr-x 1 vsduser docker 69 Jun 29 2021 general.tcl
-rwkr-xr-x 1 vsduser docker 2358 Jun 29 2021 floorplan.tcl
-rwkr-xr-x 1 vsduser docker 1527 Jun 29 2021 cts.tcl
-rwkr-xr-x 1 vsduser docker 808 Jun 29 2021 checkers.tcl
-rwkr-xr-x 1 vsduser docker 1113 Jun 29 2021 floorplan.tcl
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/configuration$ less floorplan.tcl
```

50%.



The screenshot shows a Linux desktop environment with a terminal window open. The terminal window title is "vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane". The terminal content displays a TCL script named "floorplan.tcl". The script is a configuration file for the OpenLane floorplanning tool, setting various parameters for a floorplan. Key settings include:

- Processor placement: Set to relative (set ::env(FP_IO_VMETAL) 3; set ::env(FP_IO_HMETAL) 4).
- Processor margins: Set to 0 (set ::env(FP_CORE_MARGIN) 0).
- Processor aspect ratio: Set to 1 (set ::env(FP_ASPECT_RATIO) 1).
- Processor dimensions: Set to 16.32x153.6 (set ::env(FP_PDN_WOFSET) 16.32; set ::env(FP_PDN_VPTCH) 153.6).
- Processor offsets: Set to 16.65x153.18 (set ::env(FP_PDN_HOFFSET) 16.65; set ::env(FP_PDN_RPTCH) 153.18).
- Processor auto-adjust: Set to 1 (set ::env(FP_PDN_AUTO_ADJUST) 1).
- Processor core ring: Set to 0 (set ::env(FP_PDN_CORE_RING) 0).
- Processor enable rails: Set to 1 (set ::env(FP_PDN_ENABLE_RAILS) 1).
- Processor check nodes: Set to 1 (set ::env(FP_PDN_CHECK_NODES) 1).
- Processor IO mode: Set to random equidistant mode (set ::env(FP_IO_MODE) 1; # matching mode - 1 random equidistant mode).
- Processor IO length: Set to 4 (set ::env(FP_IO_LENGTH) 4).
- Processor IO vertical width: Set to 4 (set ::env(FP_IO_VLENGTH) 4).
- Processor IO hex extend: Set to 1 (set ::env(FP_IO_HEXTEND) 1).
- Processor IO hex thickness: Set to 2 (set ::env(FP_IO_HTHICKNESS_MULT) 2).
- Processor IO multi thickness: Set to 2 (set ::env(FP_IO_MTHICKNESS_MULT) 2).

The script concludes with the command "floorplan.tcl".

The highest directory gets priority (35%)

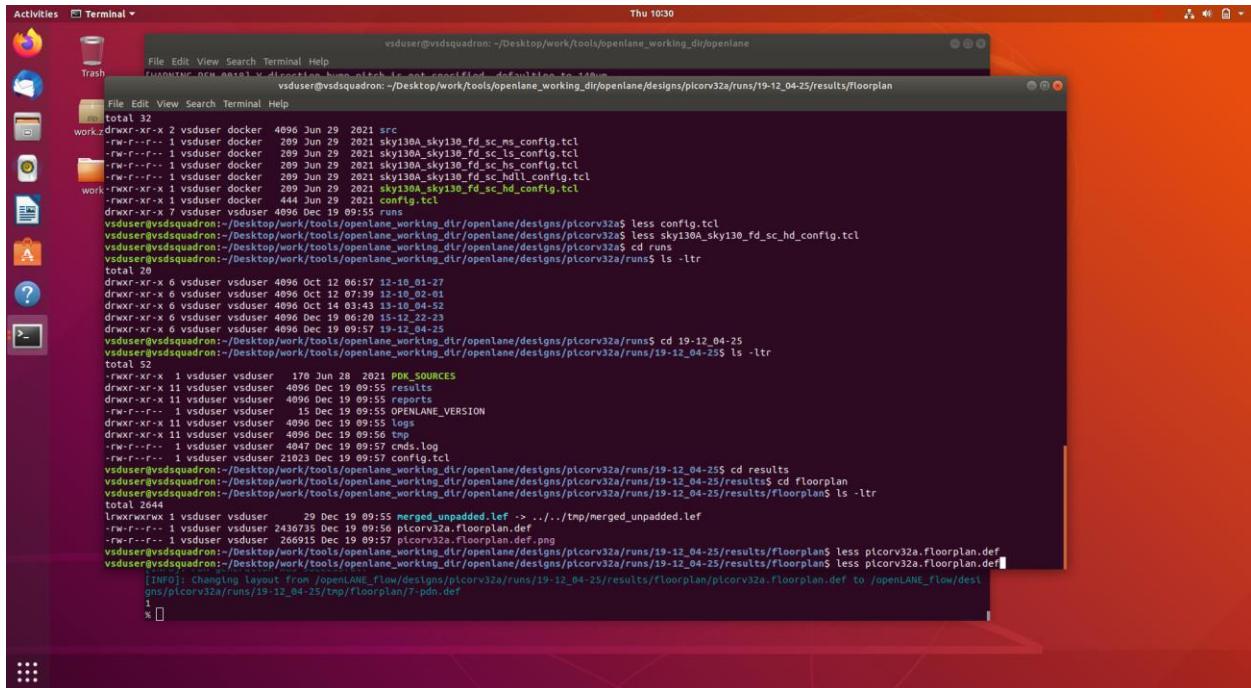
Note: In openlane flow the horizontal and vertical metals are one value more than specified (i.e 3 becomes 4)

To run the floorplan step the command is `run_floorplan`

```
Activities Terminal Thu 06:19
vsduser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Warnings: 307 unique messages, 307 total
End of script. Logfile hash: 3974efb082 CPU: user 16.51s system 1.03s, MEM: 96.50 MB peak
vsduser@vdsd4:~$ make synth_57x_2x abc (21 sec), 11x 33x opt_expr (4 sec), ...
total: 32
[INFO]: Changing netlist from .tcl to ./openlane_tcl/designs/picorv32a/runs/15-12_22-23/results/synths/picorv32a.synthesis.v
drwxr-xr-x 2 vsduser 1000 8.0K Jan 15 06:19 .
drwxr-xr-x 1 vsduser 1000 4.0K Jan 15 06:19 ..
[INFO]: current step index: 2
[INFO]: current step index: 3
[INFO]: current step index: 4
[INFO]: current step index: 5
[INFO]: current step index: 6
[INFO]: current step index: 7
[INFO]: current step index: 8
[INFO]: current step index: 9
[INFO]: current step index: 10
[INFO]: current step index: 11
[INFO]: current step index: 12
[INFO]: current step index: 13
[INFO]: current step index: 14
[INFO]: current step index: 15
[INFO]: current step index: 16
[INFO]: current step index: 17
[INFO]: current step index: 18
[INFO]: current step index: 19
[INFO]: current step index: 20
[INFO]: current step index: 21
[INFO]: current step index: 22
[INFO]: current step index: 23
[INFO]: current step index: 24
[INFO]: current step index: 25
[INFO]: current step index: 26
[INFO]: current step index: 27
[INFO]: current step index: 28
[INFO]: current step index: 29
[INFO]: current step index: 30
[INFO]: current step index: 31
[INFO]: default_operating_condition ff_1w0c_iv95 not found.
vsduser@vdsd4:~$ Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.ref/sky130_fd_sc_hd/lb/sky130_fd_sc_hd_ss_n40C_iv95.lib line
31, default_operating_condition ff_1w0c_iv95 not found.
vsduser@vdsd4:~$ Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.ref/sky130_fd_sc_hd/lb/sky130_fd_sc_hd_ss_100C_iv95.lib line
32, default_operating_condition ff_100C_iv95 not found.
[INFO]: create_clock [get_ports S::env(CLOCK_PORT)]: -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(ID_PCT)]
puts "[INFO]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 0.0000000000000001
[INFO]: Setting input delay to: 0.0000000000000001
[INFO]: Setting output delay to: 0.0000000000000001
[INFO]: Setting input delay to: 0.0000000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_idxn [lsearch [all_inputs] [get_port S::env(CLOCK_PORT)]]
#set rst_lndx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_lndx $clk_lndx]
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_lndx $rst_lndx]
set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_lndx $rst_lndx]
# correct resets
set_input_delay $input_delay_value -clock [get_clocks S::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks S::env(CLOCK_PORT)] [resetn]
set_output_delay $output_delay_value -clock [get_clocks S::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_up_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "[INFO]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -759.46
wns -24.89
[INFO]: synthesis was successful
% run_floorplan
```

Floorplan completed successfully

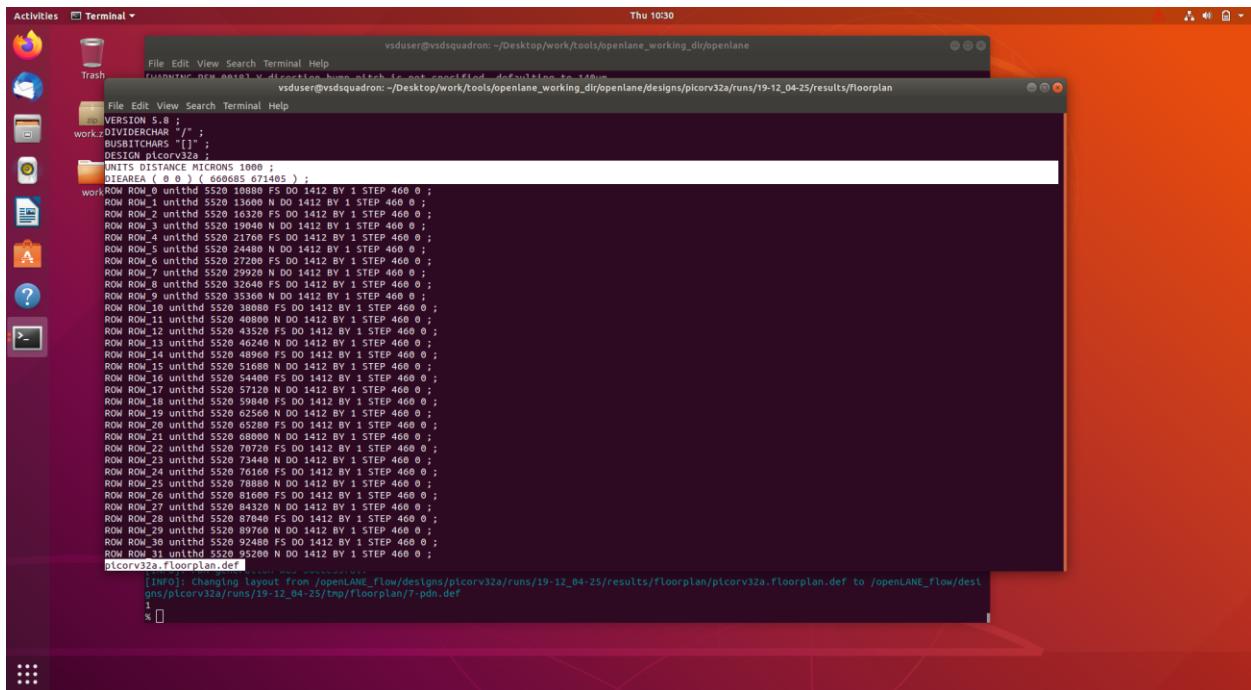
After running floorplan we check the design exchange file (def)



```

Thu 10:30
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/19-12_04-25/results/floorplan

total 32
work_zdrwxr-Xr-x 2 vsduser docker 4096 Jun 29 2021 SRC
... (output continues)
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/19-12_04-25/results/floorplan
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a less config.tcl
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a less sky130A_sky130_fd_sc_ls_config.tcl
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a less sky130A_sky130_fd_sc_hs_config.tcl
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a less sky130A_sky130_fd_sc_hdll_config.tcl
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a less sky130A_sky130_fd_sc_hd_config.tcl
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a less sky130A_sky130_fd_sc_hd_config.tcl
Drwxr-xr-x 6 vsduser vsduser 4096 Oct 12 06:57 12-10_01-27
drwxr-xr-x 6 vsduser vsduser 4096 Oct 12 07:39 12-10_02-01
drwxr-xr-x 6 vsduser vsduser 4096 Oct 14 03:43 13-10_04-52
drwxr-xr-x 6 vsduser vsduser 4096 Dec 19 06:20 15-12_22-23
drwxr-xr-x 6 vsduser vsduser 4096 Dec 19 09:57 19-12_04-25
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$ cd 19-12_04-25
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$ ls -ltr
total 52
... (output continues)
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$ cd results
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$ cd picorv32a_floorplan.def
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$ ls
total 2044
lwxrwxrwx 1 vsduser vsduser 29 Dec 19 09:55 merged_unpadded.lef -> ../../tmp/merged_unpadded.lef
-rw-r--r-- 1 vsduser vsduser 2436735 Dec 19 09:55 picorv32a.floorplan.def
-rw-r--r-- 1 vsduser vsduser 266915 Dec 19 09:57 picorv32a.floorplan.def.png
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$ cd 19-12_04-25/results
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$ ls
total 2044
lwxrwxrwx 1 vsduser vsduser 29 Dec 19 09:55 merged_unpadded.lef -> ../../tmp/merged_unpadded.lef
-rw-r--r-- 1 vsduser vsduser 2436735 Dec 19 09:55 picorv32a.floorplan.def
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$ less picorv32a.floorplan.def
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$ less picorv32a.floorplan.def
[INFO]: changing layout from /openLANE_flow/designs/picorv32a/runs/19-12_04-25/tmp/floorplan/7-pdn.def
[INFO]: changing layout from /openLANE_flow/designs/picorv32a/runs/19-12_04-25/tmp/floorplan/7-pdn.def
% 
```



```

Thu 10:30
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/19-12_04-25/results/floorplan

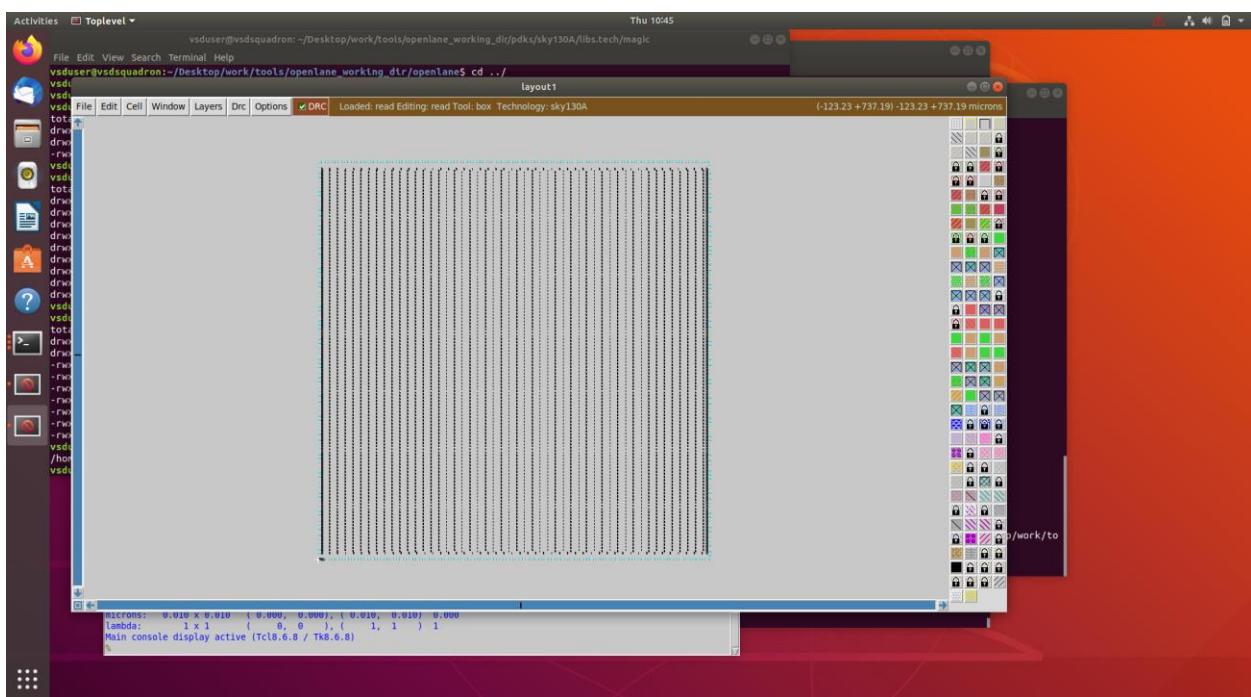
VERSION 5.0
work_DIVIDERCHAR '/';
DESIGN picorv32a ;
UNITS DISTANCE MICRONS 1000 ;
DIEAREA ( 0 0 ) ( 660685 671405 ) ;
ROW ROW 0 unithd 5520 35300 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW 1 unithd 5520 13600 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW 2 unithd 5520 16320 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW 3 unithd 5520 19640 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW 4 unithd 5520 21760 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW 5 unithd 5520 24480 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW 6 unithd 5520 27280 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW 7 unithd 5520 30080 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW 8 unithd 5520 32640 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW 9 unithd 5520 35300 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW 10 unithd 5520 38080 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW 11 unithd 5520 40800 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW 12 unithd 5520 43520 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW 13 unithd 5520 46240 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW 14 unithd 5520 49060 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW 15 unithd 5520 51680 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW 16 unithd 5520 54400 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW 17 unithd 5520 57120 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW 18 unithd 5520 60000 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW 19 unithd 5520 62560 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW 20 unithd 5520 65280 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW 21 unithd 5520 68000 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW 22 unithd 5520 70720 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW 23 unithd 5520 73440 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW 24 unithd 5520 76160 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW 25 unithd 5520 78880 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW 26 unithd 5520 81600 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW 27 unithd 5520 84320 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW 28 unithd 5520 87040 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW 29 unithd 5520 89760 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW 30 unithd 5520 92480 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW 31 unithd 5520 95200 N DO 1412 BY 1 STEP 460 0 ;
picorv32a.floorplan.def
[INFO]: changing layout from /openLANE_flow/designs/picorv32a/runs/19-12_04-25/tmp/floorplan/7-pdn.def
[INFO]: changing layout from /openLANE_flow/designs/picorv32a/runs/19-12_04-25/tmp/floorplan/7-pdn.def
1 
```

Here 1 micron is equal to 1000 database units. The lower numbers in the die area are the database units. When we divide those by 1000 we get the dimensions of the die in micrometers. (nearly 668um and 671um for the two ends).

To actually open the layout file we use the magic command

```

Activities Terminal Thu 10:43
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.tech/magic
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ cd ../
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ cd designs/picorv32a/runs/19-12_04-25/results/floorplan
total 12
drwxr-xr-- 1 vsduser docker 209 Jun 29 2021 sky130A_sky130_fd_sc_ms_config.tcl
drwxr-xr-- 1 vsduser docker 209 Jun 29 2021 sky130A_sky130_fd_sc_ls_config.tcl
drwxr-xr-- 1 vsduser docker 209 Jun 29 2021 sky130A_sky130_fd_sc_hd_config.tcl
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ less config.tcl
total 36
drwxr-xr-x 1 vsduser docker 209 Jun 29 2021 sky130A_sky130_fd_sc_hd_config.tcl
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ less sky130A_sky130_fd_sc_hd_config.tcl
total 20
drwxr-xr-x 7 vsduser vsduser 4096 Dec 19 09:55 runs
drwxr-xr-x 6 vsduser vsduser 4096 Oct 12 06:57 12-10_01-27
drwxr-xr-x 6 vsduser vsduser 4096 Oct 12 07:39 12-10_02-01
drwxr-xr-x 6 vsduser vsduser 4096 Oct 14 03:43 13-10_04-52
drwxr-xr-x 6 vsduser vsduser 4096 Dec 19 09:55 19-12_04-25
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ less config.tcl
total 400
drwxr-xr-x 6 vsduser vsduser 4096 Dec 19 09:55 runs
drwxr-xr-x 6 vsduser vsduser 4096 Oct 12 07:39 12-10_02-01
drwxr-xr-x 6 vsduser vsduser 4096 Oct 14 03:43 13-10_04-52
drwxr-xr-x 6 vsduser vsduser 4096 Dec 19 09:55 19-12_04-25
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ less sky130A_sky130_fd_sc_hd_config.tcl
total 52
drwxr-xr-x 1 vsduser vsduser 170 Jun 28 2021 PDK_SOURCES
drwxr-xr-x 1 vsduser vsduser 4096 Dec 19 09:55 runs
drwxr-xr-x 11 vsduser vsduser 4096 Dec 19 09:55 OPENLANE_VERSION
drwxr-xr-x 1 vsduser vsduser 15 Dec 19 09:55 OPENLANE_VERSION
drwxr-xr-x 11 vsduser vsduser 4096 Dec 19 09:55 logs
drwxr-xr-x 11 vsduser vsduser 4096 Dec 19 09:55 tmp
drwxr-xr-x 1 vsduser vsduser 4047 Dec 19 09:57 cmd.log
drwxr-xr-x 1 vsduser vsduser 2109 Dec 19 09:57 config.tcl
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ cd results
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ cd floorplan
/home/vsduser/vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ less picorv32a/runs/19-12_04-25/floorplan.def
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ ls -ltr
total 2644
lrwxrwxrwx 1 vsduser vsduser 29 Dec 19 09:55 merged_unpadded.lef > ../../tmp/merged_unpadded.lef
-rw-r--r-- 1 vsduser vsduser 2493782 Dec 19 09:55 picorv32a/runs/19-12_04-25/floorplan.def
-rw-r--r-- 1 vsduser vsduser 266915 Dec 19 09:57 picorv32a/runs/19-12_04-25/floorplan.def.png
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ designs/picorv32a/runs/19-12_04-25/results/floorplan less picorv32a.floorplan.def
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ designs/picorv32a/runs/19-12_04-25/results/floorplan less picorv32a.floorplan.def
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.tech/magic/sky130A.tech.lef read ../../tmp/merged.lef def read picorv32a.floorplan.def &
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/19-12_04-25/results/floorplan/picorv32a.floorplan.def to /openLANE_flow/designs/picorv32a/runs/19-12_04-25/tmp/floorplan7.pdn.def
1
%
```

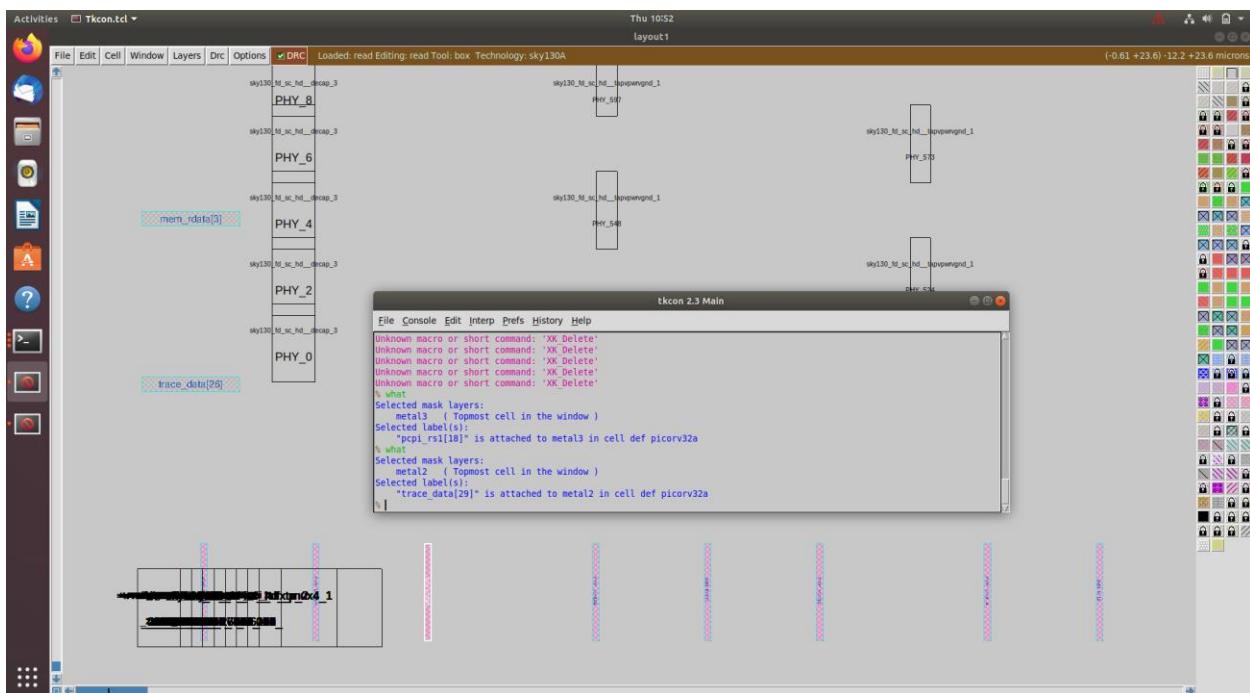
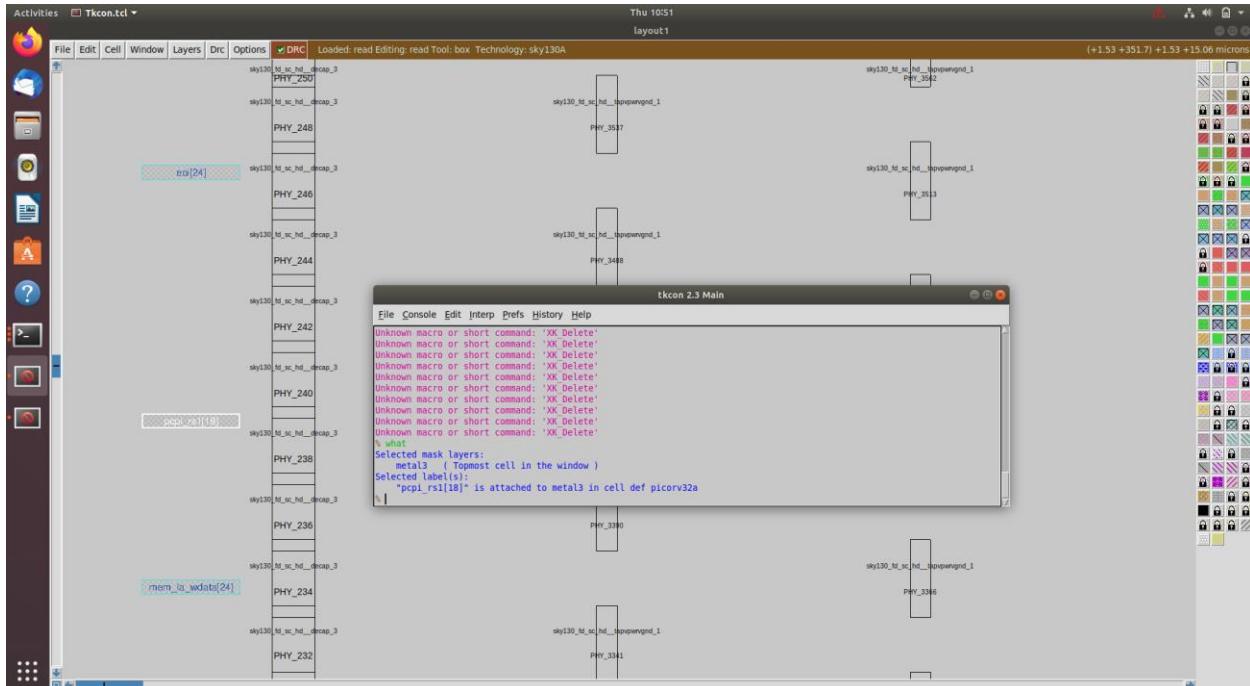


Some basic commands:

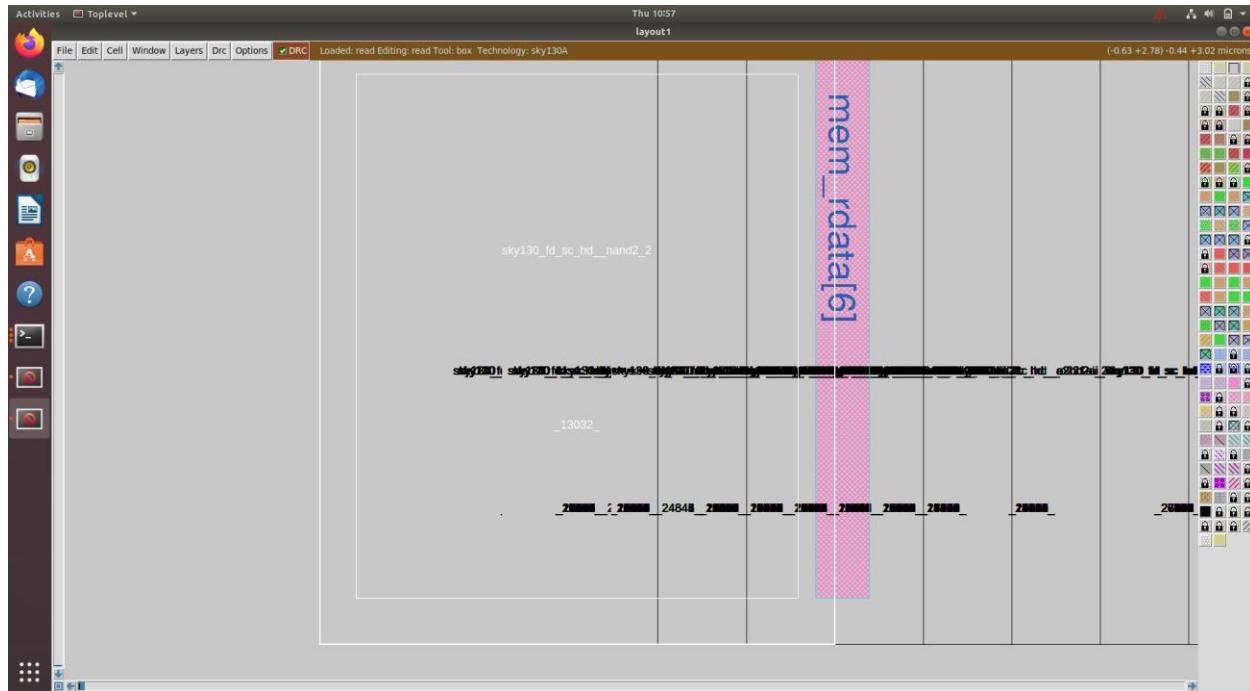
S and V to select and center align the design

Hover over the part and press S to select it.

In tkcon window do a ‘what’ to view its properties



The standard cells (Buffers, NAND, NOR) are present in the lower left corner of the design



After floorplanning, placement is carried out using run_placement

Placement completed successfully and its reports (HPWL – Half parameter wire length, OVFL – Overflow)

```
Activities Terminal Thu 23:54
vsduser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane

File Edit View Search Terminal Help
vsduser@vdsquadron:~/.vsduser$ Notice 0: Design: picrv32a
vsduser@vdsquadron:~/.vsduser$ Notice 0: Created 411 pins.
vsduser@vdsquadron:~/.vsduser$ Notice 0: Created 21699 components and 132072 component-terminals.
vsduser@vdsquadron:~/.vsduser$ Notice 0: Total 15447 nets and 65989 connections.
drwxr-xr-x 7 TW-r- Notice 0: Created 15447 nets and 56989 connections.
drwxr-xr-x 7 TW-r- Notice 0: Finished DEF file: /openLANE_flow/designs/picrv32a/runs/19-12_04-25/tmp/placement/B-resizer.def
-rw-r--r-- 1 TW-r- Notice 0: Design Stats
vsduser@vdsquadron:~/.vsduser$ drwxr-xr-x 21699-
vsduser@vdsquadron:~/.vsduser$ total 408
vsduser@vdsquadron:~/.vsduser$ drwxr-xr-x 0 0
vsduser@vdsquadron:~/.vsduser$ drwxr-xr-x 6354 0
vsduser@vdsquadron:~/.vsduser$ drwxr-xr-x 15449 0
vsduser@vdsquadron:~/.vsduser$ drwxr-xr-x 420473.3 u^2
vsduser@vdsquadron:~/.vsduser$ drwxr-xr-x 9141.3 u^2
vsduser@vdsquadron:~/.vsduser$ drwxr-xr-x 147800.5 u^2
vsduser@vdsquadron:~/.vsduser$ drwxr-xr-x 36 %
vsduser@vdsquadron:~/.vsduser$ drwxr-xr-x 53 %
vsduser@vdsquadron:~/.vsduser$ drwxr-xr-x 238
vsduser@vdsquadron:~/.vsduser$ drwxr-xr-x 2.7 u
vsduser@vdsquadron:~/.vsduser$ Vsduser
vsduser@vdsquadron:~/.vsduser$ Placement Analysis
vsduser@vdsquadron:~/.vsduser$ total 408
vsduser@vdsquadron:~/.vsduser$ drwxr-xr-x 0 0
vsduser@vdsquadron:~/.vsduser$ drwxr-xr-x 8.0 u
vsduser@vdsquadron:~/.vsduser$ drwxr-xr-x 0.0 u
vsduser@vdsquadron:~/.vsduser$ drwxr-xr-x 0.0 u
-rw-r--r-- 1 TW-r- original HPWL 766980.0 u
-rw-r--r-- 1 TW-r- legalized HPWL 779196.5 u
-rw-r--r-- 1 TW-r- delta HPWL 2 %
-rw-r--r-- 1 TW-r- layout 0.0 u
-rw-r--r-- 1 TW-r- Mirrored 6193 instances
-rw-r--r-- 1 TW-r- Notice [INFO DPL-0020] Mirrored 6193 instances
-rw-r--r-- 1 TW-r- Notice [INFO DPL-0021] HPWL before 779196.5 u
vsduser@vdsquadron:~/.vsduser$ [INFO DPL-0022] HPWL after 766980.0 u
/home/vsduser@vdsquadron:~/.vsduser$ [INFO DPL-0023] HPWL delta -1.7 %
vsduser@vdsquadron:~/.vsduser$ total [INFO] Changing layout from /openLANE_flow/designs/picrv32a/runs/19-12_04-25/tmp/placement/B-resizer.def to /openLANE_flow/designs/picrv32a/runs/19-12_04-25/results/placement/picrv32a.placement.def
-rw-r--r-- 1 [INFO] changing layout from /openLANE_flow/designs/picrv32a/runs/19-12_04-25/tmp/placement/picrv32a.placement.def to /openLANE_flow/designs/picrv32a/runs/19-12_04-25/results/placement/picrv32a.placement.def
vsduser@vdsquadron:~/.vsduser$ [INFO] Taking a Screenshot of the Layout Using Klayout...
vsduser@vdsquadron:~/.vsduser$ [INFO]0 current step index: 12
vsduser@vdsquadron:~/.vsduser$ Usine Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.tech/klayout/sky130.lyt
vsduser@vdsquadron:~/.vsduser$ Usine layout file: /openLANE_flow/designs/picrv32a/runs/19-12_04-25/results/placement/picrv32a.placement.def
vsduser@vdsquadron:~/.vsduser$ [INFO] Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.tech/klayout/sky130.lyt
vsduser@vdsquadron:~/.vsduser$ [INFO] Reading Layout file: /openLANE_flow/designs/picrv32a/runs/19-12_04-25/results/placement/picrv32a.placement.def
vsduser@vdsquadron:~/.vsduser$ [INFO] Writing out PNG screenshot '/openLANE_flow/designs/picrv32a/runs/19-12_04-25/results/placement/picrv32a.placement.def.png'
Done.
% [INFO] Screenshot taken.
%
```

We check the def file

```
Activities Terminal
vsduser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/tools/openlane_working_dir/openlane
vsduser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane
vsduser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/19-12_04-25/results/placement
vsduser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/19-12_04-25
vsduser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$ ls -ltr
total 12
drwxr-xr-x 6 vsduser vsduser 4096 Oct 12 06:57 12-10_01-27
drwxr-xr-x 6 vsduser vsduser 4096 Oct 12 07:39 12-10_02-01
drwxr-xr-x 6 vsduser vsduser 4096 Oct 12 07:43 11-12_01-52
drwxr-xr-x 6 vsduser vsduser 4096 Oct 12 07:43 11-12_02-22
total 36
drwxr-xr-x 6 vsduser vsduser 4096 Dec 19 23:52 19-12_04-25
drwxr-xr-x 6 vsduser vsduser 4096 Dec 19 23:52 19-12_04-25s
vsduser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$ cd 19-12_04-25
vsduser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/19-12_04-25s$ ls -ltr
total 56
drwxr-xr-x 1 vsduser vsduser 178 Jun 28 2021 PDF_SOURCES
drwxr-xr-x 1 vsduser vsduser 4096 Dec 19 23:52 results
drwxr-xr-x 11 vsduser vsduser 4096 Dec 19 09:55 reports
drwxr-xr-x 11 vsduser vsduser 15 Dec 19 09:55 OPENLANE_VERSION
drwxr-xr-x 11 vsduser vsduser 4096 Dec 19 23:52 tmp
drwxr-xr-x 11 vsduser vsduser 4096 Dec 19 23:52 logs
vsduser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/19-12_04-25s$ config.tcl
total 408
drwxr-xr-x 1 vsduser vsduser 2140 Dec 19 23:52 config.tcl
drwxr-xr-x 1 vsduser vsduser 4096 Dec 19 23:52 results
drwxr-xr-x 1 vsduser vsduser 4096 Dec 19 09:55 results
vsduser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/19-12_04-25s$ cd results
drwxr-xr-x 1 vsduser vsduser 4096 Dec 19 09:55 merged_unpadded.lef
drwxr-xr-x 1 vsduser vsduser 3164924 Dec 19 23:52 picorv32a.placement.def
drwxr-xr-x 1 vsduser vsduser 816328 Dec 19 23:52 picorv32a.placement.def.png
vsduser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/19-12_04-25$ cd placement
vsduser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/19-12_04-25$ ls -ltr
total 3892
lrwxrwxr-x 1 vsduser vsduser 29 Dec 19 09:55 merged_unpadded.lef -> ../../merged_unpadded.lef
-rw-r--r-- 1 vsduser vsduser 3164924 Dec 19 23:52 picorv32a.placement.def
-rw-r--r-- 1 vsduser vsduser 816328 Dec 19 23:52 picorv32a.placement.def.png
vsduser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/19-12_04-25$ results/placements
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/19-12_04-25/results/placement/picorv32a.placement.def.png'
Done
[INFO] Screenshot taken.
%
```

Magic command to view the placed cells

```
Activities Terminal Thu 23/57
vsduser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/19-12_04-25$ cd placement
vsduser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/19-12_04-25$ ls -l
total 20
drwxr-xr-x 6 vsduser vsduser 4096 Oct 12 06:57 12-10_01-27
drwxr-xr-x 6 vsduser vsduser 4096 Oct 12 07:39 12-10_02-01
drwxr-xr-x 6 vsduser vsduser 4096 Oct 12 07:40 12-10_03-01
drwxr-xr-x 6 vsduser vsduser 4096 Oct 12 07:41 12-10_04-01
drwxr-xr-x 6 vsduser vsduser 4096 Oct 12 07:42 12-10_05-01
drwxr-xr-x 6 vsduser vsduser 4096 Oct 12 07:43 12-10_06-01
drwxr-xr-x 6 vsduser vsduser 4096 Oct 12 07:44 12-10_07-01
drwxr-xr-x 6 vsduser vsduser 4096 Oct 12 07:45 12-10_08-01
drwxr-xr-x 6 vsduser vsduser 4096 Oct 12 07:46 12-10_09-01
drwxr-xr-x 6 vsduser vsduser 4096 Oct 12 07:47 12-10_10-01
drwxr-xr-x 6 vsduser vsduser 4096 Oct 12 07:48 12-10_11-01
drwxr-xr-x 6 vsduser vsduser 4096 Oct 12 07:49 12-10_12-01
drwxr-xr-x 6 vsduser vsduser 4096 Dec 19 23:52 19-12_04-25
total 56
vsduser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$ cd 19-12_04-25
vsduser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/19-12_04-25$ ls -ltr
drwxr-xr-x 1 vsduser vsduser 4096 Dec 19 23:52 .
drwxr-xr-x 1 vsduser vsduser 4096 Dec 19 23:52 ..
drwxr-xr-x 1 vsduser vsduser 4096 Dec 19 09:55 reports
drwxr-xr-x 1 vsduser vsduser 4096 Dec 19 09:55 OPENLANE_VERSION
drwxr-xr-x 11 vsduser vsduser 4096 Dec 19 23:52 tmp
drwxr-xr-x 11 vsduser vsduser 4096 Dec 19 23:52 logs
drwxr-xr-x 11 vsduser vsduser 4096 Dec 19 23:52 cmd.log
drwxr-xr-x 11 vsduser vsduser 4096 Dec 19 23:52 config.tcl
vsduser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$ cd results
vsduser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/19-12_04-25$ cd results
total 408
drwxr-xr-x 1 vsduser vsduser 4096 Dec 19 09:57 hash.cdt; results: No such file or directory
drwxr-xr-x 1 vsduser vsduser 4096 Dec 19 09:57 .
drwxr-xr-x 1 vsduser vsduser 4096 Dec 19 09:57 ..
drwxr-xr-x 1 vsduser vsduser 4096 Dec 19 09:57 merged_unpadded.lef
drwxr-xr-x 1 vsduser vsduser 4096 Dec 19 09:57 routing
drwxr-xr-x 1 vsduser vsduser 4096 Dec 19 09:57 magic
drwxr-xr-x 2 vsduser vsduser 4096 Dec 19 09:55 ts
drwxr-xr-x 2 vsduser vsduser 4096 Dec 19 09:55 klayout
drwxr-xr-x 2 vsduser vsduser 4096 Dec 19 09:55 cvc
drwxr-xr-x 2 vsduser vsduser 4096 Dec 19 09:55 cts
drwxr-xr-x 2 vsduser vsduser 4096 Dec 19 09:55 floorplan
drwxr-xr-x 2 vsduser vsduser 4096 Dec 19 09:55 placement
drwxr-xr-x 2 vsduser vsduser 4096 Dec 19 09:55 synthesis
drwxr-xr-x 2 vsduser vsduser 4096 Dec 19 09:55 timing
vsduser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/19-12_04-25$ cd placement
vsduser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/19-12_04-25$ ls -ltr
total 3892
lwrw-r--w- 1 vsduser vsduser 29 Dec 19 09:55 merged_unpadded.lef -> ../../tmp/merged_unpadded.lef
-rw-r--r-- 1 vsduser vsduser 3164924 Dec 19 23:52 picorv32a.placement.def
-rw-r--r-- 1 vsduser vsduser 816328 Dec 19 23:52 picorv32a.placement.def.png
vsduser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/19-12_04-25$ results/placement$ magic -T /home/vsduser/Desktop/work/tools/pdk/sky130A/tb/sky130A.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.placement.def &
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/19-12_04-25/results/placement/picorv32a.placement.def.png'
Done.
[INFO]: Screenshot taken.
%
```

Placement ensures that the standard cells (which were at the bottom left earlier) are placed in their rows without any DRC errors and without affecting the DECAPs.

