ASIC:	1	2	3	4	5	6	7	8
ch00	u19	u09	w14	w02	u29	u39	w26	w38
ch01	u17	u07	w16	w04	u27	u37	w28	w40
ch02	u15	u05	w18	w06	u25	u35	w30	w42
ch03	u13	u03	w20	w08	u23	u33	w32	w44
ch04	u11	u01	w22	w10	u21	u31	w34	w46
ch05	v19	v09	w24	w12	v29	v39	w36	w48
ch06	v17	v07	v12	v02	v27	v37	v22	v32
ch07	v15	v05	v14	v04	v25	v35	v24	v34
ch08	v13	v03	v16	v06	v23	v33	v26	v36
ch09	v11	v01	v18	v08	v21	v31	v28	v38
ch10	w23	w11	v20	v10	w35	w47	v30	v40
ch11	w21	w09	u12	u02	w33	w45	u22	u32
ch12	w19	w07	u14	u04	w31	w43	u24	u34
ch13	w17	w05	u16	u06	w29	w41	u26	u36
ch14	w15	w03	u18	u08	w27	w39	u28	u38
ch15	w13	w01	u20	u10	w25	w37	u30	u40

U layer, first half: conductor / chip / chan

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
2	4	2	4	2	4	2	4	2	4	1	3	1	3	1	3	1	3	1	3
4	11	3	12	2	13	1	14	0	15	4	11	3	12	2	13	1	14	0	15

U layer, second half: conductor / chip / chan

21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
5	7	5	7	5	7	5	7	5	7	6	8	6	8	6	8	6	8	6	8
4	11	3	12	2	13	1	14	0	15	4	11	3	12	2	13	1	14	0	15

V layer, first half: conductor / chip / chan

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
2	4	2	4	2	4	2	4	2	4	1	3	1	3	1	3	1	3	1	3
9	6	8	7	7	8	6	9	5	10	9	6	8	7	7	8	6	9	5	10

V layer, second half: conductor / chip / chan

21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
5	7	5	7	5	7	5	7	5	7	6	8	6	8	6	8	6	8	6	8
9	6	8	7	7	8	6	9	5	10	9	6	8	7	7	8	6	9	5	10

W layer, first half: conductor / chip / chan

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
2	4	2	4	2	4	2	4	2	4	2	4	1	3	1	3	1	3	1	3	1	3	1	3
15	0	14	1	13	2	12	3	11	4	10	5	15	0	14	1	13	2	12	3	11	4	10	5

W layer, second half: conductor / chip / chan

25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
5	7	5	7	5	7	5	7	5	7	5	7	6	8	6	8	6	8	6	8	6	8	6	8
15	0	14	1	13	2	12	3	11	4	10	5	15	0	14	1	13	2	12	3	11	4	10	5