Last Name:_____, First Initial:____

COP 4600 Operating Systems

Exam 1

5 October 2016

Instructions

1. Read all instructions. Failure to follow instructions will result in loss of points.
2. This is a closed-book examination.
3. You are permitted one 8.5 by 11 inch sheet of notes (both sides OK) that you have prepared.
4. You are permitted **45 minutes** to complete this examination.
5. **Do not start** the exam until the proctor has told you to start.
6. **Answer any two (2) questions, and no more**. All questions are of equal value.
7. **Leave sufficient room in the upper left-hand corner for the staple** and staple your answer sheets in the room you have left.
8. Put the **question number in the top center** of each answer page and label each part of the question answer.
9. Include your last name and page number in the upper right hand corner of each answer page.
10. Show your work.
11. Start the answer to each question on a **new page** (i.e., do **not** put the answer to more than one question on the same page).
12. Use exactly one page of paper (both sides is OK, or two pages front side only) to hold the answer to each question, and please write legibly.
13. Assemble your answers in **numerical order** of the questions when you submit them.
14. Print your family name and first initial in the upper right hand corner of this page, and complete the honor statement affirmation below.

Read and sign the following statement. This page **MUST** be attached to your examination answers and **MUST** be completed to obtain credit for this examination.

On my honor, I have neither given nor received unauthorized aid on this examination.

Signed _____

Printed Name: _____

UFID: _____-_____

1. Architectures
   a. How do pipelined architectures affect interrupt handling? Explain and compare to non-pipelined architectures.
   b. How does superscalar architecture affect interrupt handling? Explain and compare to pipelined architectures.
   c. How does use of cache memory benefit DMA I/O? Explain.
   d. How does use of cache memory benefit multicore systems? How does it complicate them?

2. Suppose that jobs a data processing center tend to behave in the following way. After some variable number of short CPU bursts lasting 0.5-50 ms, the job will enter a phase with long CPU bursts lasting 1-100 seconds, and thereafter alternate between some number of short bursts and number of long CPU bursts. The operators have no way of predicting how many short or long bursts there will be, and the numbers may change from one set of bursts to the next.
   a. If the primary goal is efficient use of resources (CPU, I/O, and RAM), what factors should the admission scheduler take into account, in what ways, and why?
   b. Continuing with (a), design a process scheduling policy that achieves efficiency. Explain your design choices and how they support efficiency.
   c. Now design a process scheduling policy that also satisfies users of interactive processes whose CPU bursts are no more than 1 ms during its I/O-bound phases and where response times must be no more than 100 ms during these phases (but which also may have CPU-intensive phases with much longer response times)? Explain how your policy satisfies this additional requirement without sacrificing too much efficiency.

3. Processes/Threads
   a. Which process state transitions cause the process scheduler to run when a non-preemptive scheduling policy is used? Explain. Assume there is always at least one ready process and that the memory scheduler is also in use.
   b. Answer (a) when the policy is pre-emptive.
   c. Suppose you are developing a multi-threaded program for deployment on a large number of widely varied hosts running various OS types and versions. What type of threads would be most desirable and why? Would your answer change if most of the hardware platforms had multiple cores, and the program you were developing would often be the only user program running much of the time? Justify your answer.

4. Synchronization
   a. Solve the following synchronization problem using semaphores or monitors to coordinate between the Clerk and the Detailer. A system has three kinds of processes: Clerk, Customer, and Detailer. The Clerks wait for a Customer to arrive (send a Rental Request message), and if a clean car is available, assign a car to the customer (car ID sent in a Rental Reply message). Customers drive their rental cars for some time, then request to return them by sending a Return Request message to the Detailers. Detailers wait for a Customer to return a car (send a Return Request message with the car ID), and reply to the Customer with a Return Receipt. The Detailer then cleans the car and refills the gas tank if necessary before a Clerk can rent it to another Customer. The Customer never accesses the shared variables used by the Clerk and the Detailer to keep track of which cars are rented or not and to whom, and whether or not an unrented car is clean and tanked up.
   b. State reasonable safety and liveness requirements for this system, and give an informal argument that your solution satisfies them.