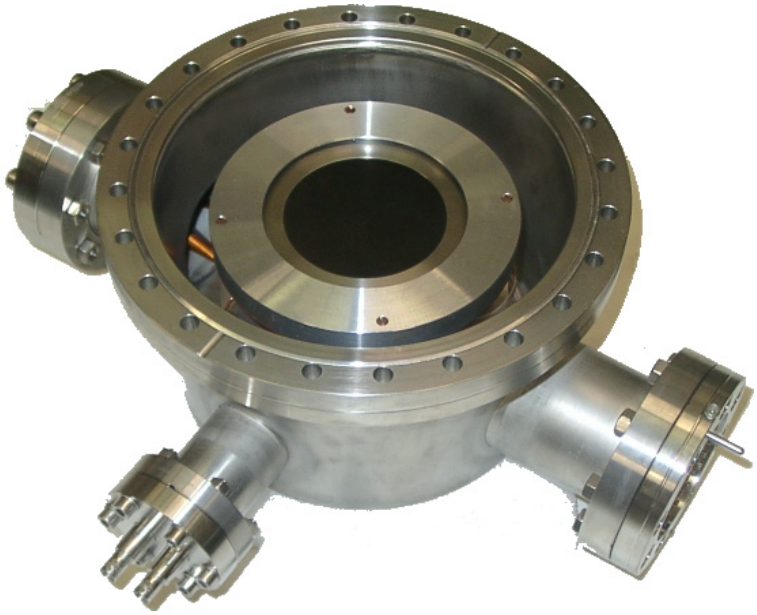
4-Quadrant Delayline Detector DLD 4040-4Q



Manual

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1 Table of Contents

2 Introduction

2.1 General Information

This manual is intended to assist users in the installation, operation and maintenance of the 4-Quadrant Delayline Detector DLD 4040-4Q. It is divided into 14 chapters. The chapter "Introduction" contains a brief description of the DLD. The chapter "Installation" refers to installation and cabling. One chapter describes the USB driver installation. Chapter "Principle of Operation" explains the theory of operation of the DLD. 3 chapters describe the technical details of the detector readout package and chapter "Operation of the DLD" describes the operation of the DLD. One further chapter describes the setup of the translation and rotation stage. The final chapters contain amongst others, technical details about the microchannel plates and the delayline detector in general.

2.2 Safety Instructions

Please read this manual carefully before performing any electrical or electronic operations and strictly follow the safety rules given within this manual.

The following symbols appear throughout the manual:

The "note symbol" marks text passages, which contain important information/ hints about the operation of the detector. Follow these information to ensure a proper functioning of the detector.

The "caution symbol" marks warnings, which are given to prevent an accidentally damaging of the detector or the readout system. Do NOT ignore these warnings and follow them strictly. Otherwise no guarantee is given for arose damages.

The "high voltage symbol" marks warnings, given in conjunction with the description of the operation/ use of high voltage supplies and/ or high voltage conducting parts.
Hazardous voltages are present, which can cause serious or fatal injuries. Therefore only persons with the appropriate training are allowed to carry out the installation, adjustment and repair work.

2.3 General Overview of the System

The Surface Concept delayline detectors are particularly developed for the needs of 1D(x), 2D(x,t), 2D(x,y) or 3D(x,y,t) area and time detection of electrons, ions, x-ray and UV-light as well as for multi hit detection of high rates with the 4-quadrant detector systems.

The DLD 4040-4Q is a 4-quadrant detector system. It is mounted on a x, y, phi translation/rotation stage within a 200mm vacuum pot. The pot is equipped with a CF 200 mounting flange as well as with feed-throughs for high voltage supply and signal transfer. The detector itself consists of a microchannel plate stack and two layers (x, y) of a 4-fold meander structured delayline. The image is sampled by the DLD readout electronics.
The 3D (x, y, t) detection bases on the measurement of time differences and time sums of signals, with a high temporal resolution in one device.

Typical applications are for example:

- imaging of parallel incident particle beams, particularly electrons
- spatially resolved time of flight spectroscopy in 2D/time resolved mode
- time referenced imaging of electrons excited by repetitive driven sources

and in energy analyzers:

- Fermi surface mapping, band mapping, photoelectron diffraction measurements, and similar angular dispersion experiments in 2D mode
- XPS, UPS, ESCA and AES in virtual channel mode
- Stroboscopic experiments in 2D/time resolved mode

3 Installation

3.1 Initial Inspection

Visual inspection of the system is required to ensure that no damage has occurred during shipping. Should there be any signs of damage, please contact SURFACE CONCEPT immediately. Please check the delivery according to the packing list (see Table 1) for completeness.

1. Dual HV Supply
2. Fourfold Quad Channel USB 2.0-TDC
3. Pulse processing unit ACU 3.16.2
4. Controller for translation/rotation stage including controller cables
5. Delayline Detector DLD4040-4Q under vacuum
6. 4x DLD readout cables (HDMI) (not displayed in figure 1)
7. USB 2.0 cables for TDC and for translation/ rotation stage controller (not displayed in figure 1)
8. 4x SHV cables & 1x SHV short circuit plug (not displayed in figure 1)
9. GUI Monitor Software (CD) and Manuals (not displayed in figure 1)
10. Controller Software (CD) and Manual for translation/rotation stage (not displayed in figure 1)
11. Power cables for TDC and HV Supply (not displayed in figure 1)

Table 1: Packing list for the Delayline Detector

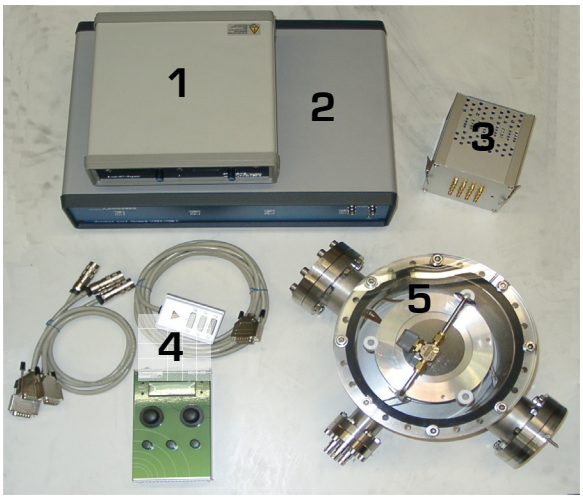


Figure 1: Contents of delivery package

3.2 Installation

3.2.1 Mounting the delayline detector

The detector is transported under vacuum. Vent the transport container **carefully** and release the M8 screws of the Plexiglas cover. The Plexiglas cover also functions as a transportation lock for the detector. Therefore remove the cover **carefully**.

Check the front side of the MCP stack for particles.

The microchannel plates in front of the detector should be protected from exposure to particle contamination. Particles that stick to the plate can be removed by carefully using a single-hair brush carefully and/or with dry nitrogen. Reading the instructions "microchannel plates" in chapter 12 is strongly recommended.

Install the detector to your vacuum chamber.
Keep the cover in case that the detector must be sent back for repairing. It can also be used to store the detector when not installed in a vacuum chamber.

The detector should be kept under vacuum all the time.

3.2.2 Detector Orientation

The black dots in Figure 2 mark the 0/0 positions of the DLD images of each quadrant, which correspond to the upper left corners of the DLD images in the GUI software.

Figure 2 is only correct when the rotator is positioned at 0° (for details see chapter 10).

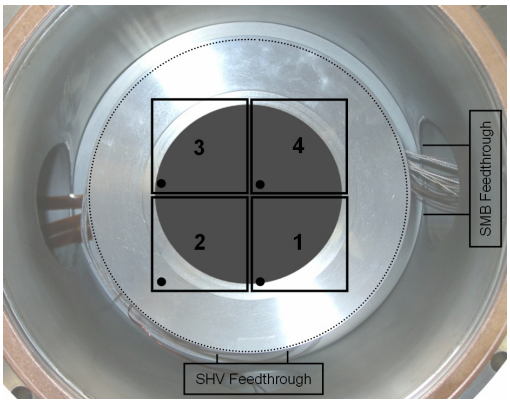


Figure 2: 0/0 positions of the DLD images of the 4 quadrants (black dots).

3.2.3 Cabling and High Voltage

The general connection scheme of the delayline detector including its readout package is shown in Figure 3.

CAUTION

The inner pins of the SMB feed-throughs of the 16-fold SMB flange are very sensitive. Be very careful when connecting the ACU 3.16.2 to the flange. Hold the ACU straight and do not tilt it, when plugging it to the flange.

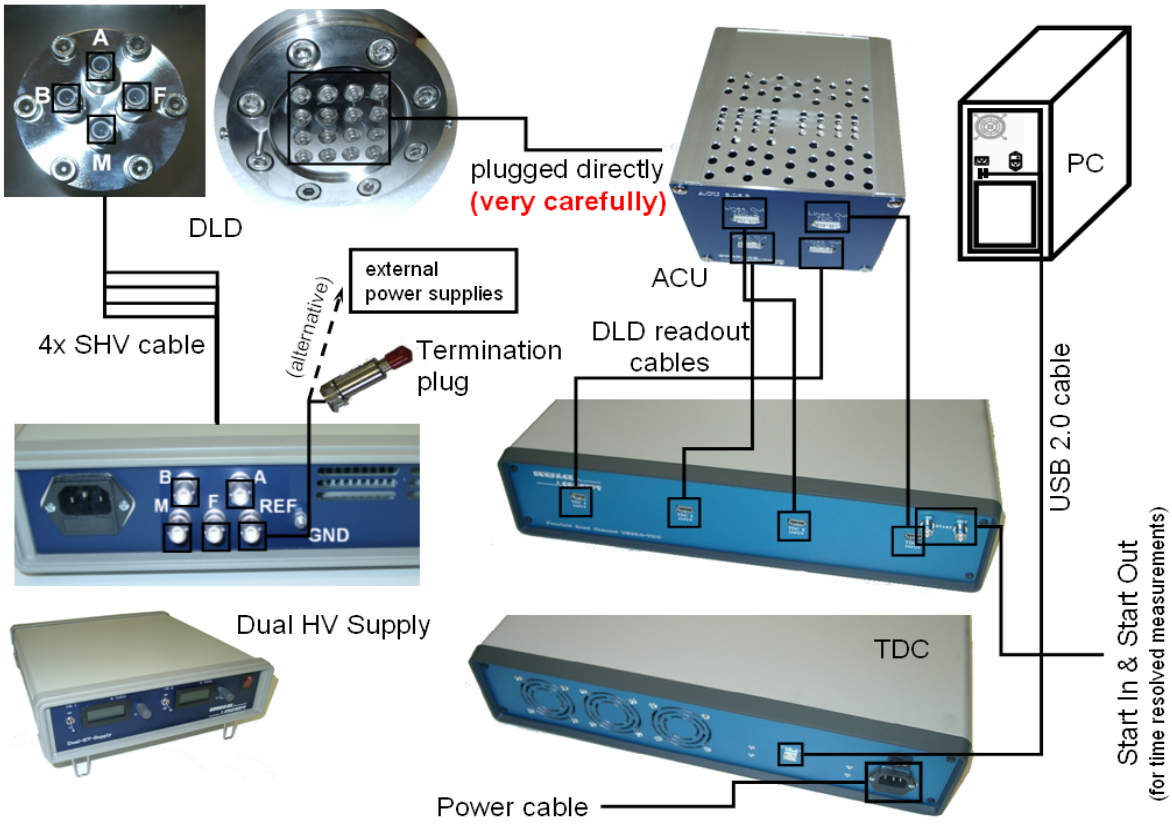


Figure 3: Connection scheme of the delayline detector and readout package.

- A CF 63 flange with 16 SMB feed-throughs is used for the signal transfer of the 4 quadrants. The pulse processing unit ACU can be connected directly to this 16-fold SMB flange. The metal pin gives the orientation. Fix the ACU with the two clips on the housing to the fastening bolds on the feed-through. **Connect the ACU very carefully. Respect the warnings given above.**

- A CF 40 flange with 4 SHV feed-throughs is given for high voltage supply of the detector. The four feed-throughs connect the detector anode (A) as well as the back side (B), the middle (M), and the front side (F) of the MCP stack. The corresponding labeling A, B, M and F can be found directly on the feed-throughs.

- The Dual HV Supply holds 5 SHV connectors labeled A, B, M, F and REF. Use the 4 SHV cables to connect the 4 SHV feed-throughs on the CF 40 flange with the corresponding SHV connectors of the Dual HV Supply. The "REF" connector can be used to apply a reference voltage to the front side of the MCP stack (e.g. the column potential in an electron microscope or the Herzog potential in an electron

spectrometer). The internal wiring of the Dual HV Supply is made in such a way, that all 4 output voltages (A, B, M, F) are floating on this reference voltage. The termination plug is used to ground the front side of the MCP stack, in case that no reference voltage is applied. Further information about detector operation voltages and MCP front reference voltages can be found in chapter 11.

A SHV termination plug is included in the delivery. In cases that no reference voltage is applied to the MCP front, the termination plug must be used to ground the MCP front. Otherwise the MCP stack is not functioning as the reference potential is missing.

Be sure that all voltages are settled to zero before connecting the high voltage cables to the detector, otherwise serious damage to the detector can occur due to high voltage sparks.

- Use the 4 DLD readout cables to connect the sockets "Lines Out TDC 1" to "Lines Out TDC 4" on the front of the ACU to the corresponding input sockets "TDC 1 Input" to "TDC 4 Input on the rear panel of the Fourfold Quad Channel USB2.0-TDC. Use the BNC socket named "Start In" to apply standard TTL signals as start trigger for the time measurement and use the signal from the "Start Out" socket to trigger an electron/ ion source. For further details see the manual of the Fourfold Quad Channel USB2.0-TDC.

- Use the USB 2.0 cable to connect the USB2.0-TDC to the PC and follow the instructions for installing the device driver if connected for the first time. If the device driver is already installed, the USB connection is established automatically. Do not use PC front panel USB connectors; they are often restricted in performance. For further details on driver installation please see chapter 4.

  Connect the power cable to the main connector and plug the USB cable into the PC. Switch on the TDC and follow the instructions for installing the device driver being connected for the first time. If the device driver is already installed, the USB connection is established automatically.

Finish the complete cabling before the TDC is turned on and the GUI monitor software is started. Also, close the software and turn off the TDC before performing any changes to the cabling.

Don't start the detector operation before you are familiar with the detailed descriptions of chapter 11 within this manual.

3.2.4 Cabling of translation/ rotation stage

The general connection scheme of the translation/ rotation stage is shown in Figure 4.

CAUTION **There is a separate manual for the translation/ rotation stage within the delivery package. Read this manual, before connecting the stage. Stick to the advices and respect the warnings given within this manual.**

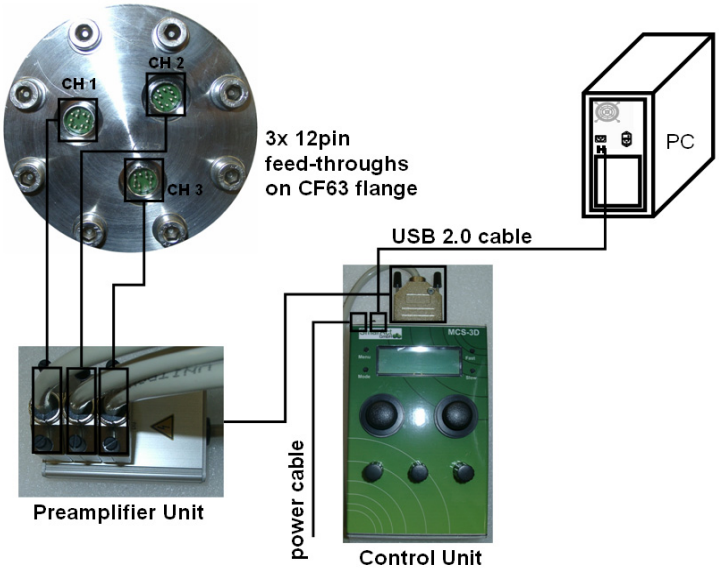


Figure 4: Connection scheme of the translation/ rotation stage.

- A CF63 flange with three 12pin feed-throughs is used for the power line and read-out signal transfer of the two translators and one rotator. The three feed-throughs are named "Ch 1" to "Ch 3" in comparison to the naming within the control unit. The naming of the feed-throughs can be found directly on the CF63 flange.
- Connect the three short signal cables to the three 12pin feed-through "Ch 1" – "Ch 3" and to the corresponding D-Sub socket of the preamplifier unit.
- Connect the preamplifier unit to the control unit.
- Connect the power supply to the control unit.
- Turn on the device.

CAUTION **First connect the power supply to the control unit, before switching it on.**
Do not connect the power supply with the power switch of the control unit switched to on.
Read the manual of the control unit.

3.2.5 Recommended System Requirements

Read-out of the USB2.0–TDC is done with a standard PC via USB2.0. For the PC the following system requirements are highly recommended:

- Processor: 1.6 Ghz
- RAM: 1GB
- Windows XP / Windows 2000
- USB 2.0 (no front panel connector)
- Monitor resolution: in Y min. 864 pixel (most critical), in X min. 1024 pixel

The use of USB2.0 for the readout of the TDC is highly recommended. In principle the readout of the TDC is compatible to USB1.0, but the required data transfer rates are not reached. Do not use PC front panel USB connectors; they are often restricted in performance.

4 USB 2.0 Driver Installation

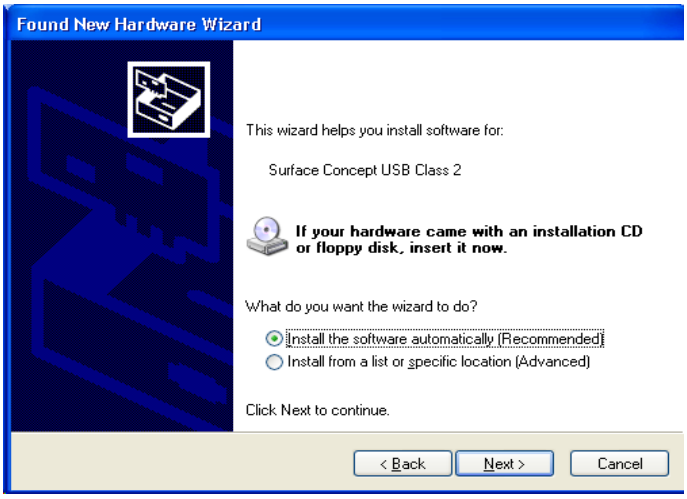
This description helps you to install the driver for the Fourfold Quad Channel USB2.0-TDC

- First, log on as Administrator. Close all applications on your PC. If you are using any anti-virus or firewall software, close them (or disable them). Turn off the TDC, if already turned on. Connect the USB cable to your Windows System with USB2.0 enabled. Windows will recognize the internal hub and will connect to it.

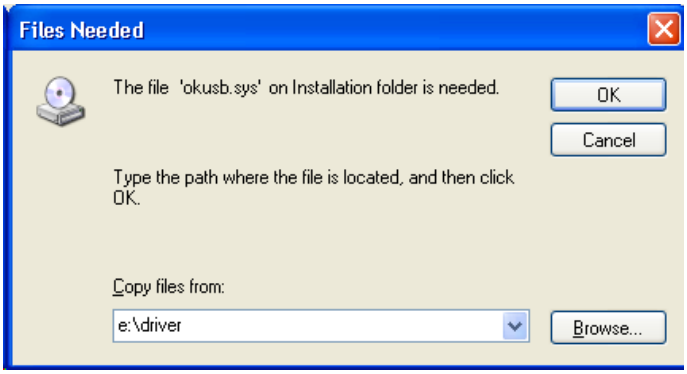
- Now turn on the TDC. The PC will detect the new hardware, and the "Found New Hardware Wizard" will launch. To continue, select “No, not this time” (not looking for windows updates) and ”click "Next>".

- Insert the CD-ROM, included in the delivery, into the PC's CD-ROM drive.

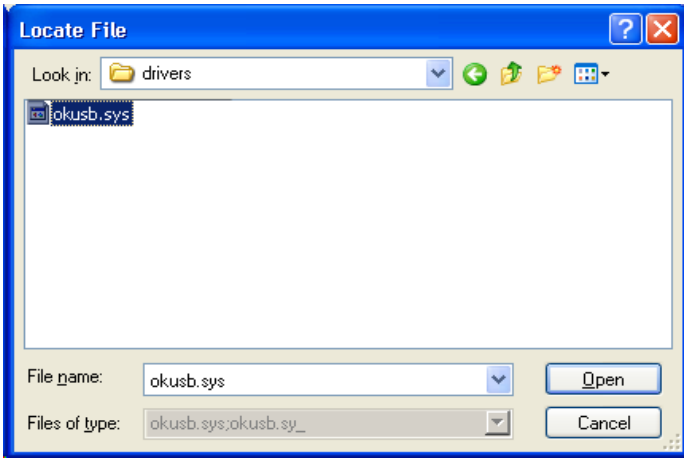
- Select "Install the software automatically (Recommended)" and Click "Next>".



- Enter the path where the driver is located (or Browse to it), if needed.

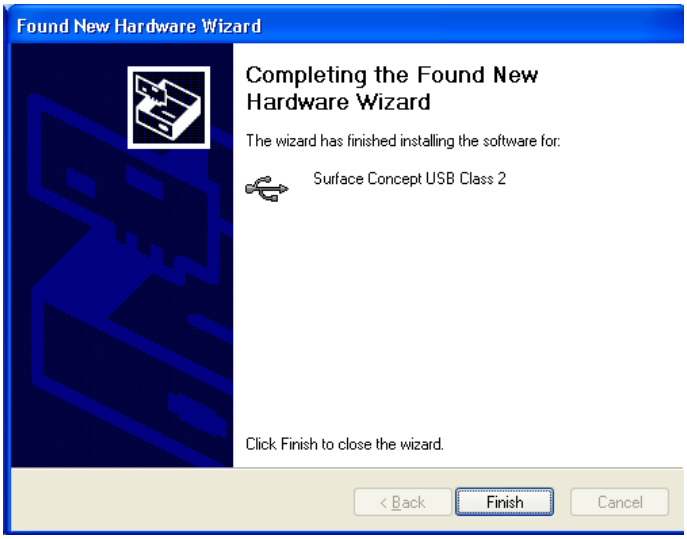


- The internal name of the USB2.0 TDC driver is “okusb.sys”, select it and press “Open”.



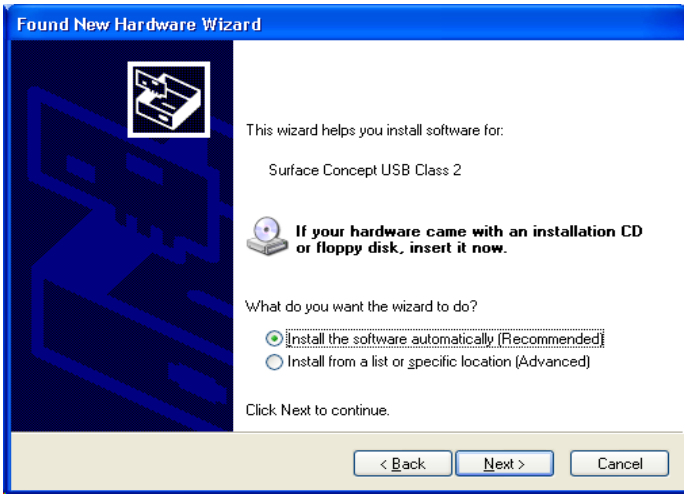
- To continue, click "OK". The driver for the Surface Concept Fourfold Quad Channel USB2.0 TDC will be installed.

- After a few seconds, a finishing dialog should appear as below. To finish, click "Finish".



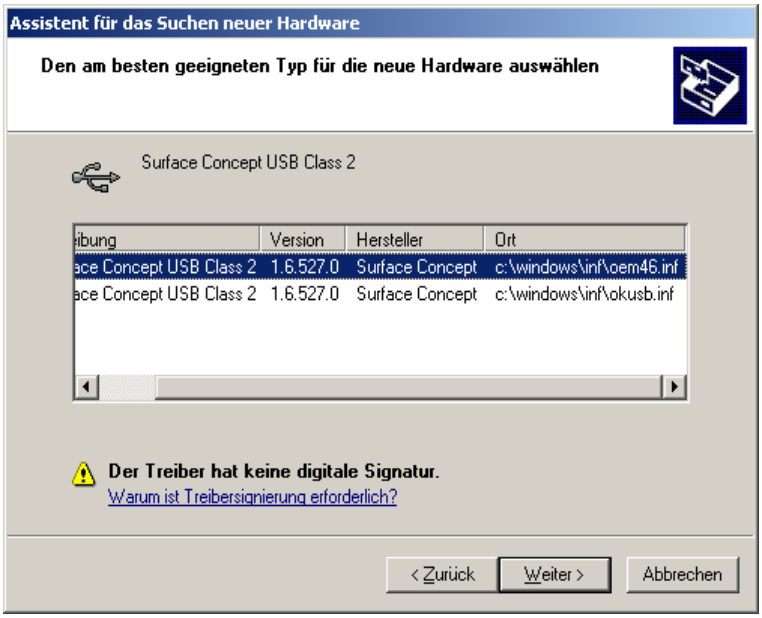
The driver must be installed four times in total, because the TDC encapsulates four independed units, which are all individually recognized by the PC. Therefore after finishing the installation for the first time, it will start again anew another three times.

- Select "Install the software automatically (Recommended)" and Click "Next>".



with the second installation windows notices that the driver has already been installed on the system and it asks you to select the best suited driver.

- Select the driver in following version: “OEM46.inf”



The installation is complete after finishing the fourth installation.

Note

The installation routine must be started for four times in total, due to the four independent units within the TDC.

5 DLD - Principle of Operation

5.1 Basics of Delayline Detection

A delayline detector (DLD) consists of a microchannel plate array for pulse amplification and an in-vacuum readout unit consisting of a meander structured delayline (DLD anode). Each hit position is encoded by a fast data acquisition unit, which also may detect the hit time referenced to an external clock in repetitive (stroboscopic) experiments.

Principle of the 3D(x,y,t) delayline operation

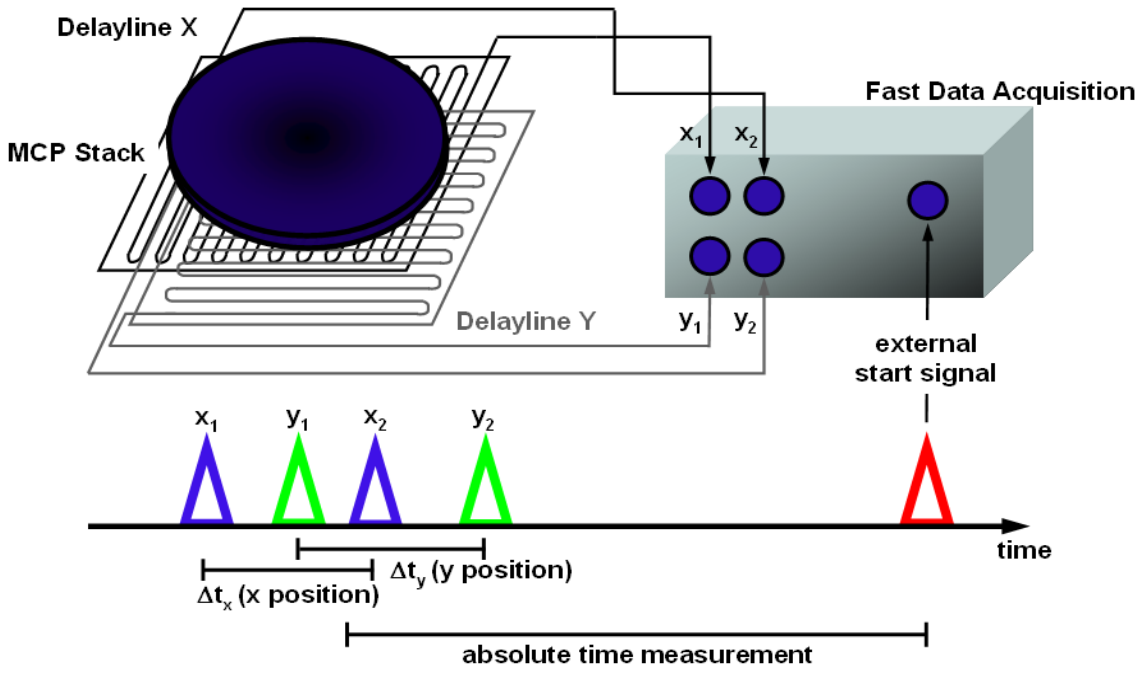


Figure 5: Priciple of the 3D (x, y, t) delayline operation

The DLD anode (for 4 quadrant DLDs: each single quadrant) consists basically of two meander structured delaylines, the one rotated by 90° with respect to the other and both isolated from each other. The delaylines are positioned behind a microchannel plate stack, which is required to amplify incoming electrons by at least

10^7. The electron cloud from the MCP stack output is drawn to the DLD meander (positive potential difference between anode and back side of MCP stack) where it induces electrical pulses in the delayline by capacitive coupling. The pulses are traveling to the both ends of the meander within a time determined by the hitting position. The average time at both ends of the meander relative to an external repetitive clock generates the time coordinate if required.

Delayline detectors are single counting devices; therefore the complete device works linearly even at extremely low numbers of incoming electrons.
The detection principle limits the maximum detectable count rates at least due to the maximum delay of the meanders. Currently, the main limitation is given by the appearance of multi-hit events, which can only be resolved up to a certain degree. The maximum count rate in the fourfold coincidence measurement is right now at about 2.0 x 10^6 counts per second.

5.2 Basic Operational Modes of the Delayline Detector

5.2.1 2D(x, y) Area Detection

The arrival times of pulses per event at the 4 ends of each DLD meander/ quadrant are subtracted in order to determine a position in x and y (x: tx1-tx2; y: ty1-ty2). The TDC stop signals are grouped internally in pairs to form x and y. All DLD software adjustments are done by the end-user software according to the user's chosen parameters.

5.2.2 3D(x, y, t) time resolved imaging

The delayline detector may measure all events in temporal reference to an external clock. For this mode, the user needs to start the USB2.0-TDC by an external clock, providing a low jitter LVTTL (or TTL) signal to the start input of the TDC.

Time measurements are performed by summing up the arrival times of pulses at the end of the DLD meanders, i.e. the same results which are used to determine positions for each event are summed. It is possible to sum only tx1 and tx2 (tsumx) or ty1 and ty2 (tsumy). Because both sums should carry the same temporal information of a time related experiment, the total sum t(DLD) of all four time measurements (tx1, tx2, ty1, ty2) may be a good choice as well. The results of all these time sums correspond to t(sum) = t(offset) + n * (t(hit) – t(reference)), where (t(hit) – t(reference)) is the interesting time (e.g. ToF) in a given experiment, n is the number of summed time results (2 or 4 results), and t(offset) is a device related constant, which depends on cable lengths, electronics propagation times, experiments setup etc.. Therefore, it is possible to completely determine position and time of each event from only 4 precise time measurements.

The software may group all measured time sums in plain 1D time histograms, which are valid for the chosen region of interest (ROI). The time bin size for each readout channel x1, x2, y1 and y2 is 82ps in the I-mode, see chapter 8.2. The channel width in the 1D histogram is 41ps for the tsumx and tsumy histograms as well as 20.5ps for the total t(DLD) histogram.
The time bin size for the readout channels in the R-mode, see chapter 8.2, is 27ps and the channel width in the 1D histogram is 13.5ps for the tsumx and tsumy histograms and 6.75ps for the total t(DLD) histogram. Due to the calculation of the tsums and t(DLD), the time axis is expanded virtually (simplified expression). The t(DLD) signature can be used in order to setup the regions of interest in time for measurements of time resolved images, the software is able to sample 3D histograms as image stacks in time, where each image corresponds to one time bin of the total time histogram.

5.3 Data Acquisition

In the delayline detector, the meander/ each quadrant is connected to a fast amplifier followed by a constant fraction discriminator (CFD) for pulse shaping. They are encapsulated inside the pulse processing electronics (ACU = Amplifier-CFD-Unit or AU = Amplifier-Unit). The main function of the CFD is digital pulse discrimination, ideally without any time-walk even at varying pulse heights. A time-to-digital converter (TDC) behind these chains serves as stop-watch for arrival time measurements. The measurement results, in terms of differences and sums are fed into the PC via a USB 2.0 interface and are completed to 2D images (with or without time stamps) by the histogram module of the data acquisition DLL. Data processing and presentation on the PC is realized achieved with the GUI software. See the corresponding software manuals for detailed information on the software package.

5.4 Working with the DLD – Important details

The DLD is a counting system that works in a laterally resolving sense by detecting four pulses from the four ends of the delayline meanders in fourfold coincidence. It only works correctly within a certain range of the supply voltage. The MCP voltage has to exceed an operation threshold for the detector otherwise the pulse detection is not possible. This is due to the induced pulses on the delayline which have to reach a certain amplitude to be detected by the electronics, independent on the intensity of the electron source (e.g. mercury lamp). On the other hand, if the MCP voltage and/or the intensity of the electron source are too high, the detector overloads and again pulse detection is not possible. Saturation effects of the MCPs limit the amount of electrons provided by single pulses. An intensity increase of the electron source leads to an increased number of hits on the MCP. The current per bunch and therefore the amplitude of the pulses decreases. There are two kinds of overloads: local and global. A local overload (locally high intensity on the MCP) leads to no count rate within this local area and to an absolute “black spot” in the images. An intensity too high and homogeneously distributed over the whole MCP first leads to diffuse images and with further increasing intensity to randomly distributed artificial structures up to no count rate at all (global overload). The explanation for the effects for a local overload is a pulse amplitude that is too low to be detected by the electronics. The explanation for the global overload effects is mainly the loss of the fourfold coincidence condition of an incoming event and a fitting fourfold coincidence of random pulses, respectively. High intensity on the MCPs always leads to a significant pressure increase. Therefore an observed pressure increase can always be taken as an indicator for an overload of the detector, when problems with the functionality of the DLD occur.

It is easy to mistake an overload for no signal at all. To distinguish between these two, check the pressure. A pressure increase indicates an overload.

The DLD has been calibrated for an optimized MCP voltage and it is strongly advised to use this optimized voltage value for operation. It is given in the specification sheet. A change of the MCP voltage can lead to artifacts within the images. The MCP voltage should only be increased to compensate a decrease in amplification of the MCP stack do to wearing-out.

6 Delayline Detector Layout

6.1 Delayline Detector - Vacuum Wiring

The delayline detector DLD 4040-4Q consist of a round detection area, defined by the MCP holders and the detector cover. The detector anode consists of four independed quadrants (numbered 1 - 4) each with two meander structured delaylines (named x and y). The x and y meander are placed above each other (electrically isolated) and are orientated perpendicular to each other. The delayline in the top layer is referred to as the x meander and the delayline in the buried layer as the y meander. Figure 6 gives a schematic orientation of the x and y meanders,
Signal readout is done via two readout lines (named 1 and 2) for each meander-structured delayline in each quadrant. There are 4 readout lines for each quadrant, therefore 16 readout lines for the complete detector. The naming of the single readout lines is put together of the naming of the quadrant 1 – 4, the naming of the meander structured delayline x and y and the naming 1 and 2 of the individual readout lines per delayline (e.g. 3-x2 for the second line of the x meander of the third quadrant).
The 0/0 position of the DLD image (top left corner of displayed image in the GUI software) is marked by a black dot.

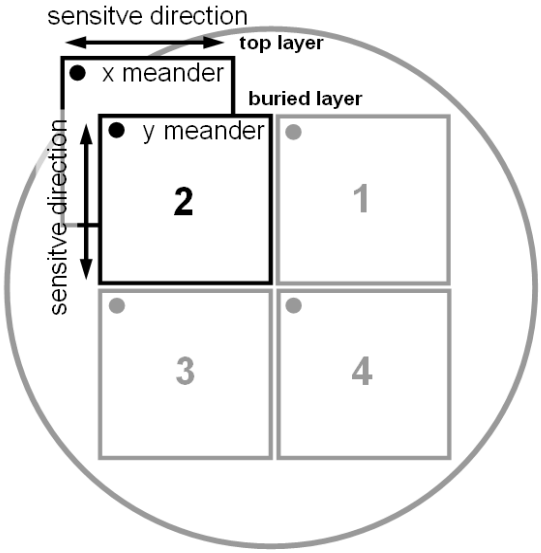
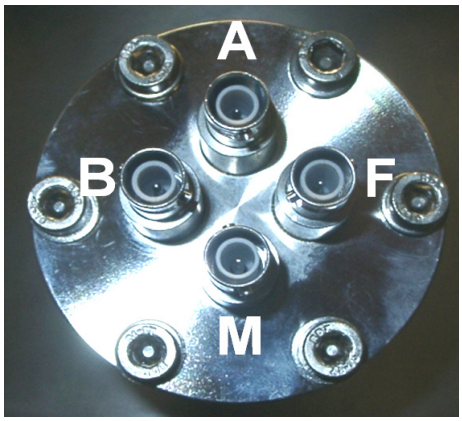


Figure 6: Schematic orientation and naming of quadrants and delay lines (view from the back side through the detector anode).

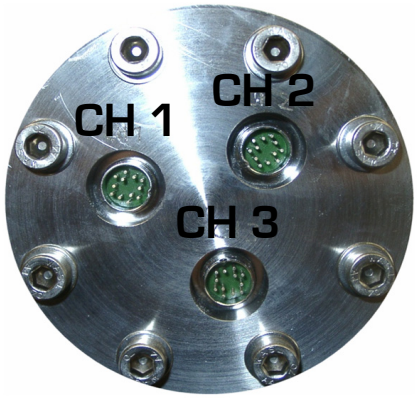
6.2 Delayline Detector – Connection Ports

The delayline detector carries a CF 40 flange with four single SHV feed-throughs for the high voltage supply of the detector, a CF 63 flange, which holds three 12pin feed-throughs for the power supply and the position readout of the translation/ rotation stage, and a second CF 63 flange, which holds 16 SMB feed-throughs for the signal transfer (see Figure 7), The flange for the signal transfer also holds an orientation pin for correct orientation of the ACU. The allocation of the 16 signal channels 1X1 – 4Y2 on the "SMB flange" can also be taken from Figure 7.

a)



b)



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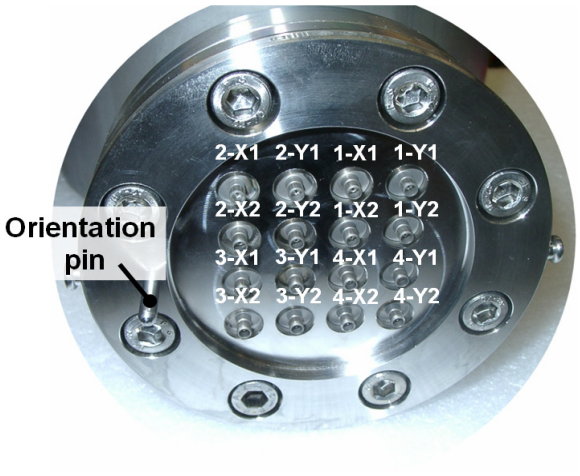


Figure 7: Connection ports for the DLD: a) 4-fold SHV feed-through for high voltage supply, b) three 12pin feed-through for power supply and sensor readout of translation/ rotation stage, and c) 16-fold SMB feed-through.

The channel naming of the three 12pin feed-throughs can be found directly written on the CF63 flange. The high voltage potentials for the delayline detector MCP front (F), middle(M), back (B) and detector anode (A) are written directly on the SHV feed-throughs. The internal high voltage connection for the delayline detector is given schematically in Figure 8.

CAUTION

Do not disconnect single high voltage cables from the delayline detector as long as high voltage is applied. This will lead to sparks which can damage the very sensitive detector, the MCPs and/or the analogue readout electronics seriously.

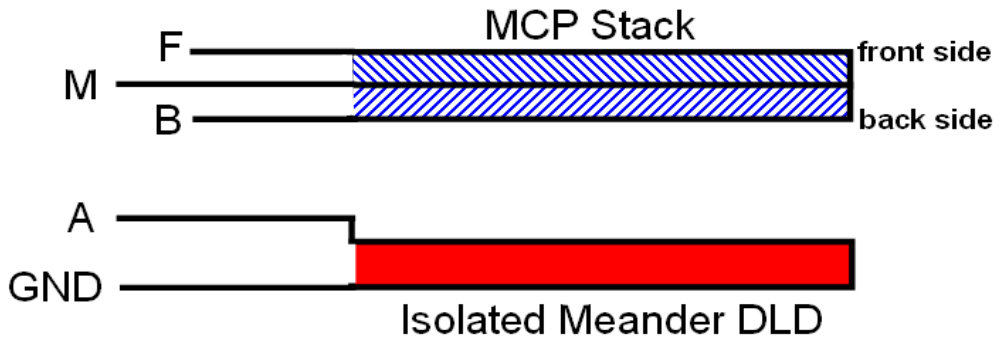


Figure 8: Internal connection of high voltage potentials (schematic).

Note

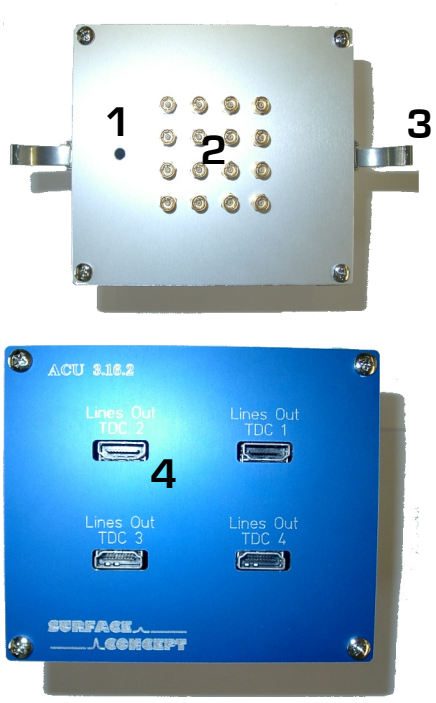
The resistance between MCP front and MCP back (resistance of MCP stack) should be in the range of 12 – 45 MΩ (the exact value is given in the specification sheet of your detector).

7 Pulse Processing Electronics

The pulse processing electronics ACU (Amplifier-CFD-Unit) and AU (Amplifier-Unit) hold all devices like the amplifiers, pulse shapers, and constant fraction discriminators to turn the analogue pulses from the detector into digital pulses suitable for the Time-to-Digital Converter. Pulse decoupling is either performed within the pulse processing electronics or directly in-vacuum, depending on detector type and layout. Some pulse processing electronics also contain an integrated high voltage power supply for the complete detector. This also depends on the layout of the detector as well as the pulse processing electronics.

7.1 Pulse Processing Electronics ACU 3.16.2

The ACU 3.16.2 contains the pulse amplifiers, pulse shapers and constant fraction discriminators.



1. Hole for orientation pin from SMB feed-through.
2. 16x SMB sockets for signal transfer from SMB feed-through.
3. Clip for fastening ACU to detector flange.
4. 4x Connection sockets for the DLD readout cables for each quadrant (corresponding naming to input sockets of Fourfold Quad Channel USB2.0-TDC).

Figure 9: Layout of ACU 3.16.2

CAUTION

The inner pins of the SMB feed-throughs of the 16-fold SMB flange are very sensitive. Be very careful when connecting the ACU 3.16.2 to the flange. Hold the ACU straight and do not tilt it, when plugging it to the flange.

The ACU can be plugged directly onto the 16-fold SMB feed-throughs. **Do this very very carefully. Hold the ACU straight and do not tilt it.** Fasten the two clips of the ACU to the fastening bolts of the CF 40 flange to fix it to the detector. Figure 9 shows the layout of the ACU 3.4.2.

7.1.1 Positions of the Discriminator Threshold Regulators

Discriminator threshold regulators as well as potentiometers for additional adjustments can be found on the corresponding boards inside the ACU 3.16.2. They can be reached through the holes on the top and the bottom side of the ACU housing (see Figure 10).

The adjustment of the readout electronics goes hand in hand with the detector voltage. In fact there is only a small "window" for an optimum setting of the readout electronics for a given operation voltage. Changes of the detector voltage, other than to compensate loss in the amplification of the MCP stack due to wearing out effects, will directly lead to a loss in performance of the readout electronics (artifacts within the image, increased dark count rate etc.). The readout electronics is adjusted to its best performance to the operation voltage of the detector when delivered. A new adjustment should not be needed. The operation voltage is given in the specification sheet.

The sensitivity of the CFD is increased (threshold decreased) by turning the screw of the potentiometer clockwise and vice versa for decreasing the sensitivity of the CFD. This is only to be used under some circumstances where adjusting becomes necessary at all.

CAUTION

The readout electronics is adjusted to its best performance to the operation voltage of the detector when delivered. Do not change the adjustment, without contacting Surface Concept before.
Changing the adjustment can easily end up with a status, where a readjustment must be done by Surface Concept.

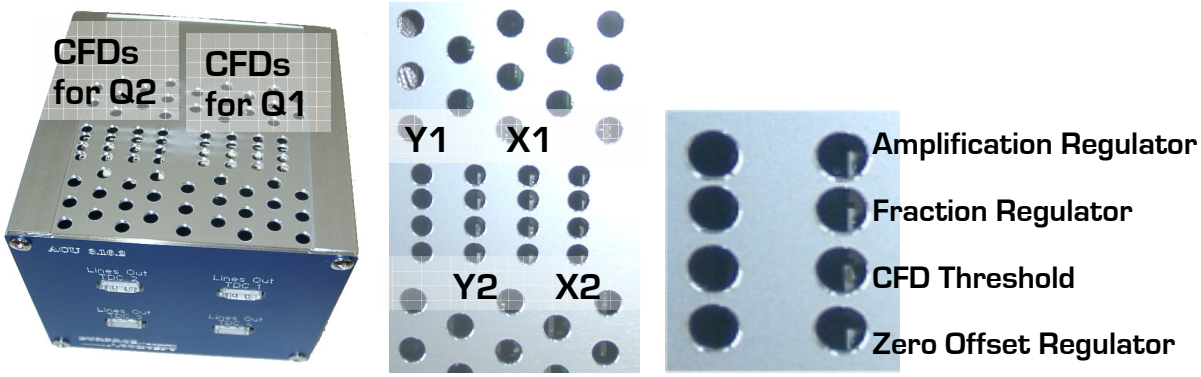


Figure 10: Labeling of discriminator threshold and amplification regulators.

8 Time-to-Digital-Converter (TDC)

8.1 Principle Layout of the USB2.0-TDC series

The USB2.0-TDC series combines the excellent performance of the GPX TDC chip (ACAM GmbH) with a field programmable gate array (FPGA) and a high speed USB interface, either in the design with a single GPX chip (USB2.0-TDC) or with two GPX chips (Double USB2.0-TDC) operated in I-mode with 82 ps bin size or with one (Dual Channel USB2.0-TDC) or two GPX chips (Quad Channel USB2.0-TDC) operated in R-mode with 27 ps time bin or G-mode with 36 ps time bin.
The FPGA enables comfortable setups and a variable data stream handling from the TDC via USB 2.0. The main delayline detector and segment readout (optional device) functionality is permanently programmed. A complex FIFO design makes data losses almost impossible. The user DLL controls the data handling and streaming for the user. The Fourfold Quad Channel USB2.0-TDC combines in principle four units of the Quad Channel USB2.0-TDCs in one device. It was especially developed for the readout of high rates of 4-Quadrant Delayline Detectors.

8.2 Principle Operation Modes of the GPX TDC Chip

The GPX TDC chip can in principle be operated in the following modes. Not all modes are available for all USB-TDC devices.

8.2.1 I-Mode (USB2.0-TDC/ Double USB2.0-TDC)

- 8 stop channels with 82.3 ps digital time bin resolution
- 1 start channel
- Input level: TTL or LVTTL
- 5.5 ns pulse-pair resolution on one channel and 0 ns between two channels
- 32-fold multi-hit capability = 182 MHz peak rate
- Trigger to rising or falling edge
- Measurement range: 0 ns – 10.6 µs in start-stop operation
- Endless measurement range by internal retrigger of START
- 10 MHz continuous rate per channel
- 40 MHz continuous rate per chip

8.2.2 R-Mode (High Resolution/ Dual Channel/ Quad & Fourfold Quad Channel USB2.0-TDC)

- 2 stop channels with typically 27.4 ps digital time bin resolution
- 1 start channel
- Input level: differential LVPECL
- 5.5 ns pulse-pair resolution on one channel and 0 ns between two channels
- 32-fold multi-hit capability = 182 MHz peak rate

- Trigger to rising or falling edge
- Measurement range: 0 ns – 40 µs in start-stop operation
- 40 MHz continuous rate per channel
- 40 MHz continuous rate per chip

8.2.3 G-Mode (High Resolution/ Dual Channel/ Quad Channel USB2.0-TDC)

- 2 stop channels with 41.2 ps digital time bin resolution
- 1 start channel
- Input level: differential LVPECL
- 5.5 ns pulse-pair resolution on one channel and 0 ns between two channels
- 32-fold multi-hit capability = 182 MHz peak rate
- Trigger to rising **and** falling edge
- Measurement range: 0 ns - 65 µs
- 40 MHz continuous rate per channel
- 40 MHz continuous rate per chip

8.3 Schematic Description of the Fourfold Quad Channel USB2.0-TDC

The Fourfold Quad Channel USB2.0-TDC consists of four units of a combined GPX-TDC and FPGA board. Each of these units works independently in respect of time measurements, data pre-conditioning, and buffering. They all carry their own 32 MByte memory for data buffering. It is restricted for operation in the R-Mode.
The Fourfold Quad Channel USB2.0-TDC is especially designed for the readout of high count rates of 4-quadrant delayline detectors. Each of these four units reads out the signals of one quadrant.
Arrival times of pulses on the stop inputs are measured by the TDC with respect to an internal reference start signal, provided by the FPGA. One of the four FPGAs is designated as master device. It controls and synchronizes the internal reference start signal as well as the measurement dwell times for data for all four devices. The measurement dwell times are settled by a quartz stabilized time gate. The TDC data streaming can be performed as measured (RawData mode) or including a DLD specific data pre-conditioning (Pair mode). This concerns as a major part a Double Hit Recognition (DHR) Algorithm which enables the detection of double hit events and also includes a pair result arithmetic. Communication to and from the PC is achieved via a USB 2.0 interface. Here the four units are linked together to an internal USB2.0 hub. A schematic sketch of the Fourfold Quad Channel USB2.0-TDC functioning is given in Figure 11.

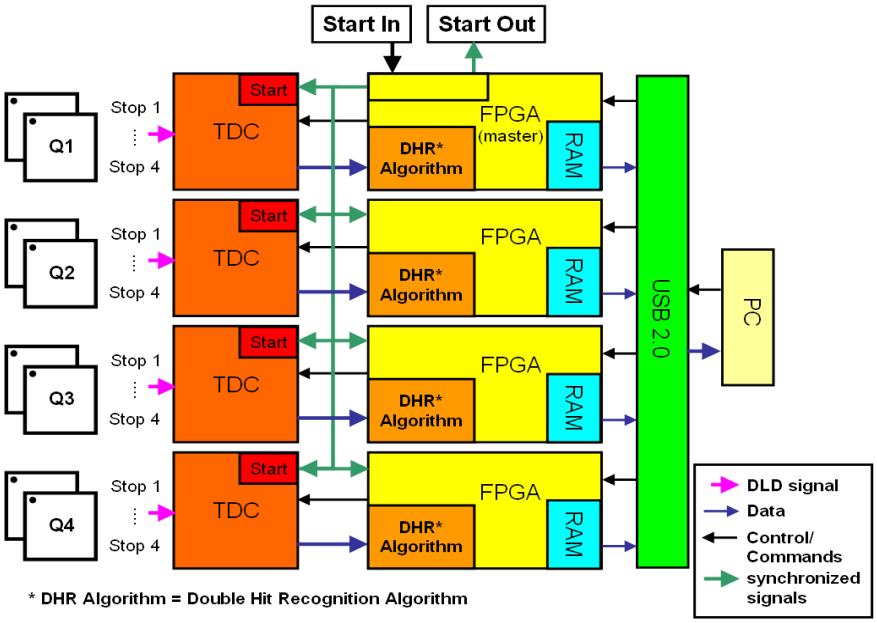


Figure 11: Schematic sketch of the Fourfold Quad Channel USB2.0-TDC functioning

8.4 Layout of the Fourfold Quad Channel USB2.0-TDC

1. BNC socket for TDC start out
2. BNC socket for TDC start in
3. Output of internal 80 MHz clock on Lemo – Socket.
4. TDC 1 Input: HDMI socket for DLD readout cable from ACU "Lines Out TDC 1" socket
5. TDC 2 Input: HDMI socket for DLD readout cable from ACU "Lines Out TDC 2" socket
6. TDC 3 Input: HDMI socket for DLD readout cable from ACU "Lines Out TDC 3" socket
7. TDC 4 Input: HDMI socket for DLD readout cable from ACU "Lines Out TDC 4" socket

8. USB 2.0 connection socket
9. Power switch to turn the TDC ON/OFF
10. Power socket

Figure 12: Layout of the Fourfold Quad Channel USB2.0-TDC

8.4.1 TDC Stop Inputs

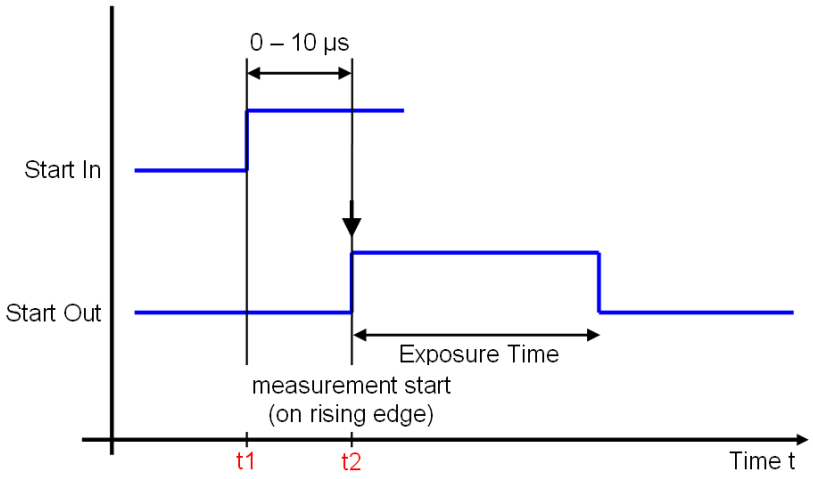
The Fourfold Quad Channel USB2.0-TDC provides 4 HDMI sockets for signal inputs (stop inputs) of a delayline detector (e.g. the 4 quadrants of a 4-Quadrant DLD). The TDC inputs are laid out for PECL levels.

8.4.2 TDC Start Inputs

The synchronized distribution of the start signal to all four units requires a defined start signal controlled and given out by the TDC itself. For this, the Fourfold Quad Channel USB2.0-TDC carries a BNC socket named "Start Out". In opposite to the other devices from the USB2.0-TDC series, the Fourfold Quad Channel USB2.0-TDC is working only with an internal start and does not offer the alternative to work with a start signal from an external source.
When starting a measurement from the software, the master unit synchronizes the measurement of all four units to the next internal start signal. Parallel the TDC gives out a start signal to the "Start Out" socket in form of a TTL pulse. The time measurement of all four units within the TDC is highly defined and stable to the rising edge of this pulse. The definition of the "Start Out" pulse is illustrated in Figure 13. This start signal must be used to start the experiment (e.g. laser, electron gun).
Additionally it is possible to apply a trigger signal to the TDC, to synchronize the start of a measurement to the needs of the application. This trigger signal must be given as a TTL pulse to the "Start In" socket of the TDC. In this case, the TDC waits with the start of the measurement for the next trigger signal after the measurement has been started by the software. There is a maximum delay time between the trigger signal to "Start In" and the actual start of the measurement of up to 10 µs (see Figure 13).

Note

It is highly important to use the "Start Out" signal to trigger your experiment/ application. There is no possibility to apply an external start signal to the TDC.



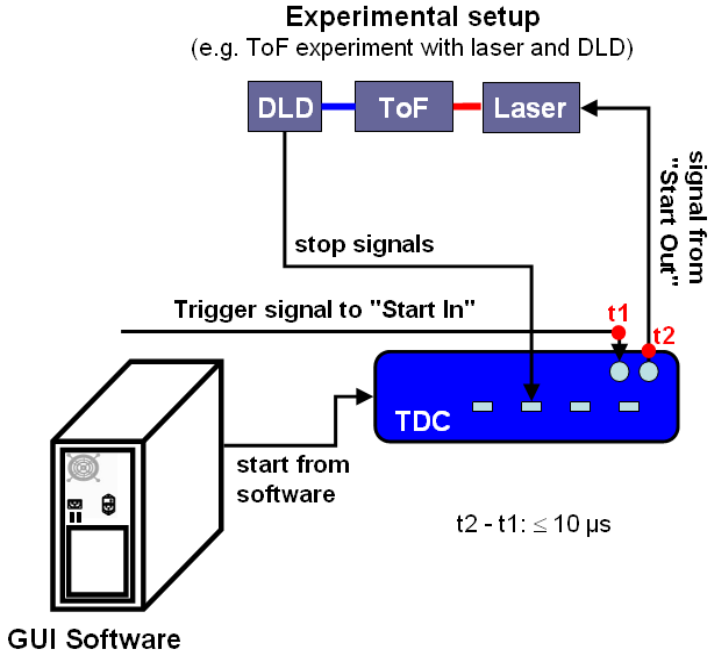


Figure 13: Illustration of signal from "Start Out" and start signal functioning for time resolved measurements.

8.4.3 Line Input

Electrical Input (LINE):	85 V – 260 V, 50/60 Hz
Power:	175 Watt (max.)
Fuse:	1x T 2.5 A

8.5 Extended Time Range and theoretical Count Rates

The Fourfold Quad Channel USB2.0-TDC is especially designed to extend the measurement time range far above the 40 µs limit of the R-mode of the GPX chip.
Hereby the maximum measurement time range as well as the maximum possible count rate differs in dependence on the data mode of the TDC (Raw Data Mode or Pair Mode).

8.5.1 Extended Time Range in Raw Data Mode

Four signals (x1, x2, y1, and y2) are needed to be measured for one event. In Raw Data Mode each of these four measurements is being transferred to the PC, before the pairing to one event (quadruple) is made by the software layer. This allows extending the maximum time range to 29.5 ms. The time base is 27.4ps (R-mode).
As long as the total number of measured events does not fill up the complete memory of 32 MByte per unit, the maximum possible count rate is limited by the writing speed into the memory. In this case, the maximum writing speed is equivalent to 15 mio. events per sec. for one single quadrant and equivalent to 60 mio. events per sec. in total for all four quadrants.
The maximum possible count rate is limited by the USB transfer speed of approx. 30 MByte in case that the memory is filled up completely during a measurement. In this case the maximum possible count rate is 1.88 mio. events per sec. in total for the complete DLD.

8.5.2 Extended Time Range in Pair Mode

In the Pair Mode the results for the single events are grouped together by the Double Hit Recognition (DHR) Algorithm directly within the FPGA. This pairing reduces the amount of data needed to describe one event significantly. It also reduces the time base from 27.4 ps to 6.9 ps (27.4ps/ 4). All this allows increasing the extended time range to a maximum of 7.5 s.
Due to the reduction in size the maximum possible count rate is also increasing. As long as the total number of measured events does not fill up the complete memory, it is now limited by the TDC measurement speed. Each unit within the TDC is able to measure 20 mio. events per sec. so that the maximum possible count rate for all four quadrants together is equivalent to 80 mio. events per sec. The maximum possible count rate is limited by the USB transfer speed again, in case that the memory is filled up completely during a measurement. Due to the reduced size per event, the USB transfer speed allows a maximum count rate of 3.75 mio. events and even more.
The DHR algorithm is designed in such a way, that the size per event is further reduced when the time range for incoming events is kept small and/ or the time binning is enlarged. In the limit of a very large time bin/ small time range for incoming events, the size per event can be further reduced by a factor of two. This has no effect when the count rate is limited by the TDC measurement speed. But in case that the count rate is restricted by the USB transfer speed, this will increase the count rate up to a maximum of 7.5 mio. events per sec. in the maximum limit.

8.6 Error Values in Time Measurements

The time measurement by the TDC itself is connected with an error, which is not constant but increases linearly with the number of incoming stop signals until the next incoming start signal resets the time measurement. Therefore the size of an error value for the measurement of a single stop signal depends strongly on the count rate and on the period of the start signal. The larger the count rate and the larger the period of the start signal, the further the error value will increase. The last detected stop signal, before the next incoming start signal, is measured with the largest error (maximum error value). The increase of the measurement error is illustrated in Figure 14.

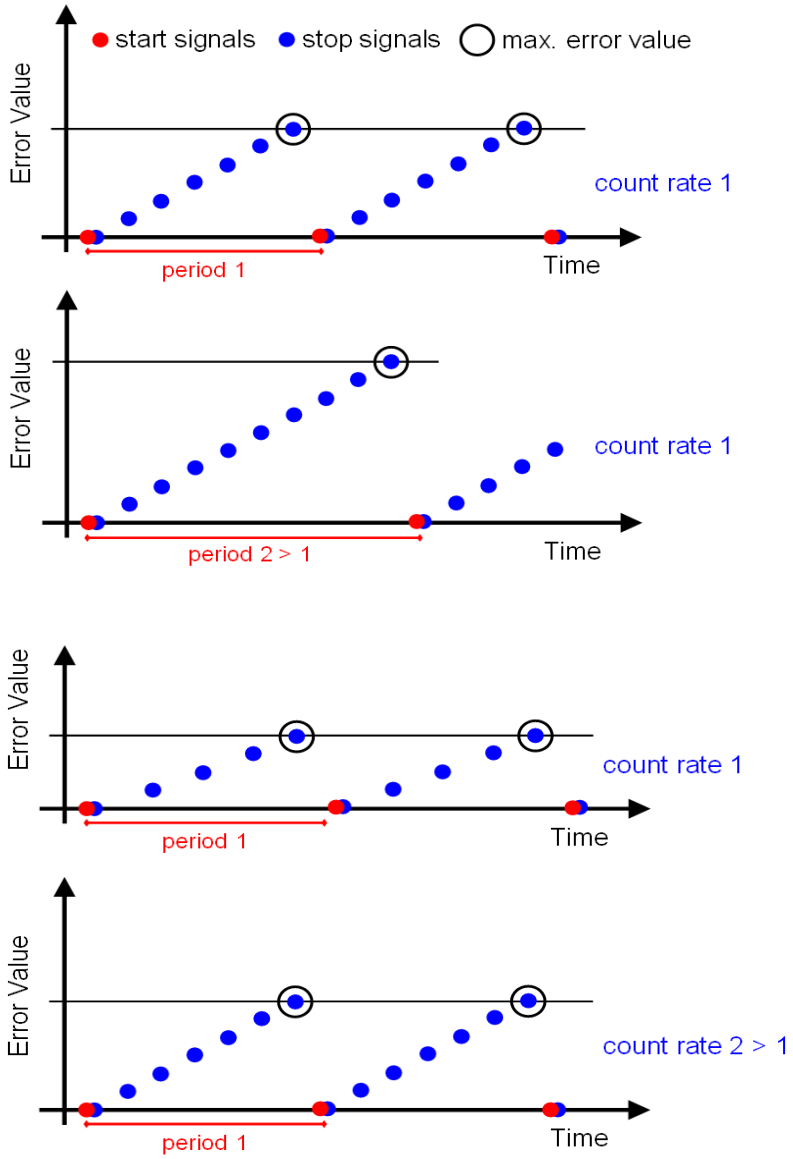


Figure 14: Illustration of increasing error in time measurements

The TDC chip contains a correction loop (the so called PLO loop) to minimize the measurement error. It takes up to some few ms for the PLO loop to minimize the measurement error. The time, which is needed by the PLO loop, also depends on the count rate and the period of the start signal. An example for the error minimization due to the PLO loop is given in Figure 15.

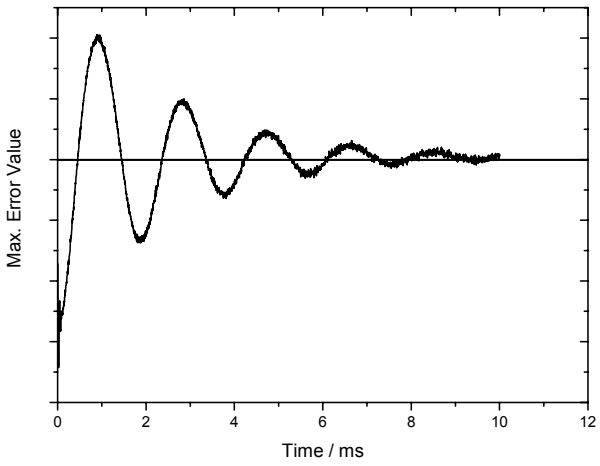


Figure 15: Example for the minimization of the measurement error of the TDC due to the PL Loop.

Figure 14 shows that the measurement error can also be minimized by decreasing the period of the start pulse. But a decreased start pulse period is directly connected to an increased loss in count rate, especially at higher rates, because the probability for a new start signal to be in between the four stop signals, which belong to one quadruple, increases. In this case the stop signals are measured in respect to different start pulses and the forming of one quadruple is not possible anymore. Therefore it's always necessary to find a compromise between measurement error and the loss in count rate. The start pulse period can be adjusted in the entry field "StartTimer" in the dld_gpx3.ini files (see chapters 3 & 4 in the GUI 4x Manual).

8.7 Interface (PC) and Software

All operation functions of the USB2.0-TDCs for data readout of the detector package are encapsulated in the dynamic linked library "delayline.dll". Data processing and presentation on the PC is realized by an end-user software (e.g. GUI, SpecsLab or Imspector). See the corresponding software manuals for detailed information on the software package and the DLL interface.

9 Dual HV Supply

This device produces lethal high voltage up to +5 kV. Hazardous voltages are present, therefore only persons with the appropriate training are allowed to carry out the installation, adjustment and repair work.

The high voltage for the delayline detector is provided by an external high voltage power supply of the type "Dual HV Supply" which is part of the delivery package. It holds 2 individual high voltage modules (HV 1 & HV 2). Due to an internal resistor network the Dual HV Supply provides four positive high voltages adjustable between +0V and up to +4.0 kV. The HV module HV 1 controls the output voltage for the detector anode (A) in respect to the MCP Front side (F), while the module HV 2 controls the output voltage for the MCP Back side (B) in respect to the MPC Middle contact (M), while the voltage for the MCP Middle contact is related to the voltage of the anode via an internal resistor.

Figure 16: Layout of the Dual HV Supply

1. High voltage turn ON/OFF for HV module 1 (HV 1)
2. Digital display for HV module 1
3. Knob for high voltage adjustment of HV module 1
4. High voltage turn ON/OFF for HV module 2 (HV 2)
5. Digital display for HV module 2
6. Knob for high voltage adjustment of HV module 2
7. Power switch, to turn ON/OFF the power supply (lighted, when set to ON)
8. Power socket

A, B, M, F High voltage outputs via SHV sockets

REF High voltage input for reference voltage of Front side MCP stack (F).

GND Ground connector

Use the 4 SHV cables to connect the outputs of the HV power supply (A, B, M & F in Figure 16) to the corresponding feed-throughs of the delayline detector. Do also use the ground connector of the power supply (GND in Figure 16) to ground the device. Finish the complete cabling, before the device is turned on (no. 7).

Before the high voltage is switched on (no. 1 & 4), make sure that the potentiometer (no. 3 & 6) is turned to the left as maximum possible (zero position of the HV modules) in order to avoid high voltage sparks.

Increase the high voltage very carefully, especially when the detector is used for the first time after installation or has been vented before. Strictly, follow the "Start-Up" procedure described in chapter 11.2.

High voltage sparks may damage the meander or the MCPs seriously.

Do not disconnect the SHV cables, while high voltage is applied to the delayline detector. This also will lead to high voltage sparks within the detector.

Do not open the power supply, while it is in operation. Hazardous voltages are present. In case that the device must be opened, turn off the device first AND pull out the power plug.

9.1.1 Dual HV Supply and MCP Replacement

The Dual HV Supply carries an internal resistor network to separate the four high voltages from the two high voltage modules. This internal resistor network is explicitly optimized to the resistance of the MCP stack of the detector. Therefore a replacement of the MCP can only be made with a MCP stack of the same resistance (exact value is given in the specification sheet) or in combination of a new adjustment of the resistor network of the HV Supply. In any case Surface Concept should be contacted before a replacement is made.

Contact Surface Concept before any replacement of the MCP stack.

9.1.2 Line Input

Electrical Input (LINE):	230 V, 50 Hz
Power:	28 Watt (max.)
Fuse:	1x T 1.6 A

10 Translation/ Rotation Stage

10.1 Setup

The Translation/ Rotation Stage consists of two linear positioner and one rotational positioner on top. The positioners are controlled via a 3 channel control unit. Figure 17 shows an image of the stage together with the movement direction and the movement range of each positioner. The zero position (defined via a reference mark in the positioning readout system) is indicated by the small black line perpendicular to the movement direction. It also gives the allocation of the single positioners to the channel nos. of the control unit. The same allocation can be found on the CF64 flange with the 3x 12pin feed-throughs.

The detector head has an outer diameter of 152 mm, while the vacuum pot has an inner diameter of 200 mm. This allows a maximum range of translation in any direction x, y of 17 mm.

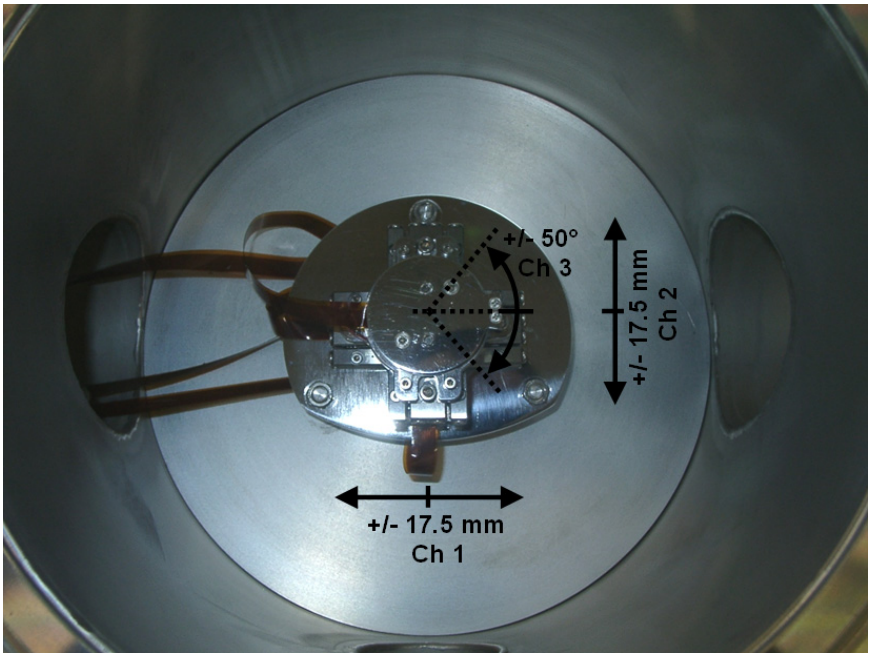


Figure 17: Image of translation/ rotation stack with movement direction, movement range and allocation to the channel nos. of the control unit.

10.2 Operation

There is a separate manual for the translation/ rotation stage within the delivery package. Read this manual, before connecting the stage. Stick to the advices and respect the warnings given within this manual.

11 Operation of the DLD

11.1 Getting Started

- Be sure, that the vacuum pressure at the detector is remarkably below 10^{-6} mbar, otherwise the microchannel plates might be damaged by a local discharging (in general: the lower the pressure, the longer the lifetime of the MCPs).
- Finish the complete cabling as described in chapter 3 and turn on the TDC.
- Start the GUI software and within it the Rate Meter. For details see the GUI software manual.

- Turn off all sources for electrons, ions, light or X-rays that might hit the detector.

The ion-gauge and the gatterpump are both sources for electrons, ions and also X-rays (the gatterpump). They can produce so many particles/ X-rays, that the detector is in a complete overload, even when they are not facing the detector directly. This will wear out the MCPs very fast. Turn off gatterpump and ion-gauge, if they are too close and/or in direct direction to the detector.

- Turn on the high voltage carefully, as described in the following chapter.

11.2 Turning on the High Voltage

High voltage sparks may seriously damage the meander or the MCPs. Observe the chamber pressure carefully every time the high voltage is turned on. Switch off the high voltage immediately in case of a temporary pressure rise by an order of magnitude or more. This indicates high voltage sparking.

If sparking occurs, turn down the high voltage immediately and wait some time (up to 5 min.). Start the "Start-Up" procedure again with an increased ramp time. Is it not be possible to reach the operation voltage without sparking, then turn off the high voltage, stop the procedure and call SURFACE CONCEPT for further assistance.

11.2.1 "Start-Up" Procedure (for new systems and for systems, after being vented)

The first time the detector is used or after the system has been vented, the detector high voltages must be ramped very slowly to the final operation value. The voltage increase should not exceed 100 V per minute.
A schematic sketch on how to ramp the voltages during the "Start-Up" procedure is given in Figure 18.

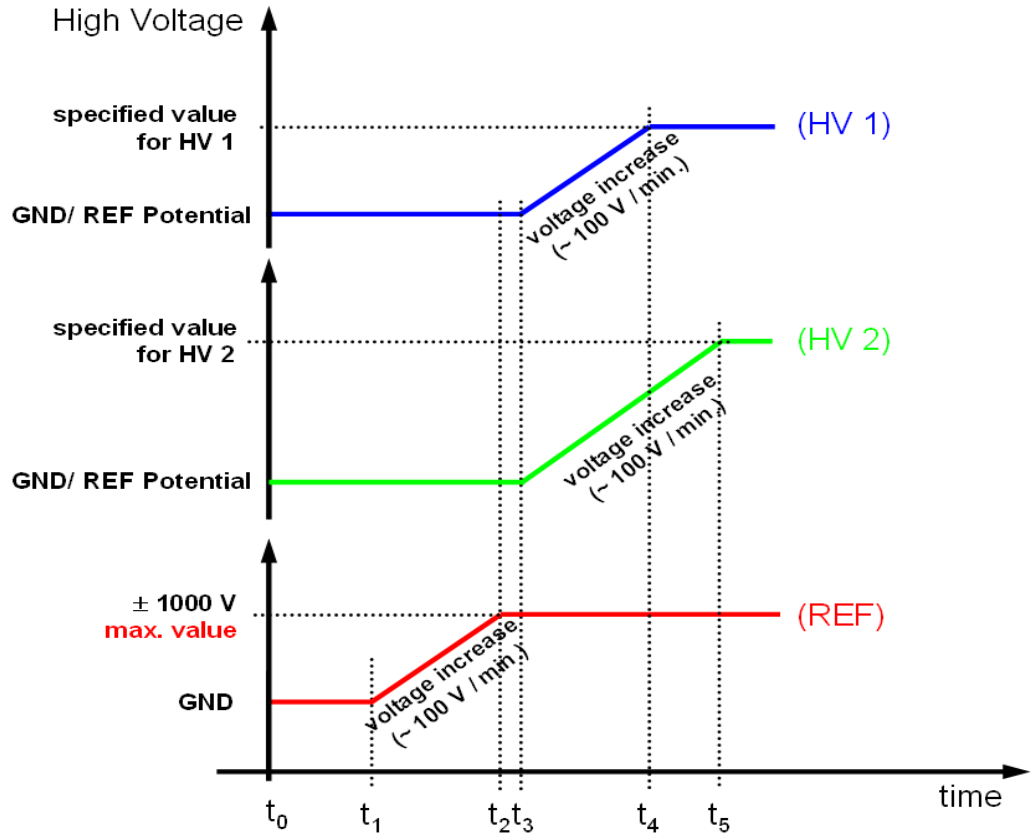


Figure 18: Schematic sketch on voltage ramping during "Start-Up" procedure.

If a reference voltage is applied to the REF input of the Dual HV supply, than first ramp this voltage to a max. value of not more than ± 1000 V. Start to ramp the HV 1 and HV 2 voltage only, after the ramping of the REF voltage has been finished (t3 > t2). Please note that HV 1 and HV 2 must be ramped parallel up to their specified values (see specification sheet for exact values). The ramping of HV 1 and HV 2 can be started directly, when the REF input is grounded.

The analogue readout electronics has been adjusted to an optimized detector voltage. These specified voltages for HV 1 and HV 2 are given in the specification sheet of the detector. There you also find a max. operation voltage. Never exceed this voltage.

Stick to the voltages given in the specification sheet. Contact Surface Concept before any other – especially higher – voltages are applied to the detector.

The max. allowed voltage for REF is ± 1000 V. Connect the termination plug to the REF socket, if no external voltage is applied.

HV 1 and HV 2 must be ramped parallel. A difference of max. ± 200 V between both voltages during ramping is allowed.

Example: A detector should be operated with a REF voltage of +500 V. Therefore a ramp time of 5 min. should be used to change the REF potential from 0 V to +500 V using a separate HV module. After this the HV 1 and HV 2 voltages should be ramped to exemplarily values of +1500 V and + 2100 V. The ramp time should be 15 min. for HV 1 and 21 min. for HV 2 respectively, with increasing both voltages parallel.

- **After high voltage has been applied to the detector, check the detector output by means of the GUI software. The dark count rate without any source should be lower then 20 cps on the entire active detector area.**
- **Now you may start carefully with an electron/ light source observing the detector output.**

Keep in mind the description about the important operation details in chapter 5.4.

11.2.2 Standard Start Procedure

The following procedure is used for all later operation starts, when the detector has already been operated in vacuum and has not been vented in between:

- **Turn off all sources for electrons, ions, light or X-rays that might hit the detector.**

The ion-gauge and the gatterpump are both sources for electrons, ions and also X-rays (the gatterpump). They can produce so many particles/ X-rays, that the detector is in a complete overload, even when they are not facing the detector directly. This will wear out the MCPs very fast. Turn off gatterpump and ion-gauge, if they are too close and/or in direct direction to the detector.

- **Turn up the high voltage carefully and stepwise within 2 or 3 minutes to the operation voltages.**
- **Watch the vacuum pressure during this procedure; turn the voltages back, if an unusual increase is observed in the pressure.**
- **Check the detector output by means of the GUI software. The dark count rate without any source should be lower then 5 cps on the entire active detector area.**
- **Now you may start carefully with an electron source observing the detector output.**

Keep in mind the description about the important operation details in chapter 5.4.

Turn off the high voltage, close the software and turn off the TDC before performing any changes of the cabling.

11.3 Bake Out Procedure

The maximum allowed temperature for the detector is 150°C. Do not exceed this temperature.

- Please read the bake out instruction completely and carefully, before starting the bake out procedure.
- Windows and feed-throughs should be wrapped with aluminum foil, to protect them from rapid temperature changes.
- The use of heating tapes and jackets is not recommended, due to danger of local overheating.
- Do not remove the blankets until the entire system has thoroughly cooled off.
- Do not operate the detector before the temperature has returned to ambient conditions.
- The detector electronics (ACU) must be removed before any bake out.

After a bake out, the detector needs at least half a day (approx. 12 hours) to cool down. If channel plates are operated at higher temperatures (> 50°C) they can suffer damage. Such channel plates will lose gain and exhibit a markedly higher detector plateau.

Even if the detector housing feels just warm, any internal parts seated on insulators (e.g. the meander detector) may still be too hot for safe operation. It is imperative that all users be informed of this issue and take the necessary precaution to ensure proper device operation.

12 Microchannel Plate (MCP)

Contact SURFACE CONCEPT before performing a replacement.

The replacement must go hand in hand with a readjustment of the Dual HV Supply (see chapter 9.1.1 for further details).

Take care to note the orientation of the MCPs. The channels in the MCPs include a certain angle against the surface normal to the plate and the MCPs must be mounted in a chevron or z-stack configuration (depending on no. of MCPs). All parts of the detector, especially the MCPs should be handled with great care. The MCP surfaces are very sensitive and should never be touched or scratched.

12.1 Storage

Because of their structure and the nature of the materials used in manufacture, care must be taken when handling or operating MCPs. The following precautions are strongly recommended:

- The most effective long-term storage environment for an MCP is an oil-free vacuum.

12.2 Handling

- Shipping containers should be opened only under class 100 Laminar flow cleanroom conditions.
- Personnel should always wear clean, talc-free, class 100 clean-room compatible, vinyl gloves when handling MCPs. No physical object should come into contact with the active area of the wafer. The MCP should be handled by its rims, there is no solid glass border! Use clean degassed tools fabricated from stainless steel, Teflon™ or other ultra-high vacuum-compatible materials. Handling MCPs should be limited to trained, experienced personnel.
- MCPs without solid glass border should be handled very carefully with great care taken to contact the outer edges of the plate only.
- The MCP should be protected from exposure to particle contamination. Particles which become affixed to the plate can be removed by using a very pure and low pressure air flow such as from a clean rubber bellows.
- The MCP should be mounted only in fixtures designed for this purpose. Careful note should be

taken of electrical potentials involved.

Voltages must not be applied to the device while at atmospheric pressure. The pressure should be 1 x 10^{-6} mbar or lower at the microchannel plate before applying voltage. Otherwise, damaging ion feedback or electrical breakdown will occur.

12.3 Operation

- A dry-pumped or well-trapped/diffusion-pumped operating environment is desirable. A poor vacuum environment will most likely shorten MCP life or change MCP operating characteristics.
- A pressure of 1 x 10^{-6} mbar or better is preferred. Higher pressure can result in high background noise due to ion feedback.
- When a satisfactory vacuum has been achieved, voltages may be applied. It is recommended that this is done slowly and carefully. If fluctuations do appear, damage or contamination should be suspected and the voltage should be turned off. The assembly should then be inspected before proceeding.
- Voltage across single MCPs should not exceed the max. voltage given in Table 2 and in the specification sheet of the detector. Higher potentials may result in irreversible damage.
- MCPs can be degraded by exposure to various types of hydrocarbon materials which raise the work function of the surface, causing gain degradation.
- Operation at higher temperatures (> 50 °C) will cause gain degradation.

Thickness	1.5 mm
Outer diameter	86,6 mm
Active diameter	80 mm
L/D (channel length / channel diameter)	60 : 1
Resistance (single MCP)	1.6 – 6 MOhms
Max. voltage (single MCP)	1200 V
Max. Gain @ 1200 V	$\geq 1 \cdot 10^{5}$ minimum
Pore size (diameter)	25 µm
Center – to – Center Spacing	32 µm
Bias angle of channels	19° ± 1°
Quality level	detection quality, extended dynamic range
Open area ratio	45 % minimum
Operating pressure	$< 1 \cdot 10^{-6}$ mbar

Table 2: MCP Specifications

13 Technical Data

Delayline detector General:

HV capability:	none
Active area:	∅ 80 mm round separated into 4 quadrants with 40mm x 40mm overall dimension each.
Operation voltage at detector:	see specification sheet
Max. voltage at HV 1:	+ 2900 V
Max. voltage at HV 2:	+ 1400 V
Max. voltage at REF input:	+/- 1000 V
Max. bake-out temperature:	150°C
Vacuum pressure range for operation:	< 10^{-6} mbar

Amplifier – CFD – Unit ACU 3.16.2:

No. of Amplifier-CFD channels:	16
Bandwidth of DLD amplifiers:	1.6 GHz
CFD working frequency:	200 MHz
CFD jitter (max.):	20ps
CFD walk (typ.):	< 50 ps (while ambient temperature varies less then 5 K)

14 List of Figure

EU Declaration of Conformity

Manufacturer **Surface Concept GmbH**
Staudinger Weg 7
D - 55128 Mainz
Germany

CE

Product details Delayline Detector DLD 1D, 2D, 3D, Quadrant in all variations and sizes to be operated with ACU and USB2.0-TDC in all versions and subversions.

The above named products comply with the following European directive:

89/336/EEC	Electromagnetic Compatibility Directive, amended by 91/263/ EEC and 92/31/ EEC and 93/68/EEC
73/23/EEC	Low Voltage Equipment Directive, amended by 93/68/EEC

The compliance of the above named product to which this declaration relates are in conformity with the following standards or other normative documents where relevant:

EN 50081-1 (3/94)	Electromagnetic Compatibility Generic Emission Standard-Part 1:
EN50082-1 (3/94)	Electromagnetic Compatibility
EN 61010-1 (2001)	Safety Requirements for Electrical Equipment for Measurement, Control and Laboratory Use

For and on behalf of **Surface Concept GmbH**

SURFACE CONCEPT
Surface Concept GmbH,
Staudingerweg 7, 55128 Mainz

Mainz, 28.02.2008 Legal signature .....
(date) (Dr. Andreas Oelsner – Managing Director)

This declaration does not represent a commitment to features or capabilities of the instrument. The safety notes and regulations given in the product related documentation must be observed at all times.

EU Declaration of Conformity

Manufacturer **Surface Concept GmbH**
Staudinger Weg 7
D - 55128 Mainz
Germany

CE

Product details High voltage power supplies “Single HV Supply” and “Dual HV Supply”

The above named products comply with the following European directive:

89/336/EEC	Electromagnetic Compatibility Directive, amended by 91/263/ EEC and 92/31/ EEC and 93/68/EEC
73/23/EEC	Low Voltage Equipment Directive, amended by 93/68/EEC

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