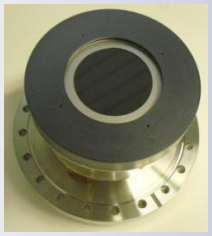
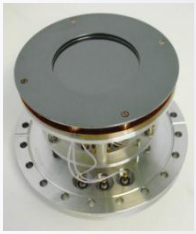
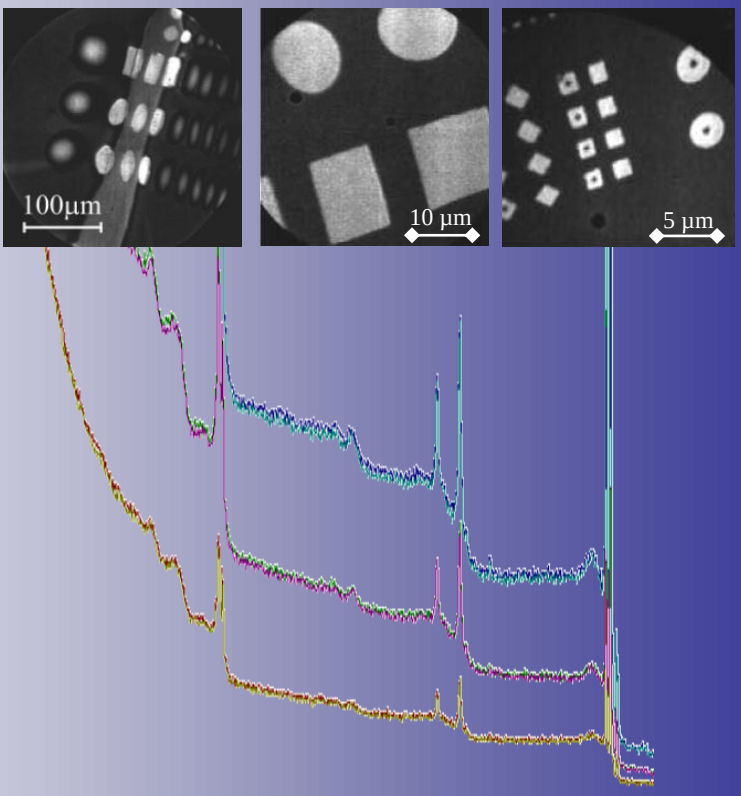
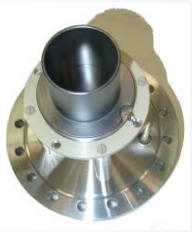
# Surface Concept
# Delayline Detectors

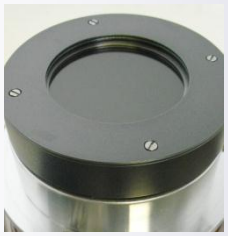
## Catalogue 2011

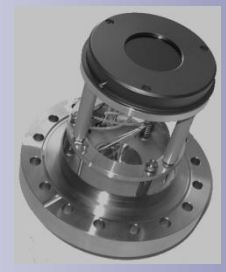










SURFACE CONCEPT

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Printed version: 11.2011

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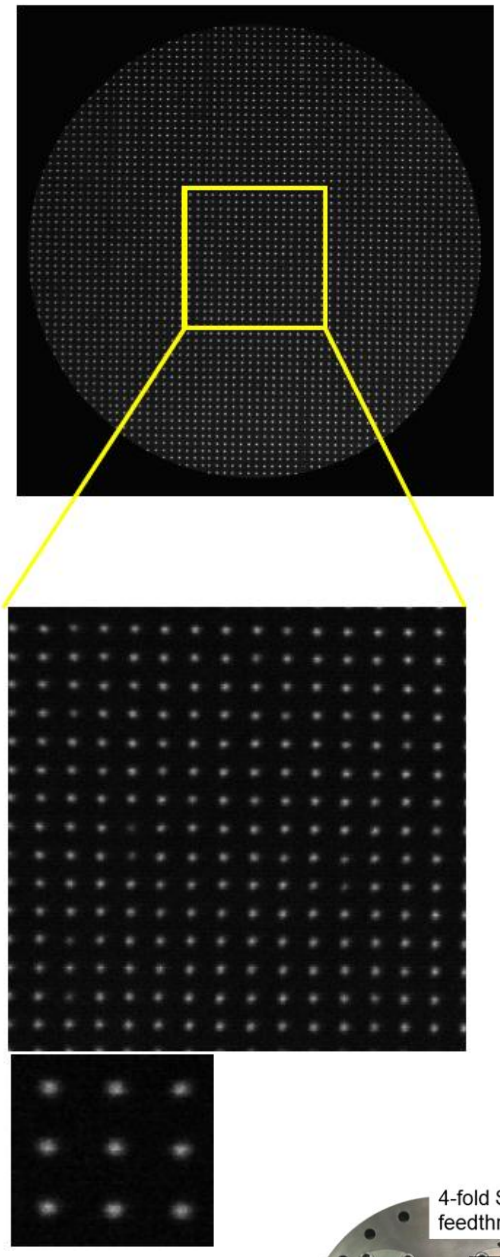
# Get the future‘s detector already today

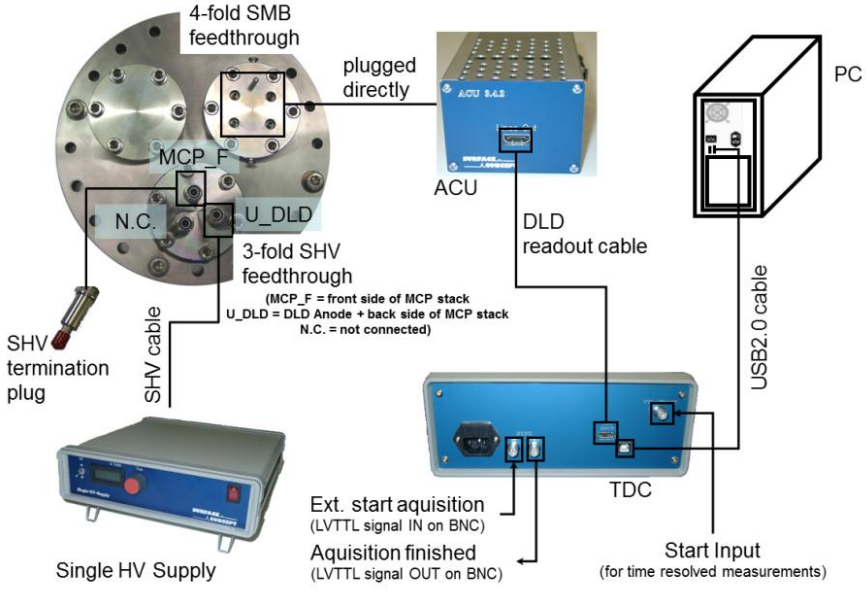


## 3D-DLDs and 1D-DLDs:

- Very High Count rates
- True Counting
- No Readout Noise
- Superior Single Counting Capability
- Extremly High Countrate Linearity
- Pico Second Time Resolution
- Very Small Dead Times
- Fast Scanning Support
- Synchronized High Speed Camera Mode (up to >100000 frames per second)
- Optimized Pulse Pattern Synchronization
- High Pixel Number (up to 8k x 8k for large detectors)
- High Voltage Versions (up to 20kV floating)

## 4Q-DLDs:

- Extreme High Burst rates (>100MCPS)
- High Multi-hit capability
- Fully Independent Sub-Area Read-Outs
- Small Dead Times
- Customizable Sizes
- Customizable Sub-Areas
- Extreme Wide Dynamic Range
- No Read Out Noise
- Large Areas
- High Resolution
- Software Interface Support
- Adapted Calibrations



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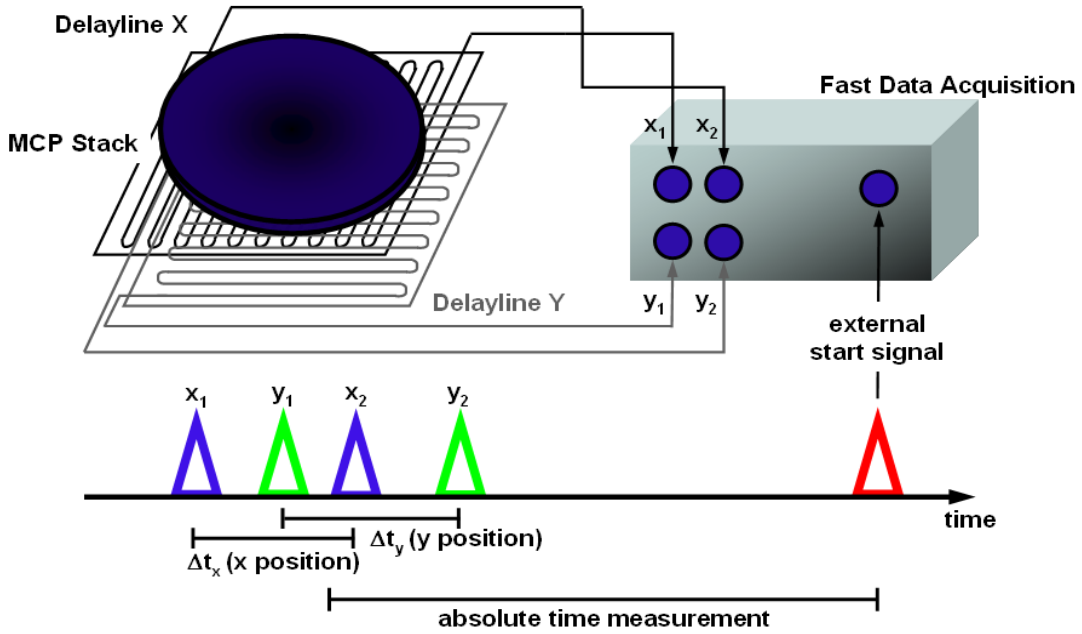
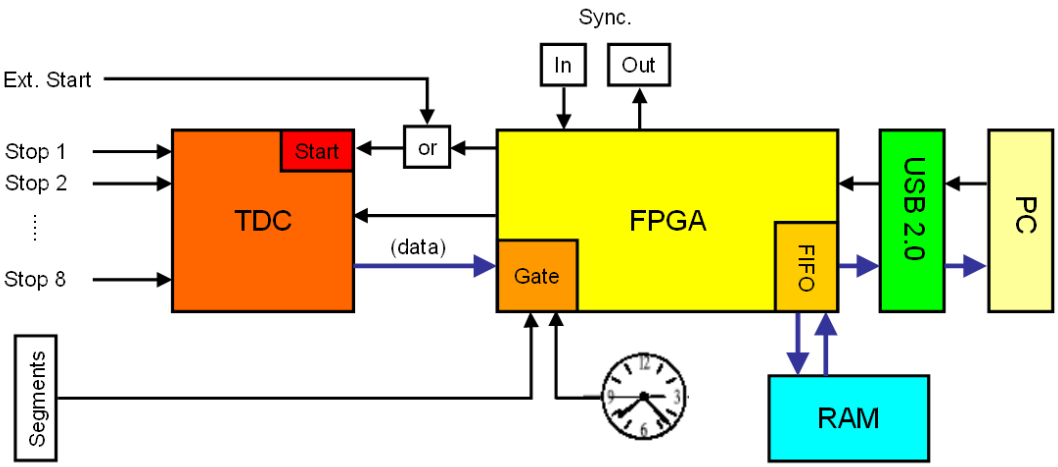
# DLD – principle of operation




The DLD anode consists basically of two flat serpentine-like wire arrangements (meanders); one below the other, rotated by 90°, close together, but insulated. This stack is positioned behind a Chevron micro-channel plate stack for electron amplification. The electron cloud hit from the MCP stack output couples into the meanders where it induces electrical pulse groups traveling to the wire ends within a time determined by the hitting position. Time measurement therefore allows reconstructing the hitting position. The detector enables absolute time measurements with respect to an external start signal. This is derived from the average time at both coil ends in relation to an external repetitive clock signal.




Pulse readout is realized by a fast analog electronics and a time measurement unit (TDC = time to digital converter). A field programmable gate array (FPGA) within the TDC enables comfortable setups and a variable data stream handling from the TDC via USB 2.0.
The main delayline detector and segment readout (optional device) functionality is permanently programmed. A complex FIFO design makes data losses almost impossible. The user DLL controls the data handling and streaming for the user.



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# New Meander Technology

In 2008, Surface Concept introduced new meander structured delaylines to replacing the traditional wire coils. The new lithographically produced meander delaylines hold serveral benefits in comparison to the wire coils delaylines such as:

- much higher mechanical stability
- device matched close to 50 Ohm
- coaxial cables in vacuum for signal transfer
- 2x shorter pulse traveling time
- far higher max. count rates

The new meander delayline sets the new standard for all our delayline detectors.

# Typical Delivery Package for DLDs

- DLD with MCP stack mounted in housing on conflat flange
- Pulse processing unit with preamplifiers and constant fraction discriminators (CFD) tuned individually for the delivered detector
- Time to Digital Converter (TDC) with free programmable gate array logic (FPGA) and USB 2.0 interface tuned up for the delivered detector
- High voltage power supply
- All needed connection cables
- Windows® DLL with interface discription
- Stand alone image acquisition software for monitoring and histogramming
- Transport vacuum-housing for delivery and storage of UHV part

On request:

- LabView™ VI set optional available
- 64 bit software will be available during the first half year of 2012, which will be compatible with all older DLDs since 2009 production date



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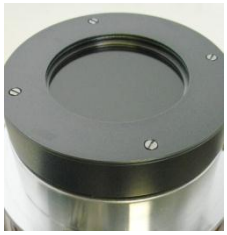
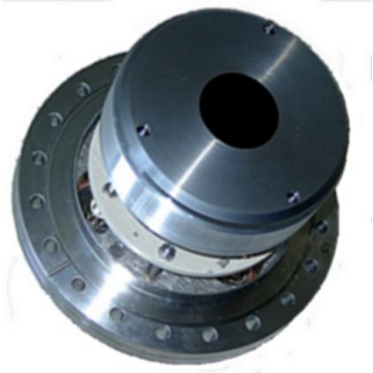
# DLD 3030 / 3636 / 4040

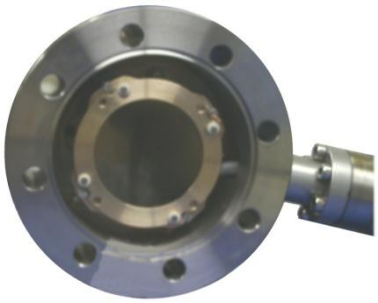
## Small area Delayline Detectors (2D(x,y); 3D(x,y,t))



DLD4040



DLD3636



## Features

- 2D(x,y)/ 3D(x,y,t) detector
- CF150 mounting flange
- typ. active areas[1]: ∅30mm / 36x36mm² / 40x40mm²
- active MCP area: ∅ 48mm (max.)
- typ. image sizes in pixels: 400x500 / 700x850 / 900x1100 (higher values possible as custom specific layouts)
- typ. time resolution: ≤ 240ps absolute, ≤ 100ps relative
- linear response due to single event counting[2]
- extremely low dark count rate: ≤ 5 cps (under UHV conditions)
- up to 8 million counts per second random hits in 2D/ 3D mode

*[1] The active area of a DLD is the intersection of the rectangular active area of the wire coils/ meander and the round active area of the MCP stack. Depending on these both areas, the active detector area can be round, rectangular or rectangular with rounded edges.*

*[2] The linear response is accurately valid for small count rates. The detector response loses its linearity with increasing count rate due to typ. deadtimes between 20ns and 100ns, but can be restored by software corrections.*



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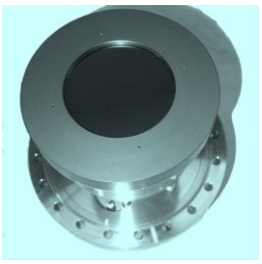
# DLD 6565 / 8080 / 120120

## Large area Delayline Detectors (2D(x,y); 3D(x,y,t))

DLD6565



DLD8080

DLD120120

## Features

- 2D(x,y)/ 3D(x,y,t) detector
- CF150 mounting flange
- typ. active areas[1]: 65x65mm² / 80x80mm²
- active MCP area: ∅ 80mm (max.)
- typ. image sizes in pixels: 2000x2200 / 3000x3400 / 6000x7000
- typ. time resolution: ≤ 240ps absolute, ≤ 100ps relative
- linear response due to single event counting[2]
- extremely low dark count rate: ≤ 5 cps (under UHV conditions)
- up to 5 million counts per second random hits in 2D/ 3D mode

[1,2] see page 7 for detail



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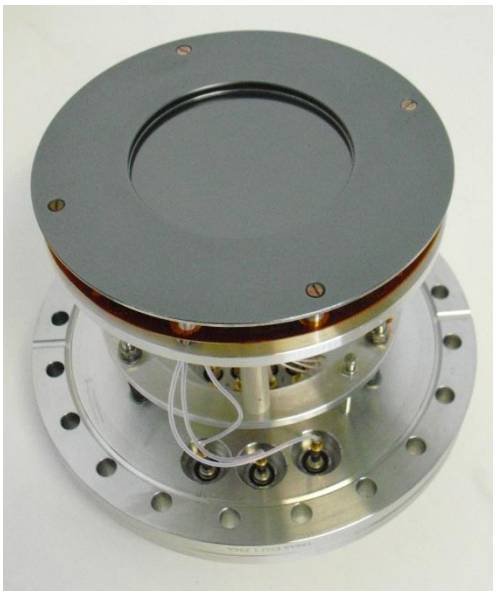
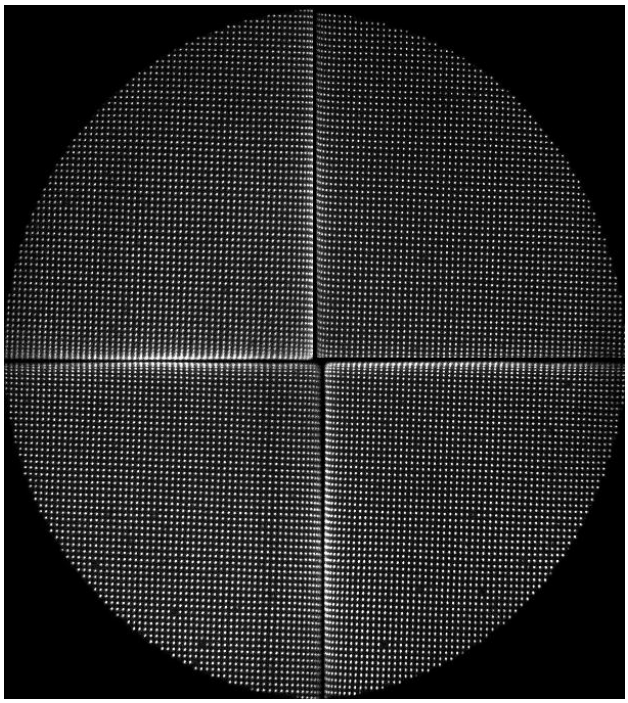
# DLD3030-4Q / DLD4040-4Q

## 4 Quadrant multi-hit delayline detector for fast burst imaging (2D(x,y); 3D(x,y,t))

- ***Renewed realization of Surface Concept's patented multi-anode DLD layout***
- ***Multi-hit 4 fold detector optimized for fast burst recognition above 100 MCPS equiv.***
- ***Large detection area up to 60 mm x 60 mm (60 mm x 30 mm used in PHOIBOS 225)***
- ***Real parallel detection of 4 hits without any dead time due to the fourfold design***
- ***Multi hits on single quadrants (all 10 ns possible) are always unambiguous, no data redundancy problems due to the short single delays of about 9 ns.***





## Features

- Multi-hit 2D/3D 4-fold delayline detector
- Up to 4 multi hits with absolutely zero dead time
- Up to 400 multi hits per 1 µs
- Burst rates above 100 MCPS equivalent rate
- 60 x 60 mm² (or 80 x 80 mm²) active area of DLD body and ∅ 82 mm active MCP area
- Down to 30 µm of pixel size
- < 250 ps over all time resolution
- Linear response due to single event counting
- Extremely low dark count rate: ≤ 0.2 cps/ cm²
- Up to 40 MCPS permanent count rate in 2D/3D mode

[1,2] see page 7 for detail



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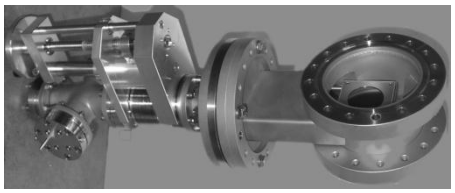
# DLD 1818 IC – 4040 IC

Interchangeable-in-UHV Delayline Detectors
(2D(x,y); 3D(x,y,t))



DLD4040 IC

## Features

- 2D(x,y)/ 3D(x,y,t) detector
- CF63 mounting flange
- Interchangeable system for in-situ change of DLD position, e.g. for electron/ ion optics front-ends
- typ. active areas[1]: ∅18mm - ∅40mm
- active MCP area: ∅ 46mm (max.)
- typ. image sizes in pixels: 200x250 - 900x1100
- typ. time resolution: ≤ 240ps absolute, ≤ 100ps relative
- linear response due to single event counting[2]
- extremely low dark count rate: ≤ 5 cps (under UHV conditions)
- up to 8 million counts per second random hits in 2D/ 3D mode

[1,2] see page 7 for detail



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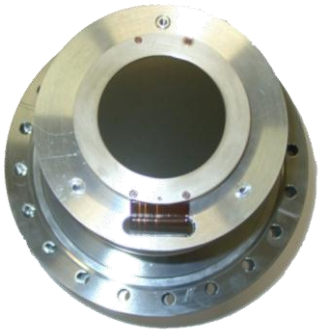
# 1D DLD 18 / 43 / 64 / 64-2

Multichannel Delayline Detectors (1D(x); 2D(x,t))



1D DLD 64

1D DLD 43

## Features

- 1D(x)/ 2D(x,t) delayline line detector
- CF150 mounting flange
- typ. active detection length: 18mm / 43mm / 64mm
- detection width (nonresolving): 15mm / 20mm / 20mm
- typ. no. of lines: 40 / 215 / 320 (higher values up to 2000 channels as custom specific layouts possible)
- typ. time resolution: ≤ 240ps absolute, ≤ 100ps relative
- linear response due to single event counting[2]
- extremely low dark count rate: ≤ 5 cps (under UHV conditions)
- up to 6 million counts per second random hits (DLD43, DLD64)
- up to 15 million counts per second random hits (DLD64-2)

[1,2] see page 7 for detail



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# Optional Packages

In addition, we offer for all Delayline Detectors optional setup packages for extented time measurement ranges, improved time resolution, and multi-hit recognition. A virtual segmentation readout is possible for spectroscopy applications, which enables higher countrate recognition. The high voltage option enables floating operation of the detector head up to 20kV.

## Multimode Virtual Segment Package

The countrate limits of a delayline detector can be remarkably enhanced when it works in a virtual segmant mode. Up to 8 segments can be read in spectroscopy applications as a software switchable mode. The virtual segment mode enables to operate up to 10 million counts per second random permanent with 8 energy channels distributed along one DLD dimension.

## Enhanced Time Resolution Package

Individual optimization of the readout electronics to improve the absolute time resolution from ≤ 240ps to ≤ 150ps and the relative time resolution from < 100ps to < 30 ps.



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# Optional Packages

## Multiple Hit Package

### Not in combination with the High Resolution Package

FPGA assisted double hit option

- 7 ns minimum pulse distance
- available for all DLD packages without changing of vacuum parts
- restricts max. count rate to 1.5 MHz
- multiple hits > 2 available, restricts further max. count rate

## Extented Time Range Package

Individual optimization of the time measurement range from 40µs to a few milliseconds or even seconds. This may be needed for ion time-of-flight applications in particular.


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# Custom Designed DLDs

Surface Concept is an expert in custom designed delayline detectors. We build all parts of delayline detectors (active areas, housings, mounting flanges) adapted to the customer's application.

Some of our custom designed detectors out of the last years:

- DLD 120120
  - active area: 120x120mm²
- special sized DLD 1818
  - active area: ∅18mm
  - CF40 mounting flange
  - also with interchangable system
- DLD4242H9
  - hybrid design of a DLD and a 9-segment-detector
  - active area: 42x42mm²
- High Voltage (HV)DLDs
  - base potential of up to -20kV
- HV DLD/ MircoMott Detector Combination
  - HV DLD combined with a micromott detector
  - base potential up to -12kV
- DLD3030-4quad
  - 4-Quadrant Delayline Detector for multiple hit detection
  - active area: ∅80mm (4x 30mm x 30mm)
- Encapsulated X-Ray DLDs and EUV DLDs












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# Results / Applications

Results / Applications with Delayline Detectors.

## Spatial Resolution

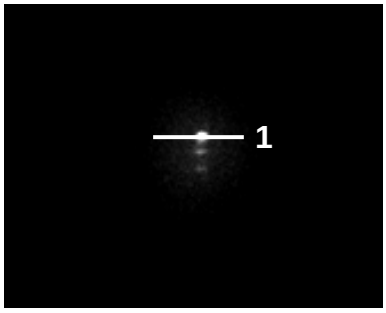
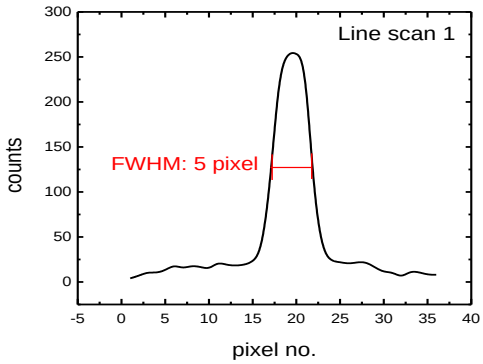



Figure 1



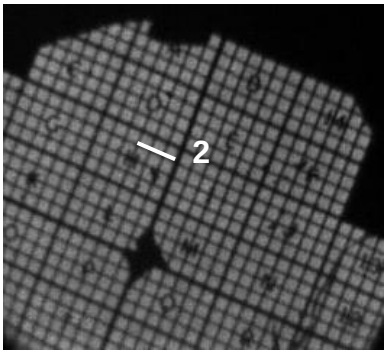
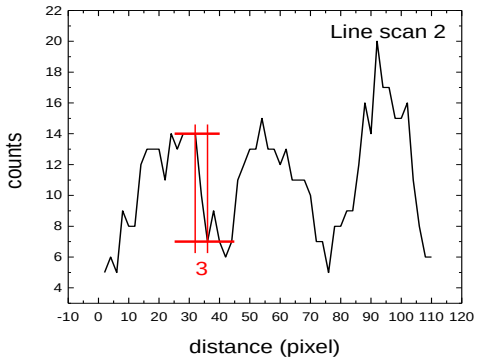




Figure 2




## Time Resolution

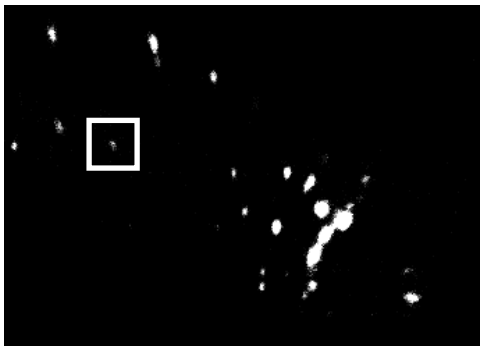


Figure 3

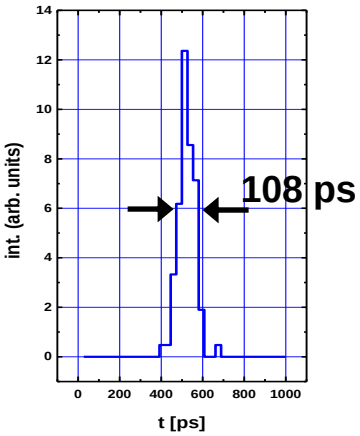



*Figure 1: Image taken with the DLD exposed to a focused blue pulsed diode laser with 408 nm wavelength as well as a line scan deduced from the DLD image along line 1 (note: vertical weak spots are due to laser reflection at window).*
*Figure 2: DLD image taken with a shadow mask exposed to a TiSa fs-laser with 400 nm wavelength and a line scan deduced from the DLD image along line 2.*
*Figure 3: Sum image of image series in time and time histogram, extracted from marked (white) area of interest (AoI) (measured with DLD4242 optimized for improved time resolution).*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# Applications

## Imaging with the DLD (meander type)

Imaging with the DLD (meander type)

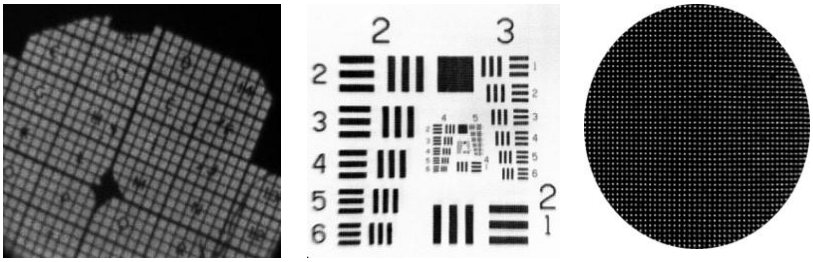


Figure 4

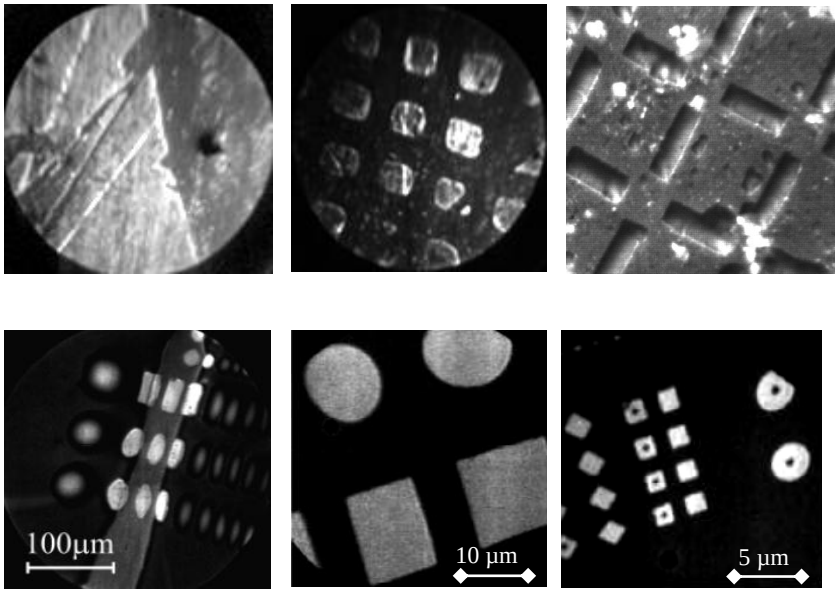


Figure 5

*Figure 4: Imaging of shadow masks with UV light excitation.*
*Figure 5: Photoemission electron microscope image of different samples.*



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# Applications

**Delayline detectors are true counting, imaging particle detectors with time resolution:**
- time slice images can be taken with time windowing down to below 100 ps
- true single counting system, thus high linearity in hit rate response
- brilliant signal / background ratio and very high sensitivity

**Applications:**
- time of flight analysis for electrons and ions
- time correlated or coincidence photon and particle imaging
- gated imaging and spectroscopy tasks for X-ray spectroscopy, electron spectroscopy
- true counting imaging tasks with large areas up to 120 mm detection size

**Methods and instruments equipped with delay line detectors:**
- in electron energy analyzers and time of flight analyzers (XPS, UPS, EELS)
- in photoemission electron microscopy (time-of-flight PEEM)
- in medium energy ion scattering (MEIS with time of flight analysis)
- in atom probe tomography/microscopy (APT, 3D-AP)
- in X-ray absorption-emission spectroscopy (XAS, XES)
- in X-ray pico-second imaging by means of time gating for contrast enhancement
- in fluorescence lifetime imaging (FLIM, FLIM-FRET)
- in ion mass spectroscopy methods (MALDI-TOF, TOF-SIMS, FRES, COLTRIMS)
- in low energy electron diffraction (LEED, femto-Ampere-LEED)
- in imaging of ultra-cold quantum gases in expansion, operates in intense burst mode

## Time Resolved Imaging

Time Resolved Imaging

### Time-of-flight spectromicroscopy as chromatic selector

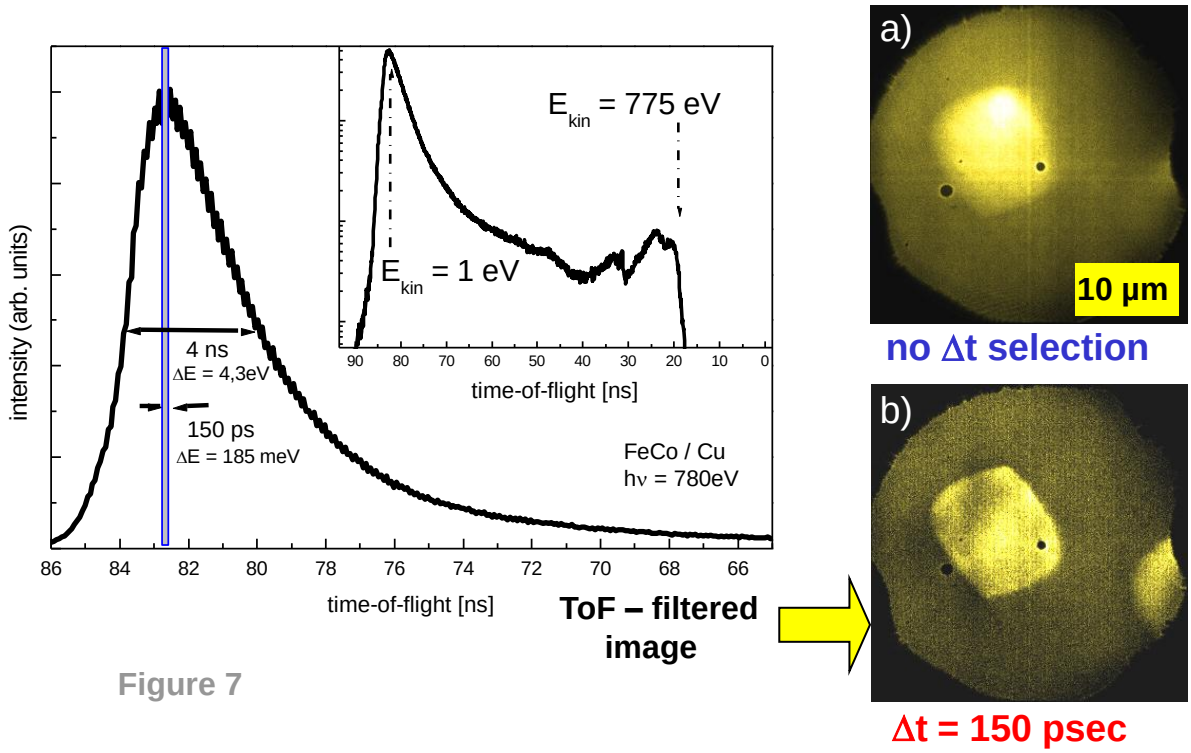


Figure 7

*Figure 7: Time histogram of a ToF spectromicroscopy measurement. A time filtered image (b) shows a significant reduction in the chromatic aberration, compared to a non time filtered image (a).*


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# Applications

## Testing the pulse response of a wire junction at a micro-chip surface (die):

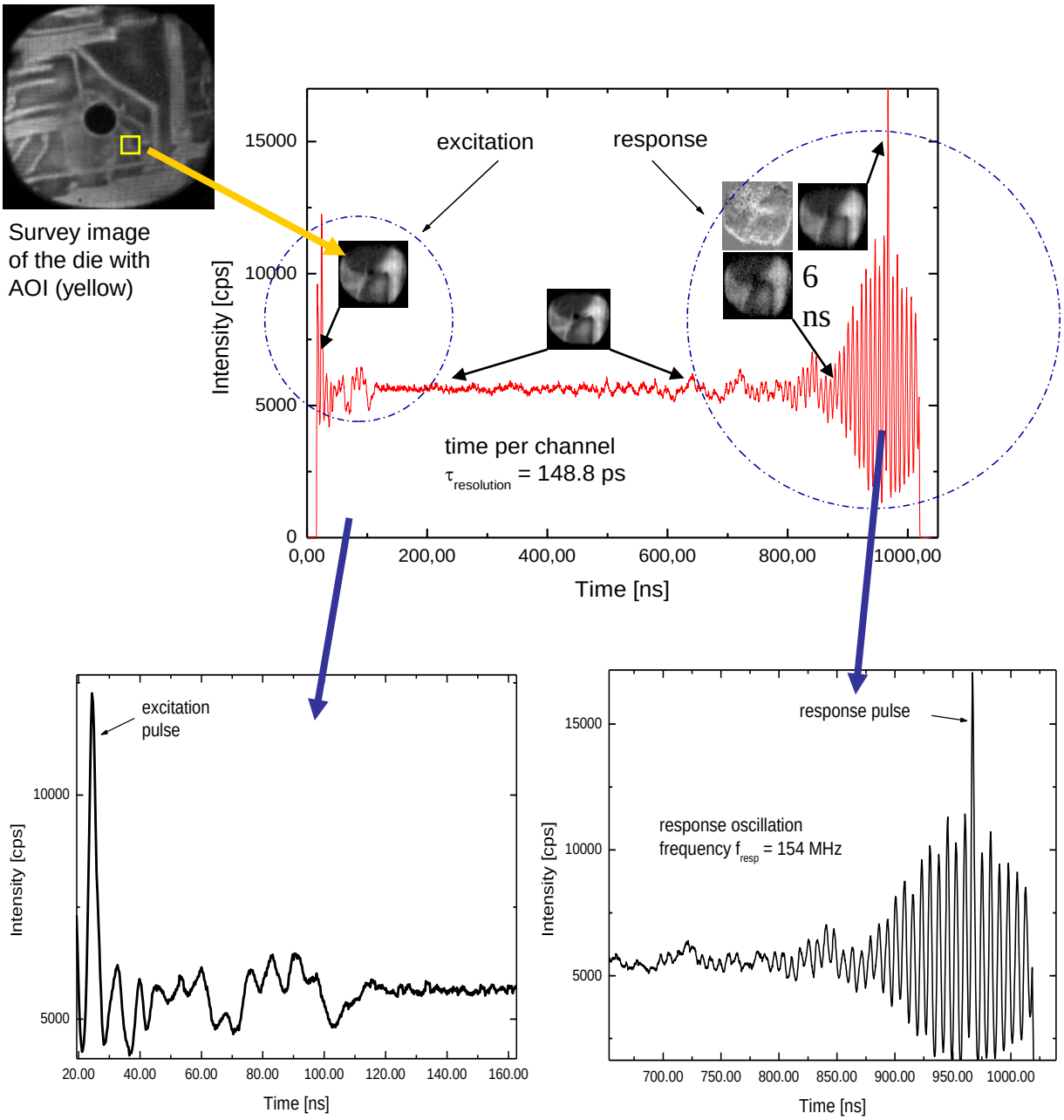


Figure 8

*Figure 8: While a small voltage pulse is electrically coupled into the die, a photoemission electron microscpe observes a certain area of interest (AoI) at its surface. The photoelectron excitation has been chosen continuously using a Hg-lamp. All measurements at the delayline detector are referenced with respect to the initial pulses. The 3D-detector signal responds with small changes in the 3D histogram of data, visualized in spatialy resolved images. The time variation of a small 2D-cut in space is shown directly at an electrical junction within the circuit. The initial pulse as well as the circuit response at this position are clearly seen in the data set.*



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## Hemispherical Analyzer Measurements

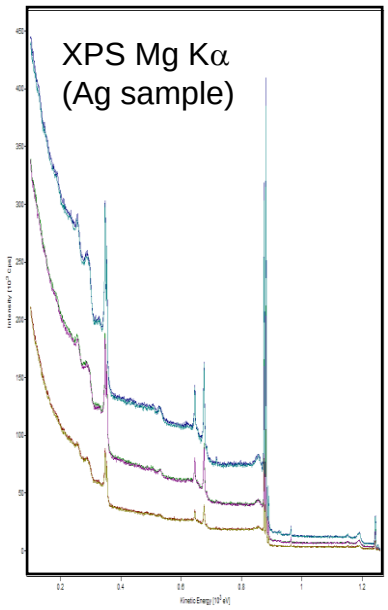



Figure 9

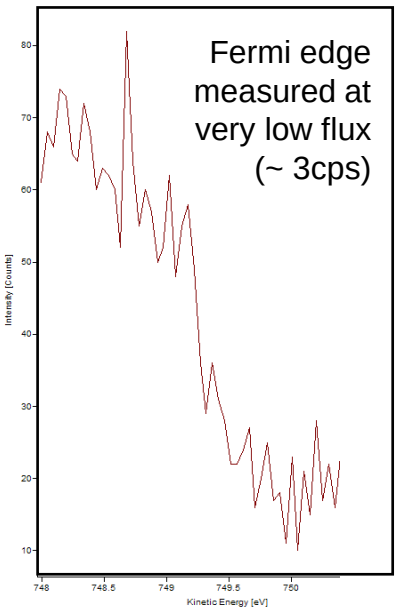
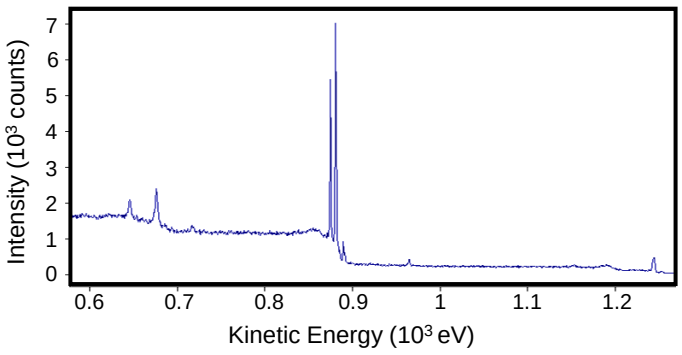



Figure 10

## XPS Measurements with Multichannel DLD




**XPS snapshot**

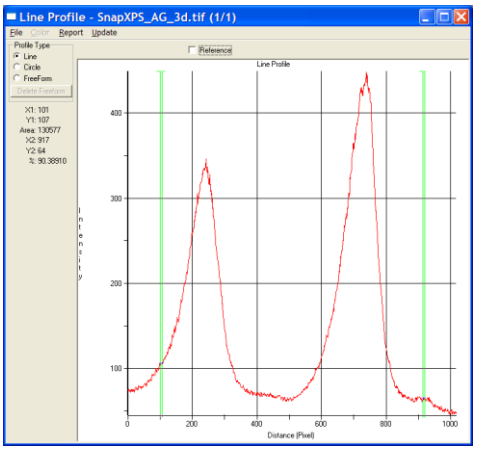



Figure 11

*Figure 9: XPS at Ag with Mg-K alpha and DLD. Epass 10 eV, 15 eV, 20 eV.*
*Figure 10: XPS of a Fermi edge at 3 CPS with the DLD, possible due to the outstanding signal/ background ratio of the DLD.*
*Figure 11: XPS of the Ag3d, taken with the Multichannel DLD.*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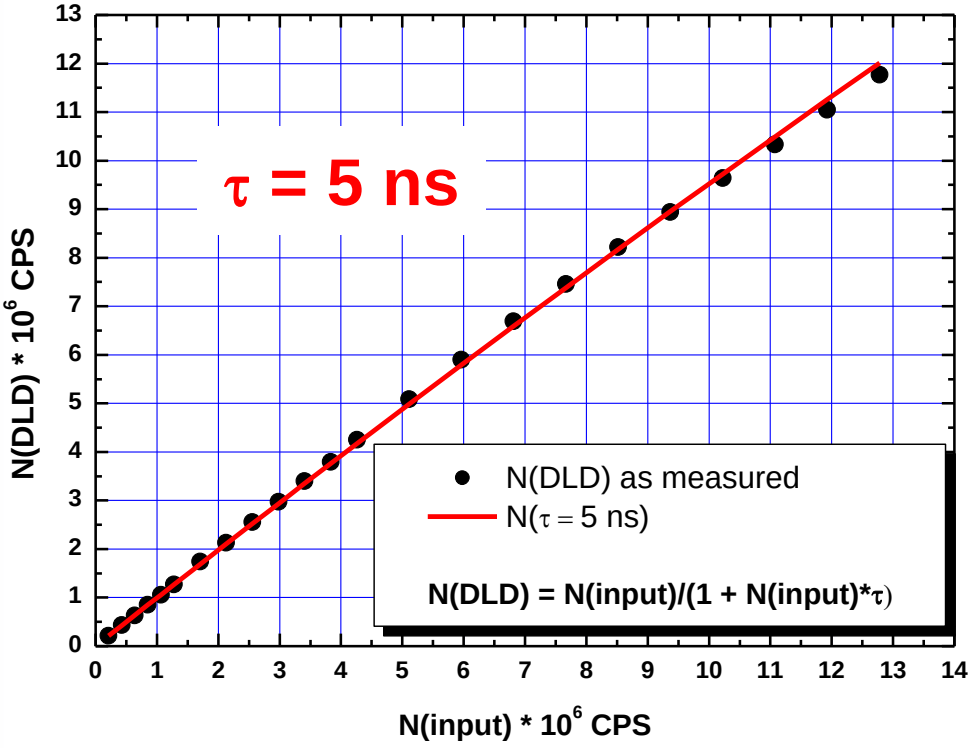
# Applications

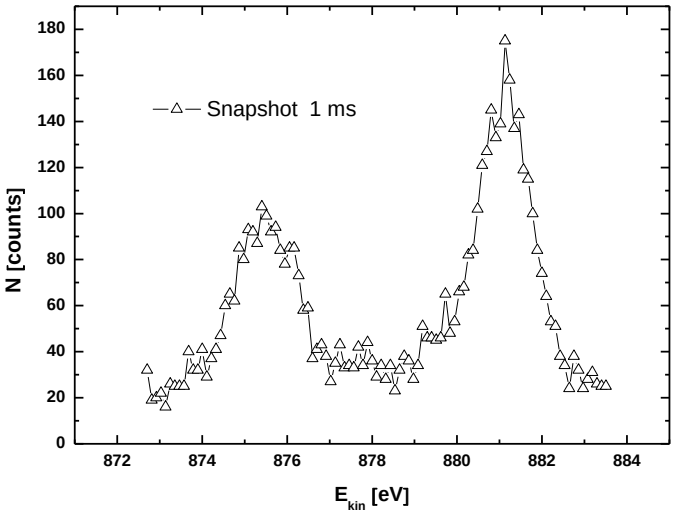
## Hemispherical Analyzer Measurements

Hemispherical Analyzer Measurements

### Dead-time of 1D DLD 64-2 system




### Short snap-shot performance



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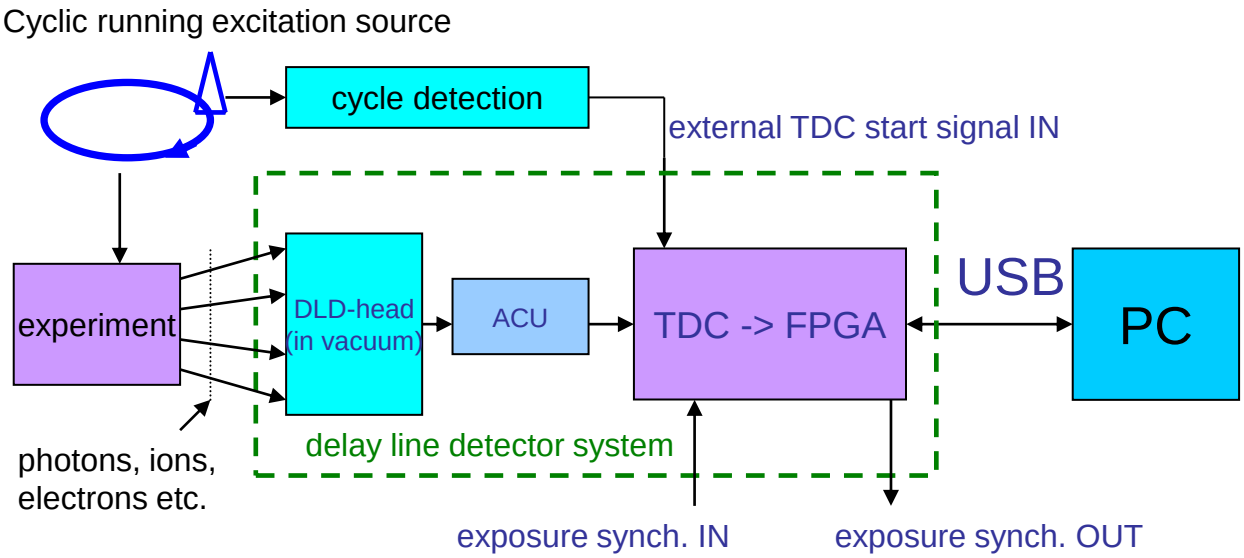
# Delay line detector data acquisition




ACU: fast pulse processing electronics
TDC: time-to-digital converter
FPGA: field programmable gate array
DLD: delay line detector for subsequent single particle detection (x,y,t)

***Features:***

- ***Unlimited dead-time free snapshots synchronized by hardware and streamed over USB***
- ***Flexible excitation bunch data selections and time tagging features,***
- ***Live observation of multiple images selected by time range***
- ***Live image monitoring and parallel listmode file savings for each detector event as x, y, t coordinate set***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