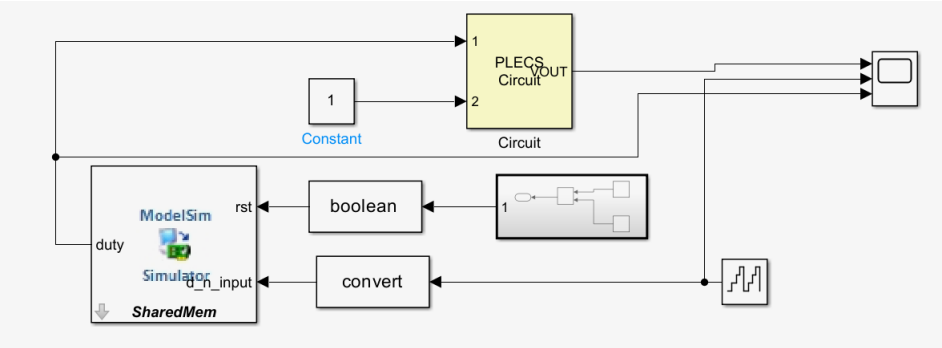
Realization of DPWM Report

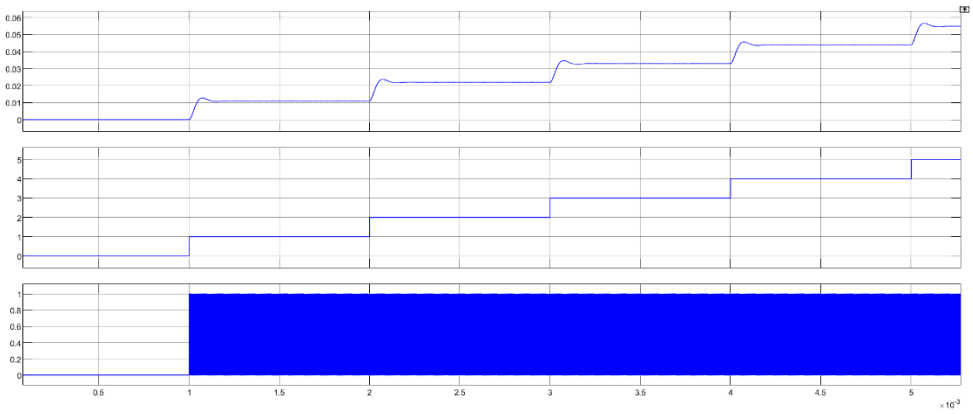
1. System

A. This system also uses Simulink and ModelSim for co-simulation. The figure below shows the block diagram of this system, where the comparator inside PLECS is replaced with the output result of digital circuits. The open-loop behavior of the 9-bit counter DPWM is simulated. By using Verilog to model the digital circuit behavior, the impacts and differences of three DPWM methods—**Counter DPWM, Hybrid DPWM, and Dither DPWM**—on the system are observed. The counter free-running is set to 9 bits, and the sample time is set to 1e-3 as provided in the handout.



2. Counter DPWM

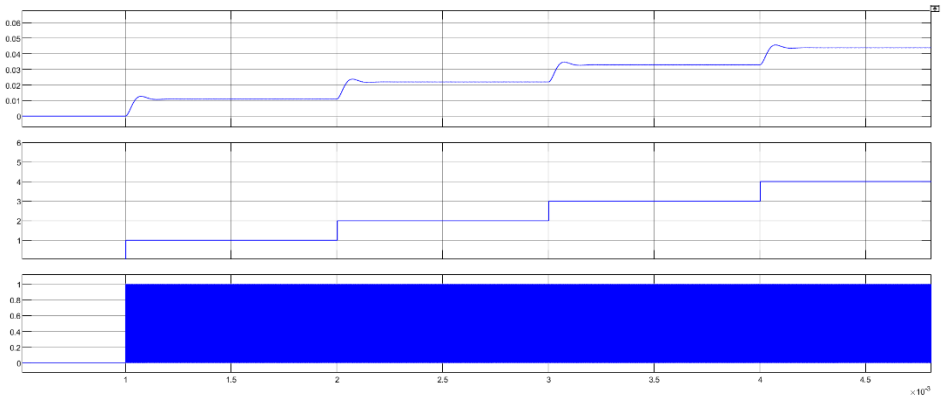
A. Implemented through counterbase.v. In this design, both d_n_input and count are set to 9 bits, and the counter resets to zero when overflow occurs. During co-simulation, since DPWM is 9 bits, the duty sample frequency is set to 2^9 * 500k, and the clock (clk) is also set to 2^9 * 500k.



B. As seen in the waveform diagram above, the output voltage vo increases with the rise of the digital circuit voltage, oscillating according to the duty. The simulation results match the expected behavior.

3. **Hybrid DPWM**

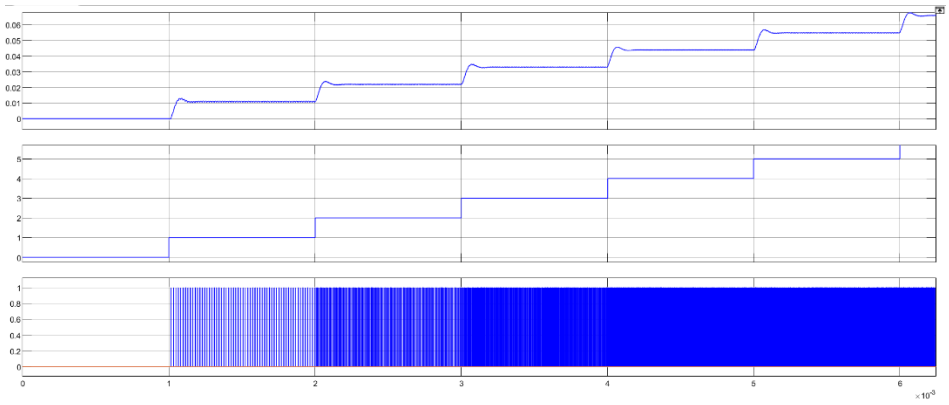
   A. The original 9-bit counter DPWM is split into a 6-bit counter plus a 3-bit delay line. Since the counter is reduced to 6 bits, the clock frequency is adjusted to 2^6 * 500k.



   B. During simulation, a duty period of 4e-9 caused the circuit to miss voltage changes, so it was modified to 2e-9. As seen in the waveform diagram above, the output voltage Vo increases with the digital circuit voltage and oscillates with the duty. The simulation results are as expected.

4. **Dither DPWM**

   A. In this design, the table-based output generates ditherin. Overflow handling must be addressed. Thus, the condition inside the if statement resets to zero when count = 3'b111.

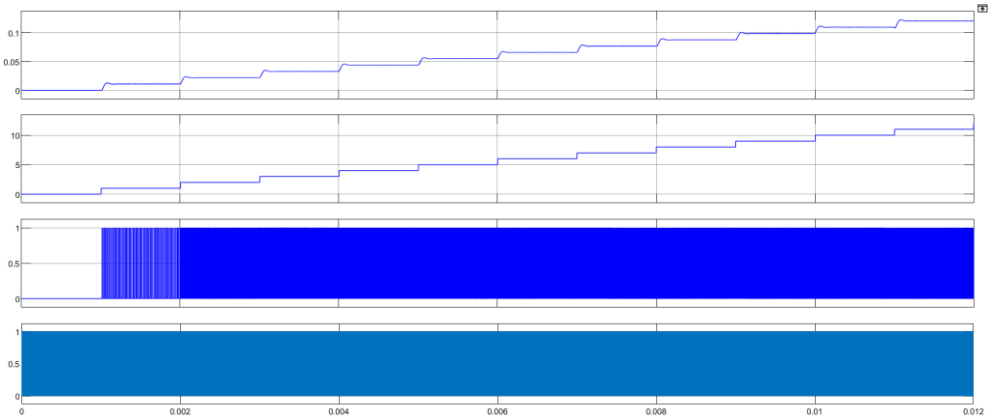


   B. The co-simulation setup is the same as earlier cases. Observation of the waveform diagram also confirms that the simulation results meet expectations.

5. **Dither DPWM with Dead-Time**

   A. After adding dead-time, the counter module in the top file is replaced with a dead-time module. duty_high and duty_low are used instead of the original

duty function, with their sample time set to 2e-9.



B. Because two MOSFETs are operated separately, the NOT logic gate in PLECS can be removed. The rest of the configuration remains the same.

C. From the waveform results, it is observed that duty_high and duty_low switch between each other, ensuring only one MOSFET is on at a time. The final output vo matches the expected performance.

6. **Submission Materials**

A. Lab report document (Lab4_StudentID.docx)

B. Verilog file (.v)