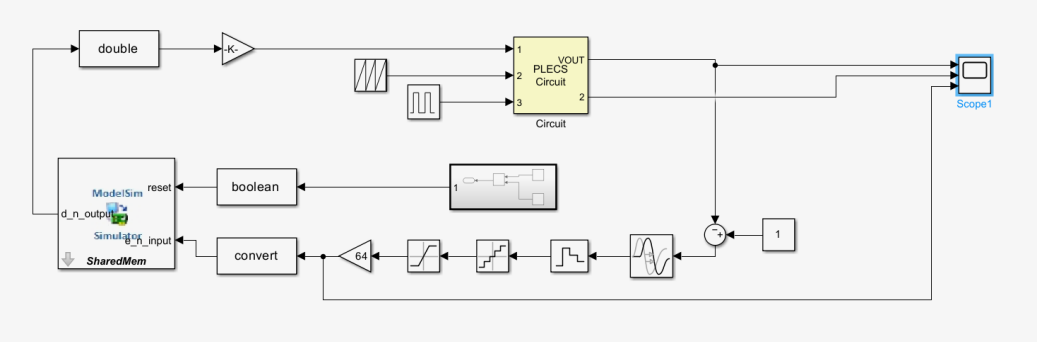
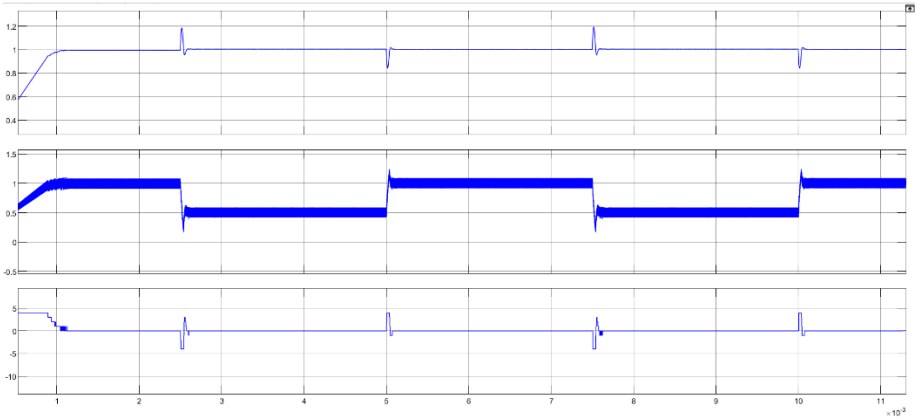
Digital PID Compensator Implement Report

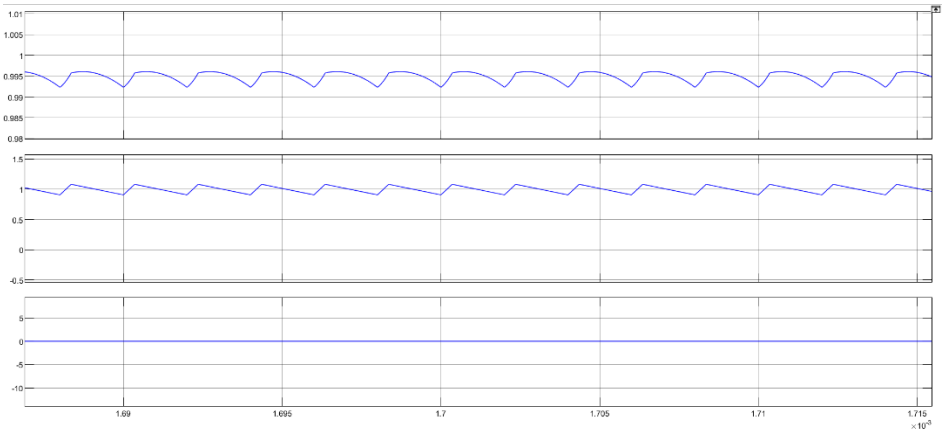
1. Digital Compensator Quantization
   A. The digital compensator implemented should be quantized so that it can be realized in hardware. By decomposing each coefficient of the compensator, the number of bits required for both integer and fractional parts is determined. The maximum value among them decides how many bits are required for LUT conversion. According to the program results, a 16-bit LUT is sufficient to meet the required specifications without distortion during conversion, while ensuring enough precision.
2. Digital Compensator Hardware Description Language Implementation
   A. Using the program generated in MATLAB, the coefficients a, b, and c are converted into binary representation. The corresponding LUT values are then filled into the program. The code is based on the example provided in the handout, with adjustments to the number of truncated bits. By discarding the last 7 bits, the output is maintained at 9 bits, and d_n_output is declared as an output.
3. Buck Converter Closed-Loop Simulation (including power stage, PWM, and compensator)
   A. The figure below shows the Simulink architecture of the system, based on the implementation provided in the handout. Using co-Simulink, the Verilog model of the designed code is integrated into the system. The DPWM and ADC are designed with 6 bits and 8 bits, respectively, consistent with Digitally Controlled Buck Converter. The sample time is set to 2e-6.



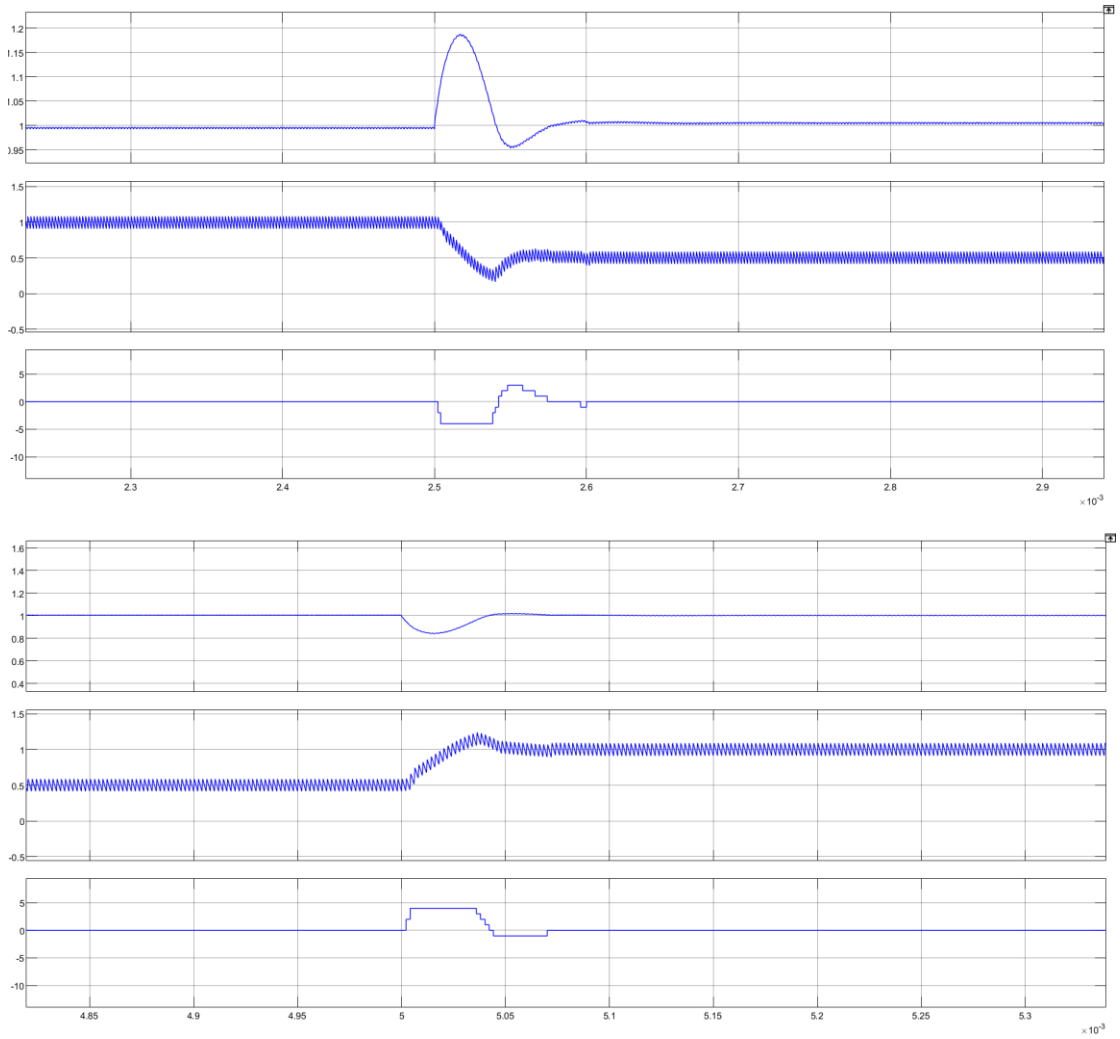
B. The simulation results (shown below) demonstrate that under heavy load, the output voltage stabilizes at 1V and the current oscillates around 1A. The transient response during load switching meets the specifications required in this Lab.



C. In steady-state, the results are consistent with the digital circuit simulation (without quantized LUT implementation). The quantization has only a negligible effect on the compensator.



D. The two figures below illustrate switching between heavy load and light load, showing results identical to those in Digitally Controlled Buck Converter.



4. Submission Package
    A. Compensator.v
    B. Quantization.m
    C. Report.pdf