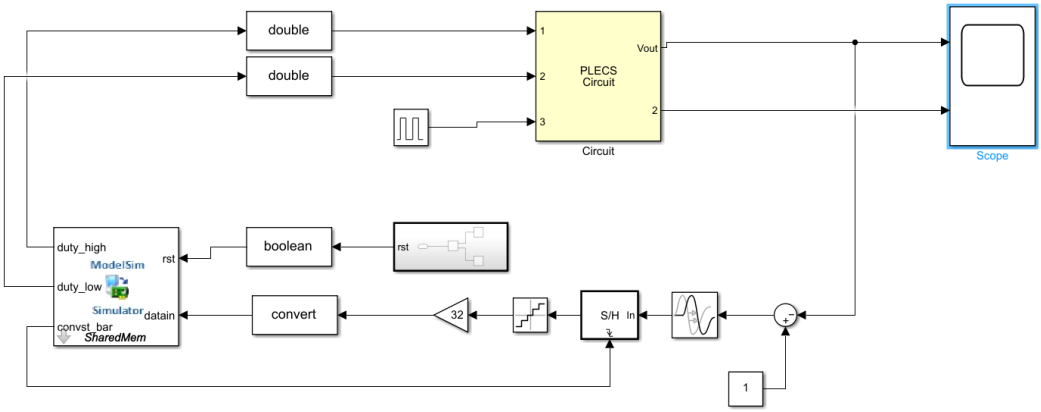
ADC Encoder Report



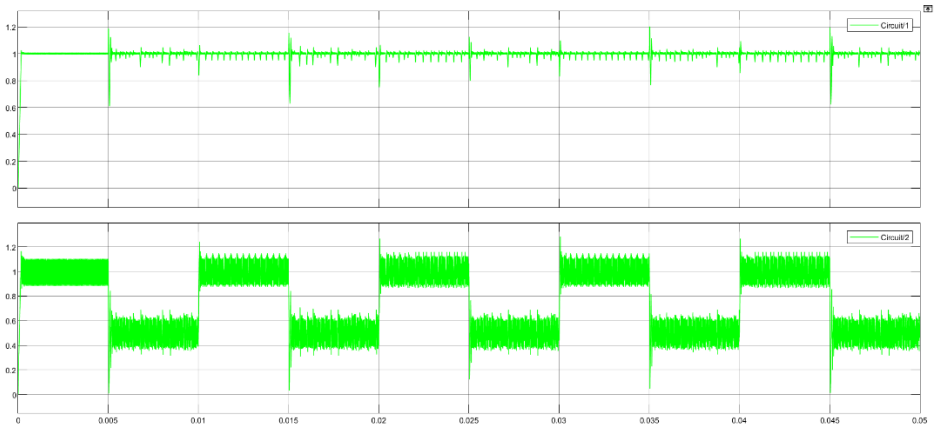
The figure above shows the Simulink wiring diagram of the system implemented. The sample-and-hold block is adjusted to the falling edge. Since the number of bits in the ADC encoder was changed, the gain is set to 32, and the quantizer step size is adjusted to half of the original value (7.825 mV). The rest of the configuration remains consistent with the previous labs, and the wiring is completed with reference to the schematic provided in the handout.

1. ADC Encoder Considerations

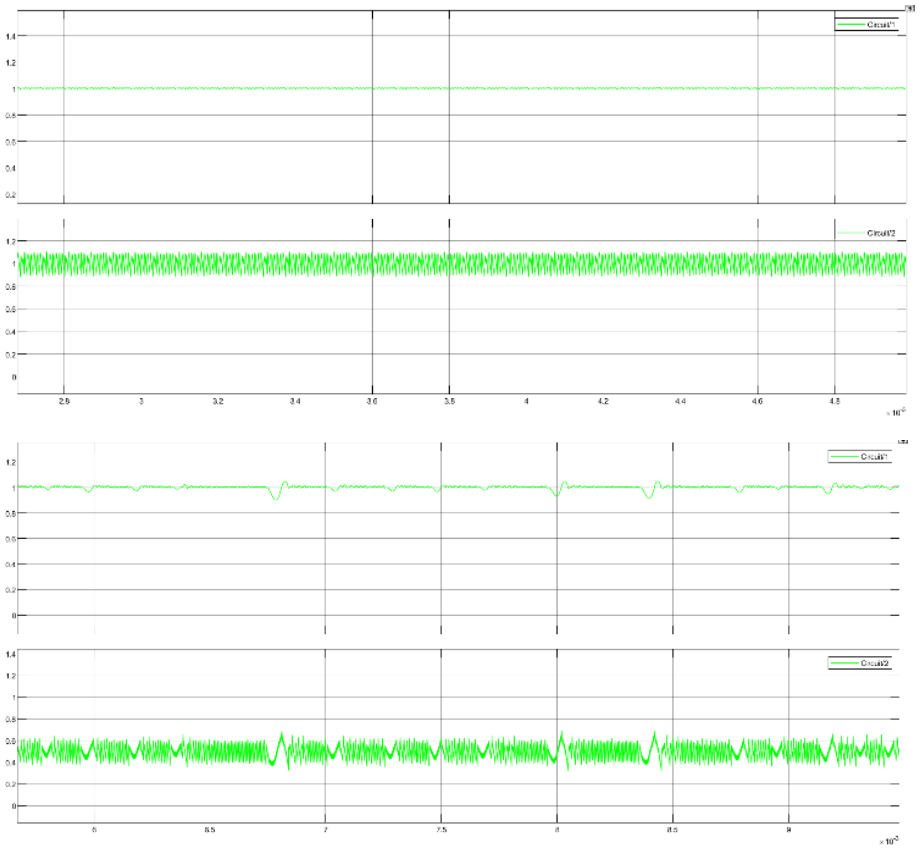
A. Since the ADC is 8 bits and the output voltage vo must remain at 1 V, the proportional calculation is performed as 2 V / 256 bits = 7.8 mV/bit. Thus, 128 bits correspond to 1 V. The ADC encoder conversion range is defined as 114–146, with 130 representing 0.

2. Digital Buck Converter Closed-Loop Simulation

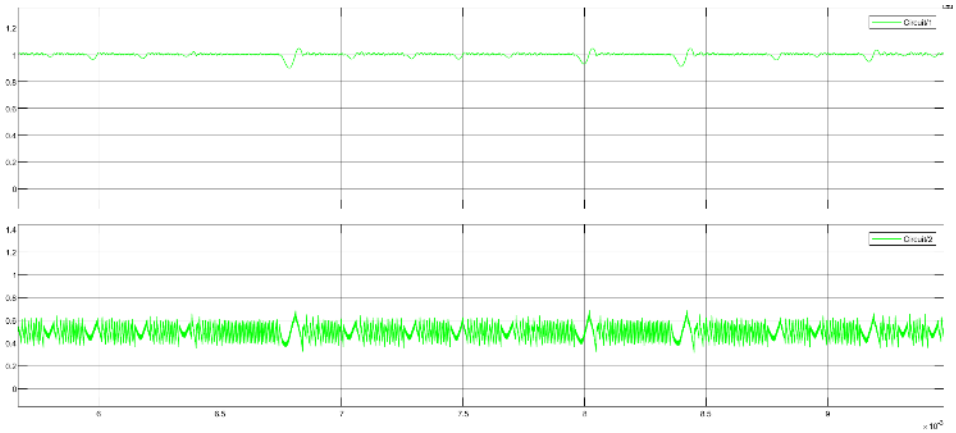
A. Overall Waveforms: The clock time is set to 64 MHz. After calculation and rounding, the clock period is set to 16 ns, and the sample time of all outputs is set to 32 ns. The resulting simulation waveform is shown above.

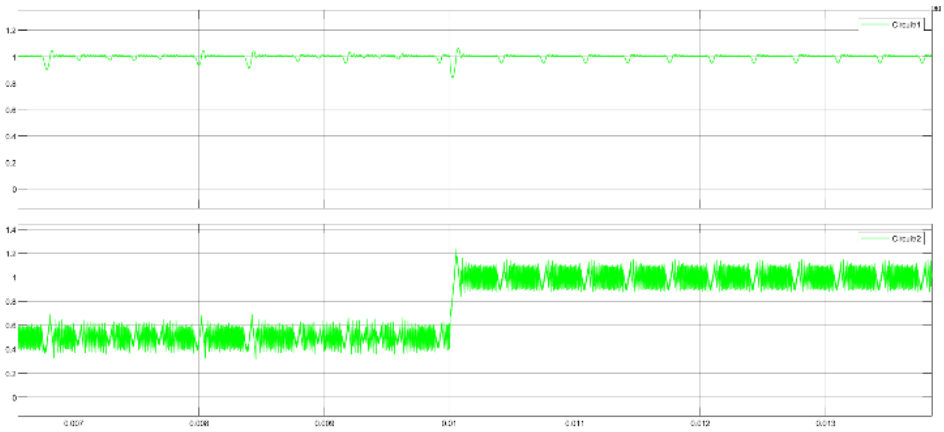


B. Steady-State Behavior: In the steady-state waveform, the voltage oscillates regularly around 1 V and 0.5 V. Although slight irregular oscillations appear under light load, the results still meet the specifications required.



C. Load Transitions: The waveforms above illustrate transitions from heavy load to light load and vice versa. During these transitions, minor oscillations occur, possibly due to an insufficiently small sample time, leading to slight instability. However, extending the load-switching interval shows a trend toward stabilization.





3. Submission Materials

A. top.v

B. clk_divider.v

C. compensator.v

D. deadtime.v

E. dither.v

F. encoder.v