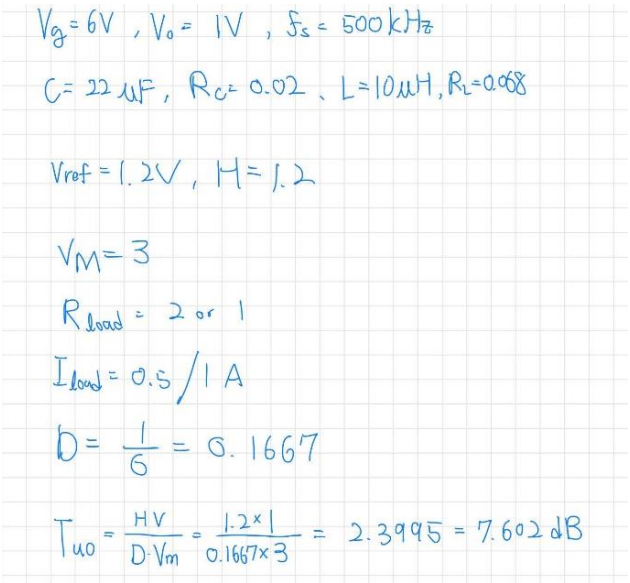
Analog Voltage Mode Buck DC-DC Converter Report

2023/03/16

A. Analog Compensator Design

1. Compensator Obtained by Hand Calculations

i. System Specification

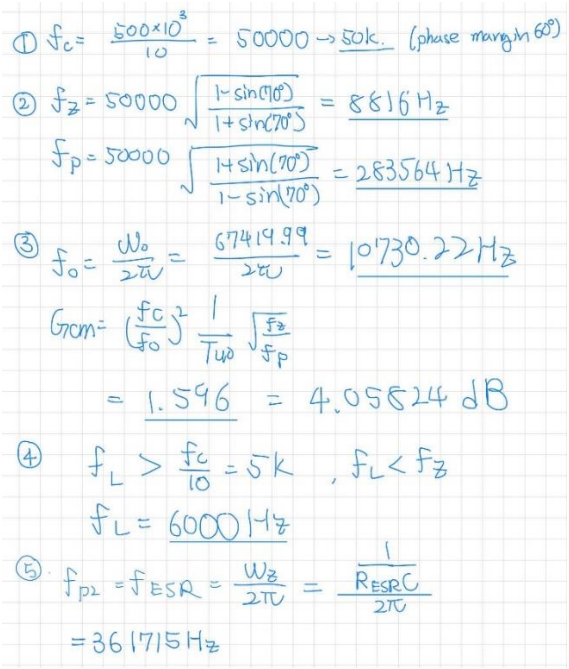


ii. Based on the specifications, we know that Vo=1V and Vref=1.2V; therefore, the sensing gain Hsense is initially set to 1.2.

iii. Since the load current Iload ranges from 0.5 mA to 1 mA, we apply V=IR and first choose Rload to be 1 or 2 (Ω).

iv. Using , we find the duty ratio D=1/6D = 1/6D=1/6.

v. Finally, Tuo is calculated in order to determine Gcm .



vi. According to the formula provided, the crossover frequency fc is set to 0.1 × the switching frequency, i.e., fc = 50kHz (phase margin = 65°).

vii. Substituting the required 65° phase margin into the equations for fz & fp gives the location of one compensator zero and one pole.

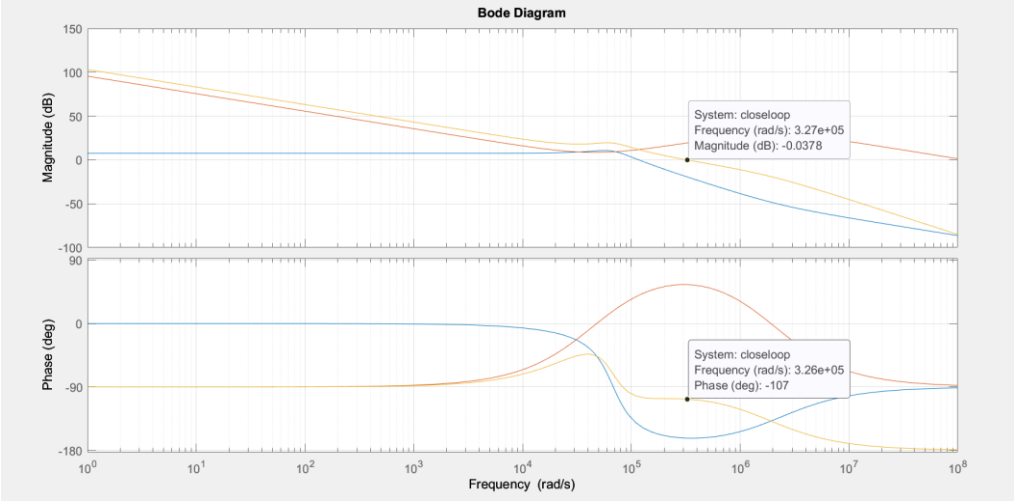
viii. Calculate fo & compensator gain Gcm

ix. Because fc = 50k, the low-frequency pole fL must exceed 5 kHz; it is therefore chosen as 6 kHz.

x. The second pole Fp2 is determined from the selected capacitor value and its parasitic resistance.

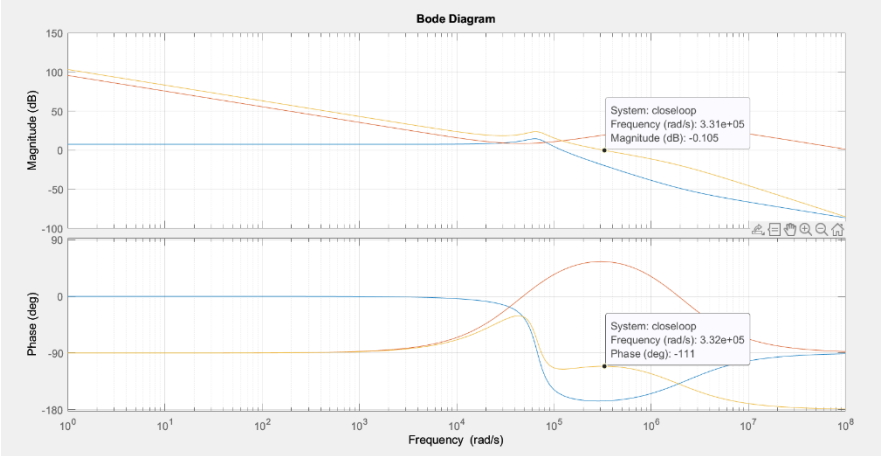
xi. Simulation Results:

a. Rload=1: From the Bode plots we observe fc = 3.27*10^-5 Hz with a phase margin of 63 degree.

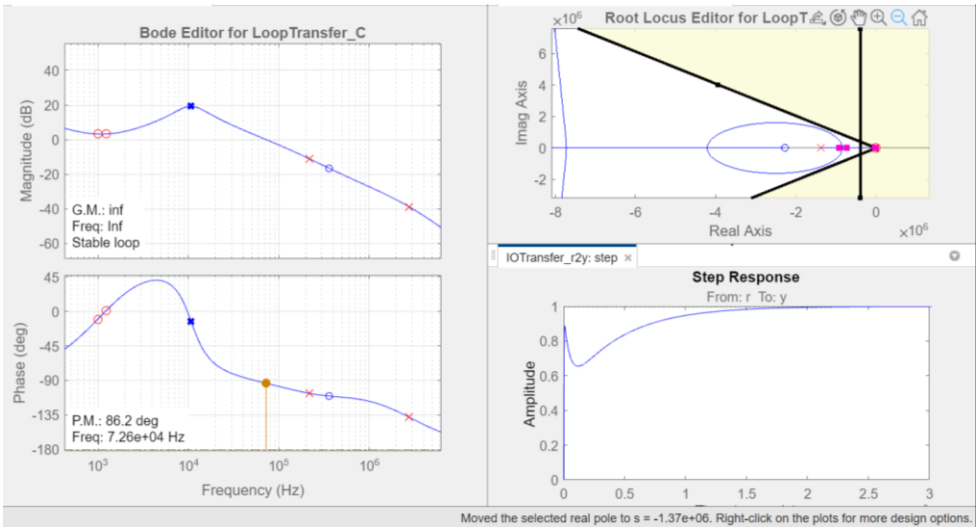


b. Rload=2: From the Bode plots we observe fc = 3.31*10^-5 Hz with a phase margin of 69 degree.

c.



2. Compensator Designed with SISOTOOL



Before launching SISOTOOL, the power stage is defined exactly as in the hand-calculated design. The interactive steps are:

i. Add zeros and poles
   a. Insert the required two zeros and three poles on the Bode plot.
   b. Define the design constraints on the root-locus plot.

ii. Rough placement & gain tuning
   a. Place all zeros and poles in approximate locations.
   b. Use fz1, fz2, fp1 and compensator gain Gm to set the crossover frequency fc initially to about 10^5 Hz.
   c. After the desired phase margin (PM) is reached, return for fine tuning.

iii. Phase-margin adjustment

a. Fine-tune fp1 and fp2 until the target PM is achieved.

iv. Stability & root-locus check

a. Verify overall stability and ensure the root-locus plot stays within the specified bounds.

b. If the locus violates the limits, adjust fp2 primarily.

v. Settling-time control

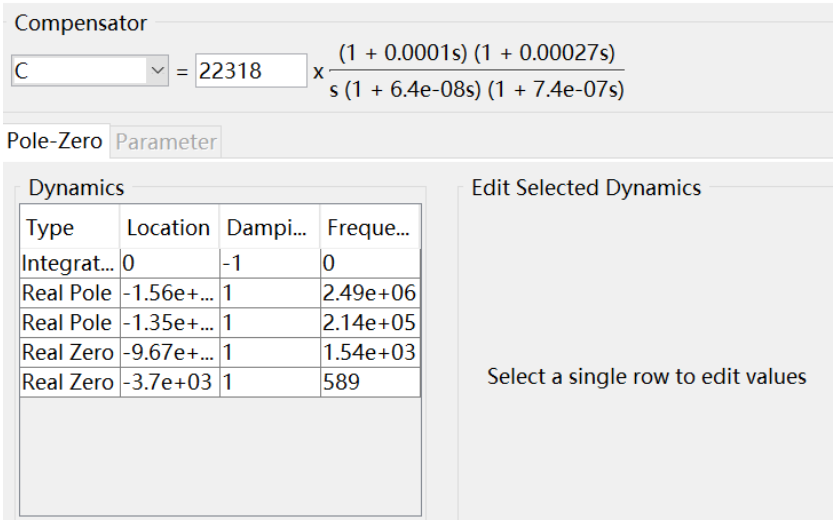
a. Adjust the relative spacing between the two zeros to keep the settling time below 10^-5 s.

vi. Step-response verification

a. Confirm that the simulated step response meets the required settling-time criterion of 1.52 µs.

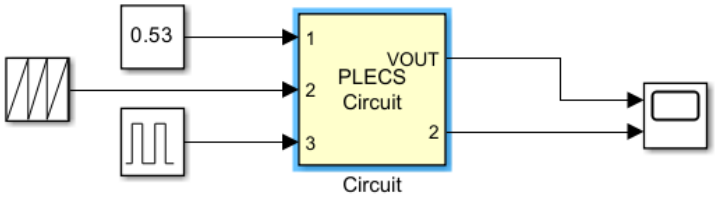
vii. The figure above shows the compensator transfer function obtained with SISOTOOL. The compensator gain is Gcm=22,318. This transfer function will be expanded and used as the compensator block in the subsequent Simulink model.

a.



B. Buck Converter – Open-Loop Simulation (Power stage + PWM only)

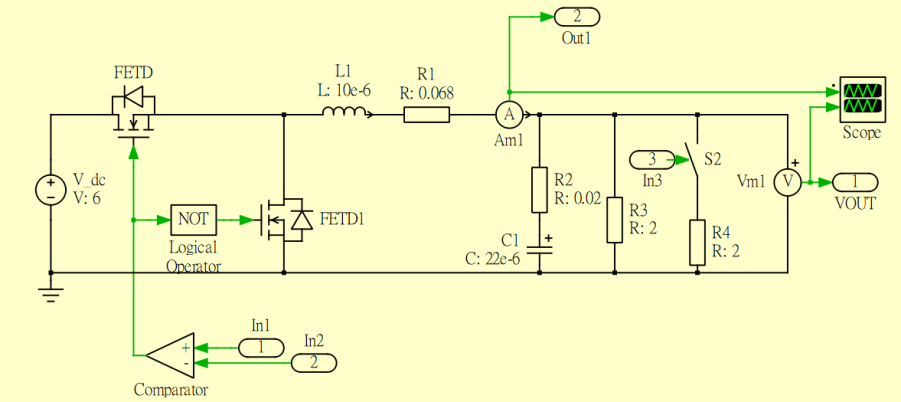
1. MATLAB/Simulink setup (Vg=6 V, Io=500 mAI and 1)



2. The schematic above shows the external circuit used for the open-loop

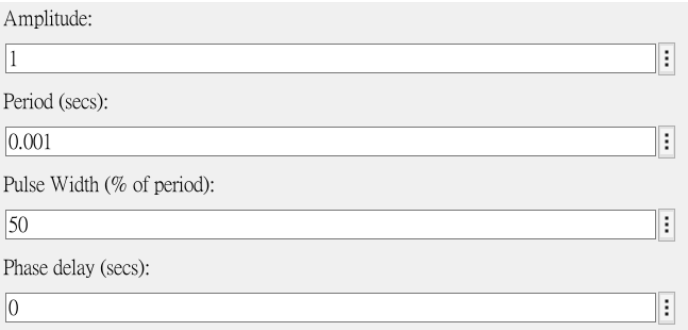
simulation:

3. Comparator reference: A constant 0.53 V is applied to the minus input of the comparator.
4. PWM carrier: A saw-tooth waveform is fed to the plus input and compared with the reference to generate the switch-drive PWM signal.
5. Load-step control: A third input, an impulse signal, forces the transition between the two load currents (500 mA → 1 A).
6. Waveform monitoring: The output voltage *V*out and the switch-node (second output) are routed to a Scope block for realtime observation.



7. The circuit is built to the specifications. For the load-current transition, two 2 Ω resistors are connected in parallel. By toggling the IN3 switch, the effective RloadR switches between 2 Ω and 1 Ω, thereby changing Iout between 500 mA and 1 A.

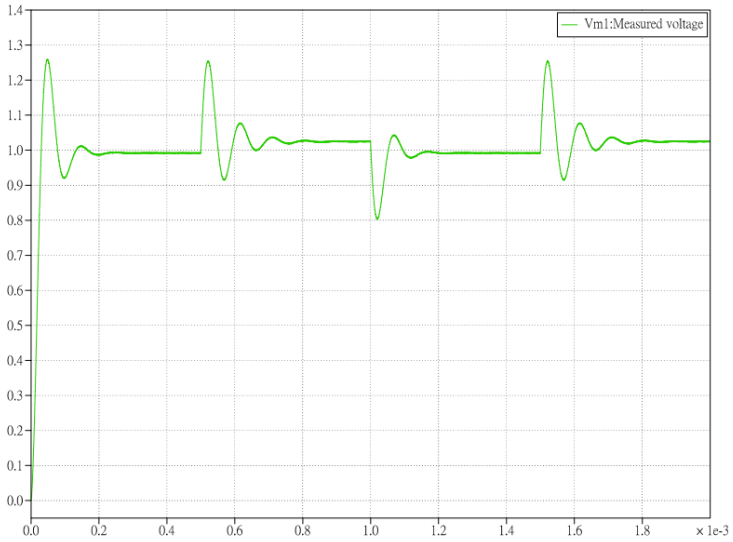
8. The saw-tooth carrier is set to a period of 2×10^−6 s (i.e., 2 µs, corresponding to 500 kHz) with an amplitude of 3 V.



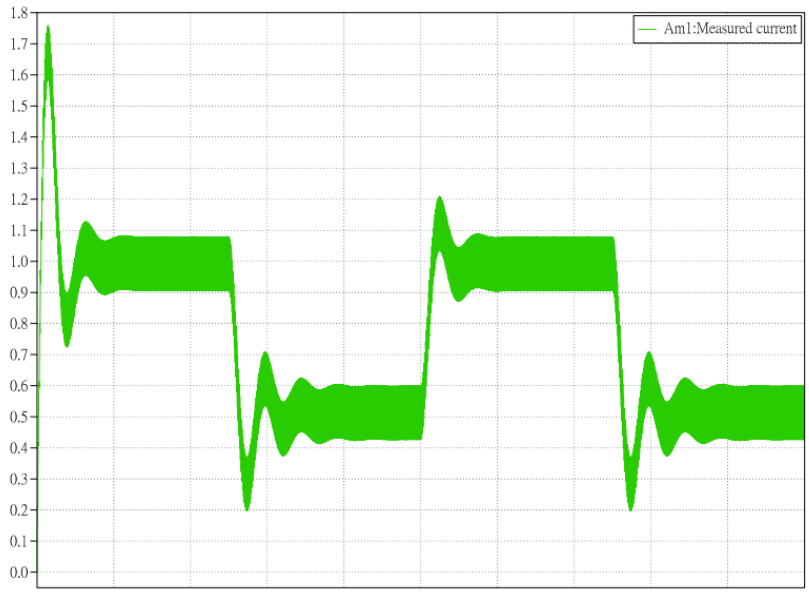
9. The square-wave source is configured with a period of 0.001 s and a 50 % duty cycle. Within the 0.002 s observation window, this setup injects (or removes) the load three times.

10. The scope display for the open-loop steady-state simulation shows that:

i. Output voltage VoutV: Thanks to the capacitor's discharge behavior, VoutV stays roughly constant at ≈ 1 V.

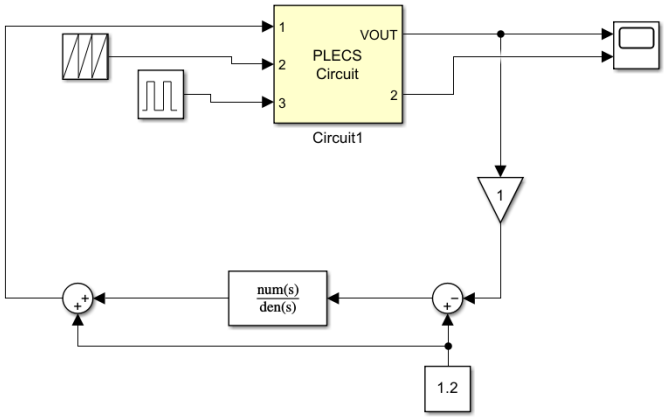


ii. Output current Iout: As the load toggles, Iout alternates between 1 A and 0.5 A.



C. Buck-Converter Closed-Loop Simulation (Power stage + PWM + analog compensator)

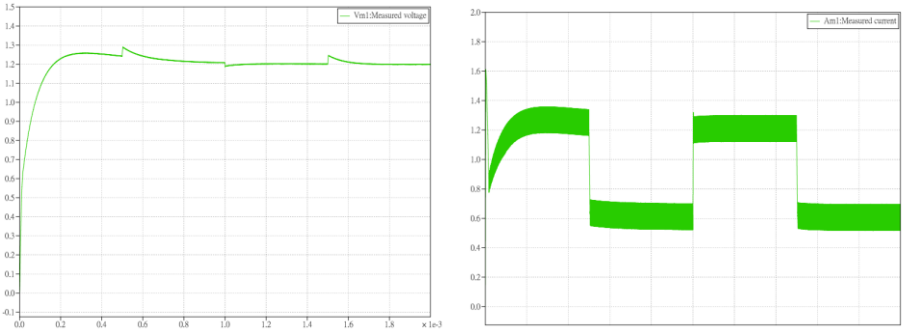
1. MATLAB/Simulink setup (Vg=6, Io=500mA,1A)



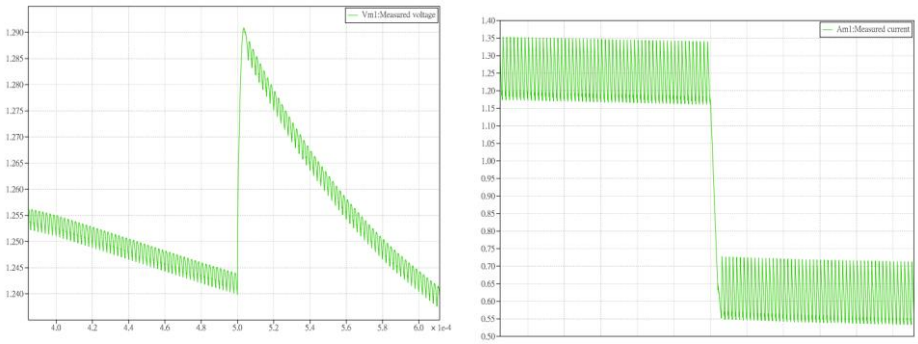
2. The external circuit for the closed-loop simulation uses the same saw-tooth carrier and impulse signal as in the open-loop model. The sensing gain Hsense is set to 1, the reference voltage Vref to 1.2 V, and the compensator employs the transfer function obtained from SISOTOOL:

$$C = \frac{0.000602586S^2 + 8.25766S + 22318}{4.736\times10^{-14}S^3 + 8.04\times10^{-7}S^2 + S + 0}$$

3. In the closed-loop simulation, the output voltage stays at approximately 1.2 V, while the output current stabilizes at around 1.2 A and 0.6 A during the load transitions.



4. When the load increases, the response times of the output voltage and current are displayed; the left and right plots use the same time scale.



5. When the load decreases, the response times of both the output voltage and current are shown; the two graphs use the same time scale.