FPGA Verification Report

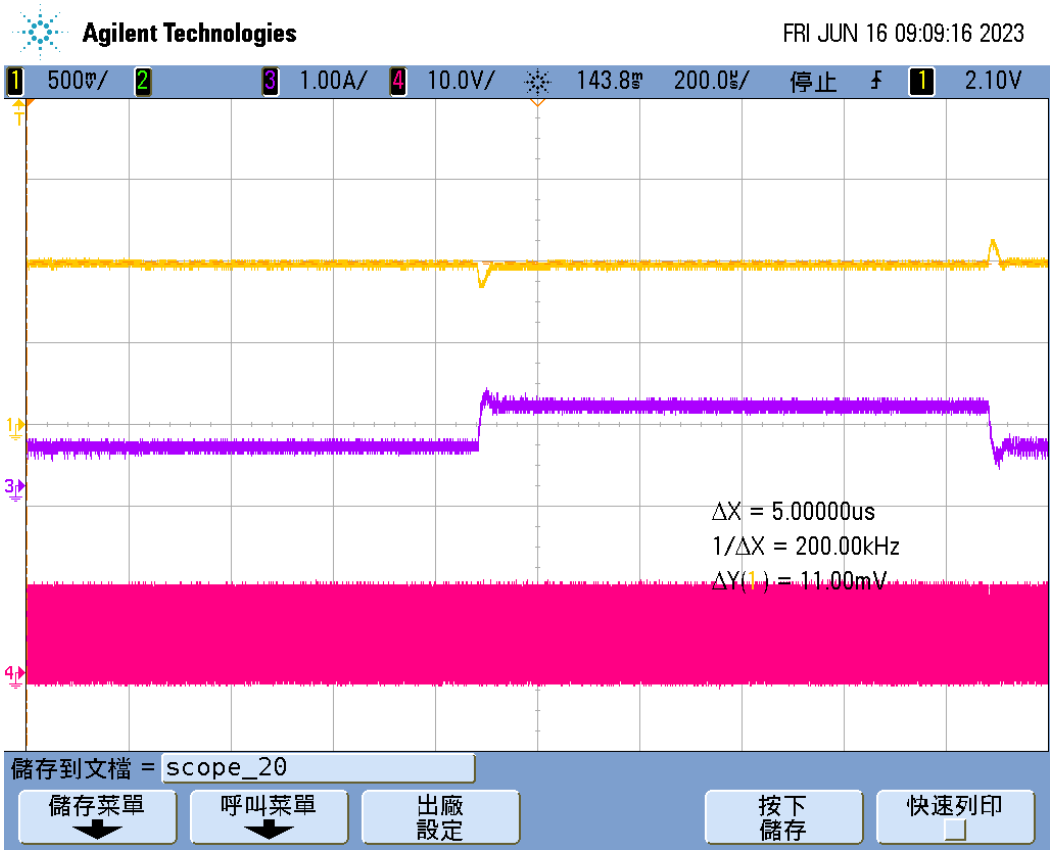
The compensator designed in\ADC exhibited issues with **Limit Cycle Oscillations (LCO)**. Therefore, a new compensator was designed, and the crossover frequency was controlled around 50 kHz, resulting in more desirable performance.

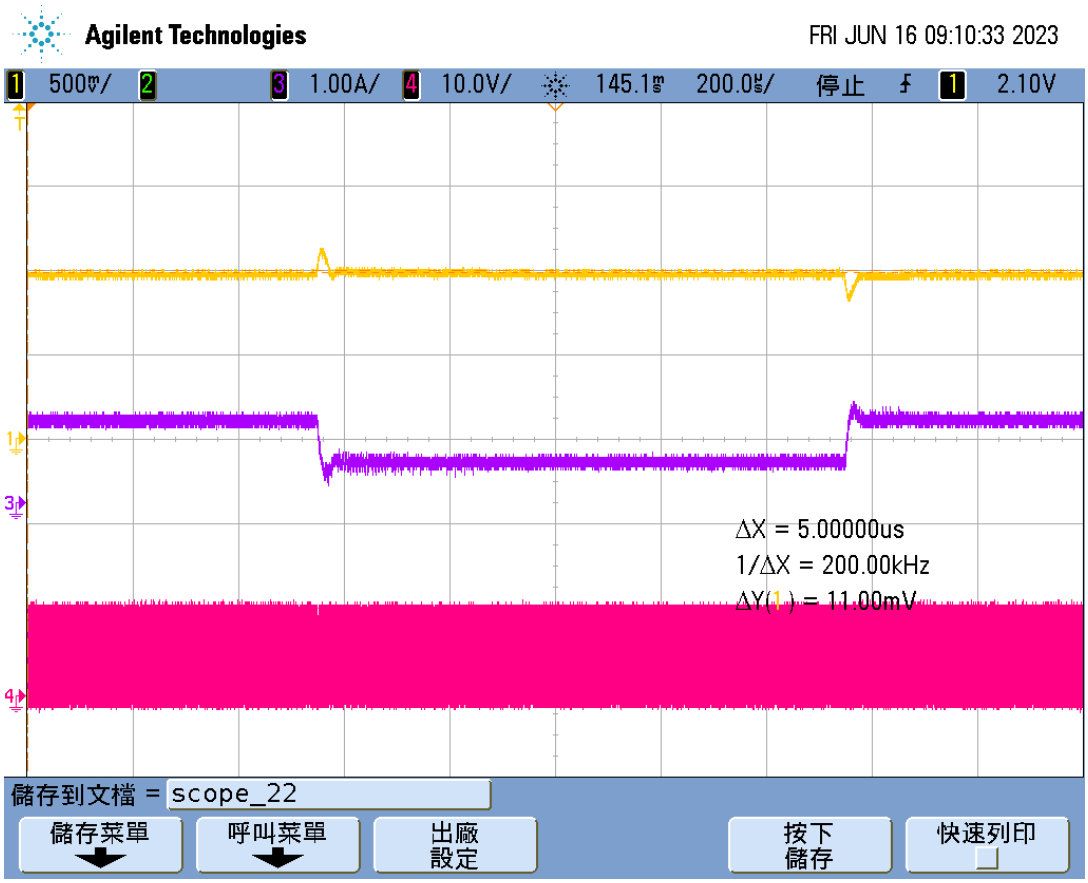
Most of the critical warnings were resolved, with only timing simulation remaining. After assigning the pins according to the specification, the SOF file was generated and programmed into the FPGA board. The digital compensator was simulated and integrated with the analog power circuit on the board. Finally, the experimental results were verified using an oscilloscope.

Notes:

The power-up sequence must be strictly followed during actual operation.

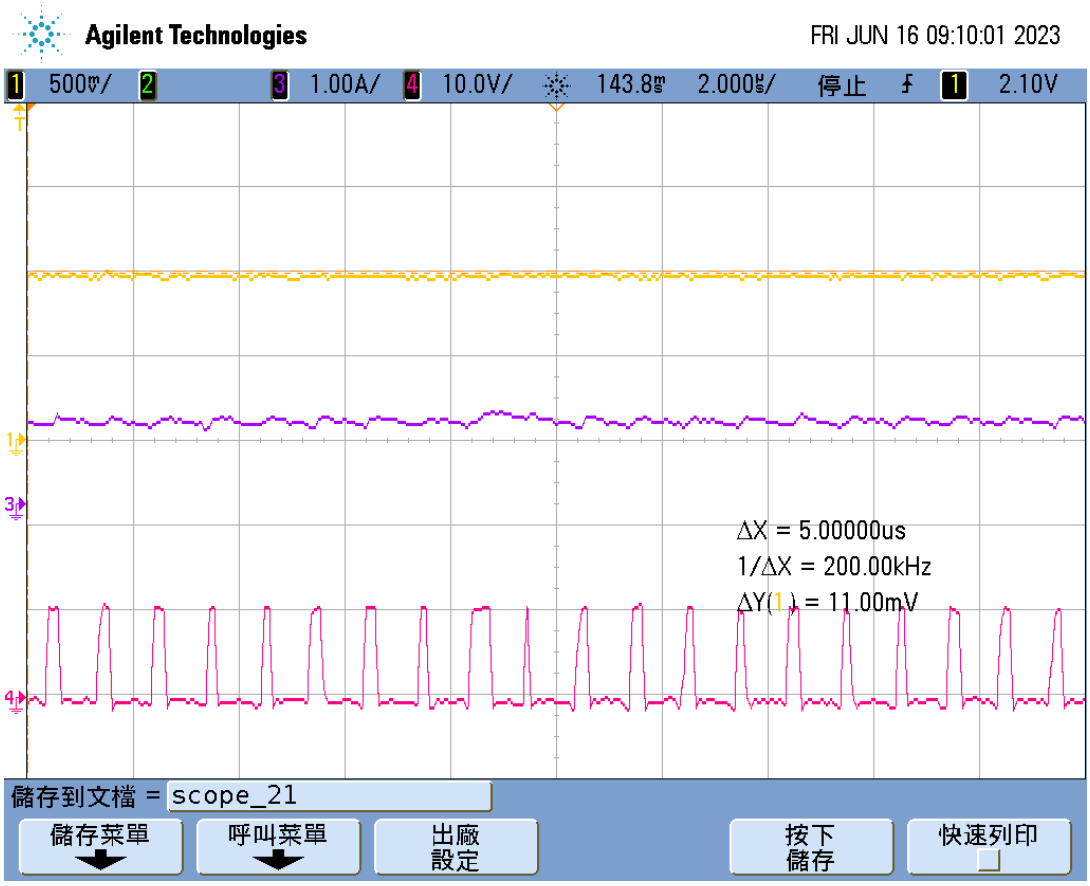
1. Load Transient Waveform





From the figure above, it can be observed that during load switching, the output voltage and current oscillations meet the required specifications. Furthermore, after the load transition, the system continues to provide stable output under both light and heavy load conditions.

2. Steady-State Waveform



The steady-state waveform also meets the specifications defined for this project, with all oscillations remaining within controllable limits.