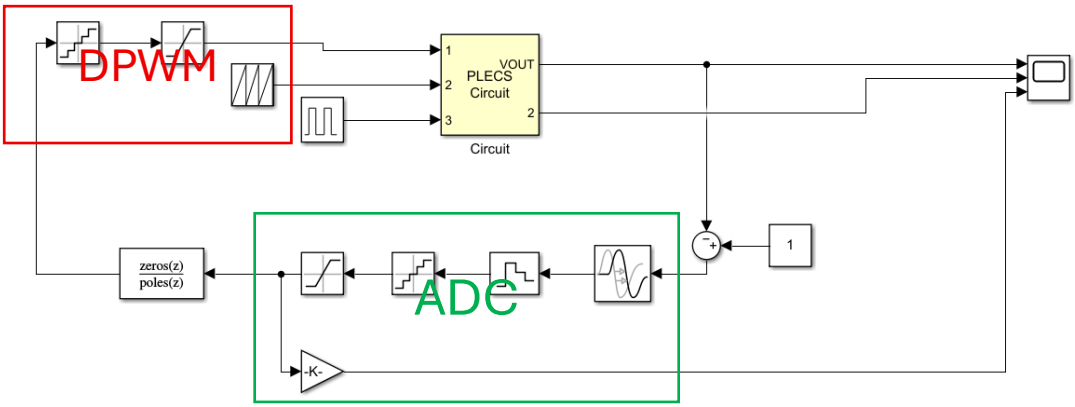
Digitally Controlled Voltage Mode Buck Converter

Report

A. Functional Blocks and Key Design Considerations



i. Analog-to-Digital Converter (ADC)

a. **Pipeline latency**: total delay t = t_{conv} + t_{cal} + t_g. With t_{conv} =420 ns, t_{cal}=65 , t_g=10 ns ⇒ **loop delay ≈ 495 ns**.

b. **Sample-and-hold (ZOH)**: sampling period $T_s=1/f_{sw}$=2µs

c. **Resolution**: 7-bit ⇒ LSB $\Delta V_q=V_{FS}/2^7$=15.625 mV

d. **Saturation**: output clamped to ±4 LSB, i.e. –62.5 mV … +62.5 mV.

e. Designed for 1 MHz switching.

ii. Digital PWM (DPWM)

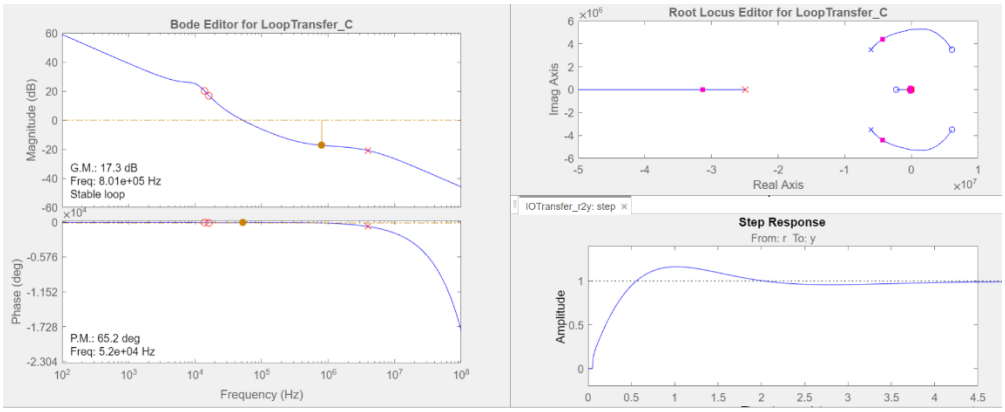
a. Resolution: **9 bits**.

b. Duty-cycle quantization step derived accordingly.

c. Higher resolution chosen to minimize limit-cycle oscillation (LCO).

B. Digital Compensator Design

i. Place desired poles/zeros in the plant transfer function while accounting for the 495 ns loop delay to meet bandwidth and stability specs.

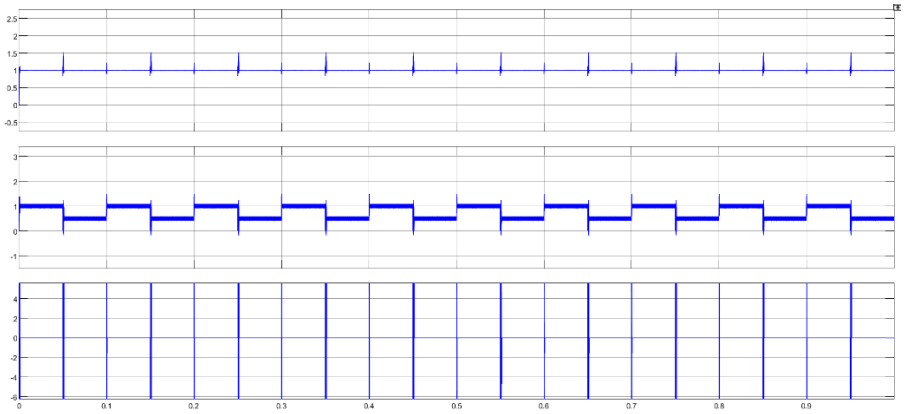


ii. Export analogue compensator into MATLAB, perform s-to-z transformation with prewarp to obtain the discrete transfer function in the form required by the digital controller.

C. Closed-Loop Simulation (Power Stage + ADC + DPWM + Compensator)

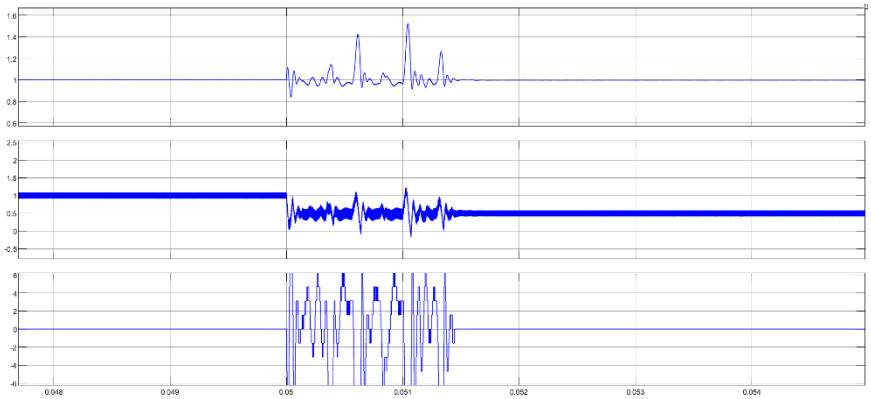
i. Time-Domain Results:

a. Overall waveform shows inductor current varying smoothly between 0.5 A and 1 A.

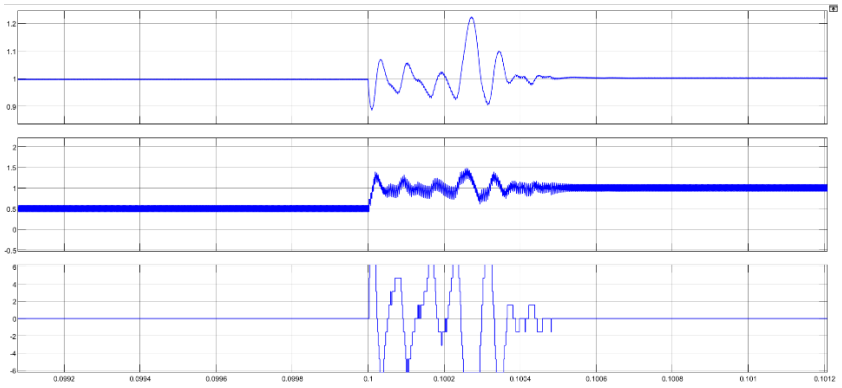


b. Transient response: Light-to-heavy load step and heavy-to-light step behave as predicted.

1. Transfer from Light load to heavy load

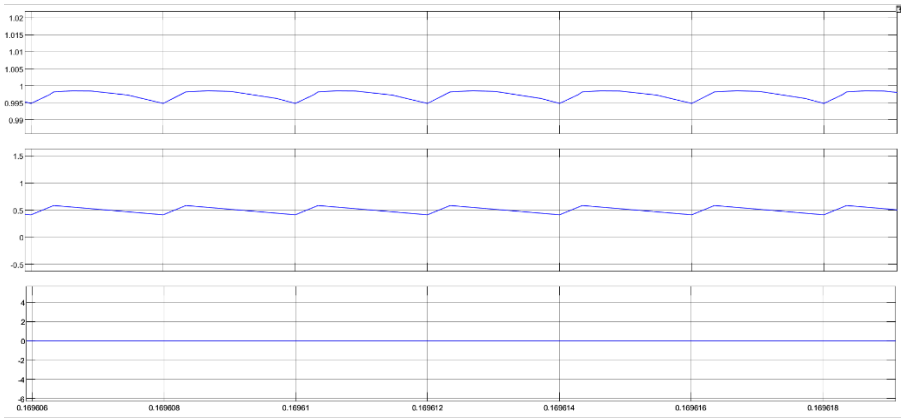


2. Transfer from heavy load to Light load



ii. Steady state:

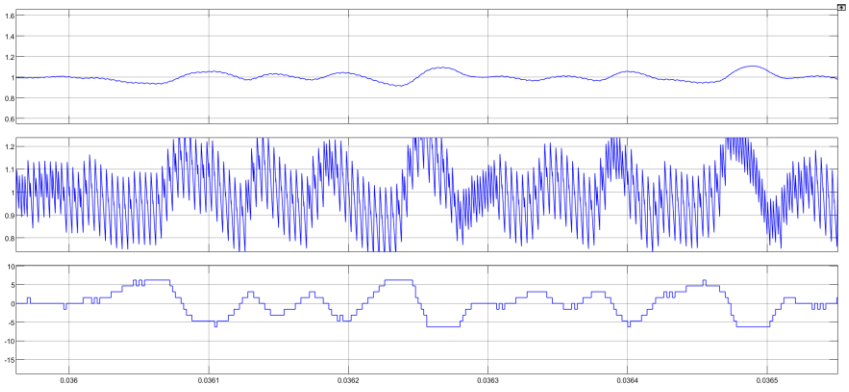
a. Verified at 1 A and 0.5 A; voltage and current ripple within spec.



D. Limit-Cycle Oscillation (LCO) Simulation

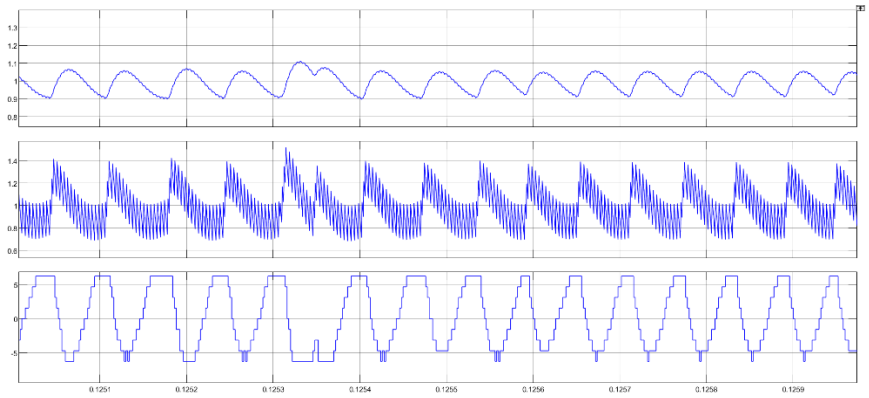
i. A1: Reduce DPWM resolution from 9 bits to **5 bits** → quantisation too coarse.

a. Waveform: Pronounced LCO appears.



ii. A2: Double compensator gain so output is no longer properly limited.

a. Waveform: Control loop becomes unstable, exhibiting oscillatory behavior.



E. Submission Package

i. Report.pdf

ii. DBE.m

iii. Model.mdl