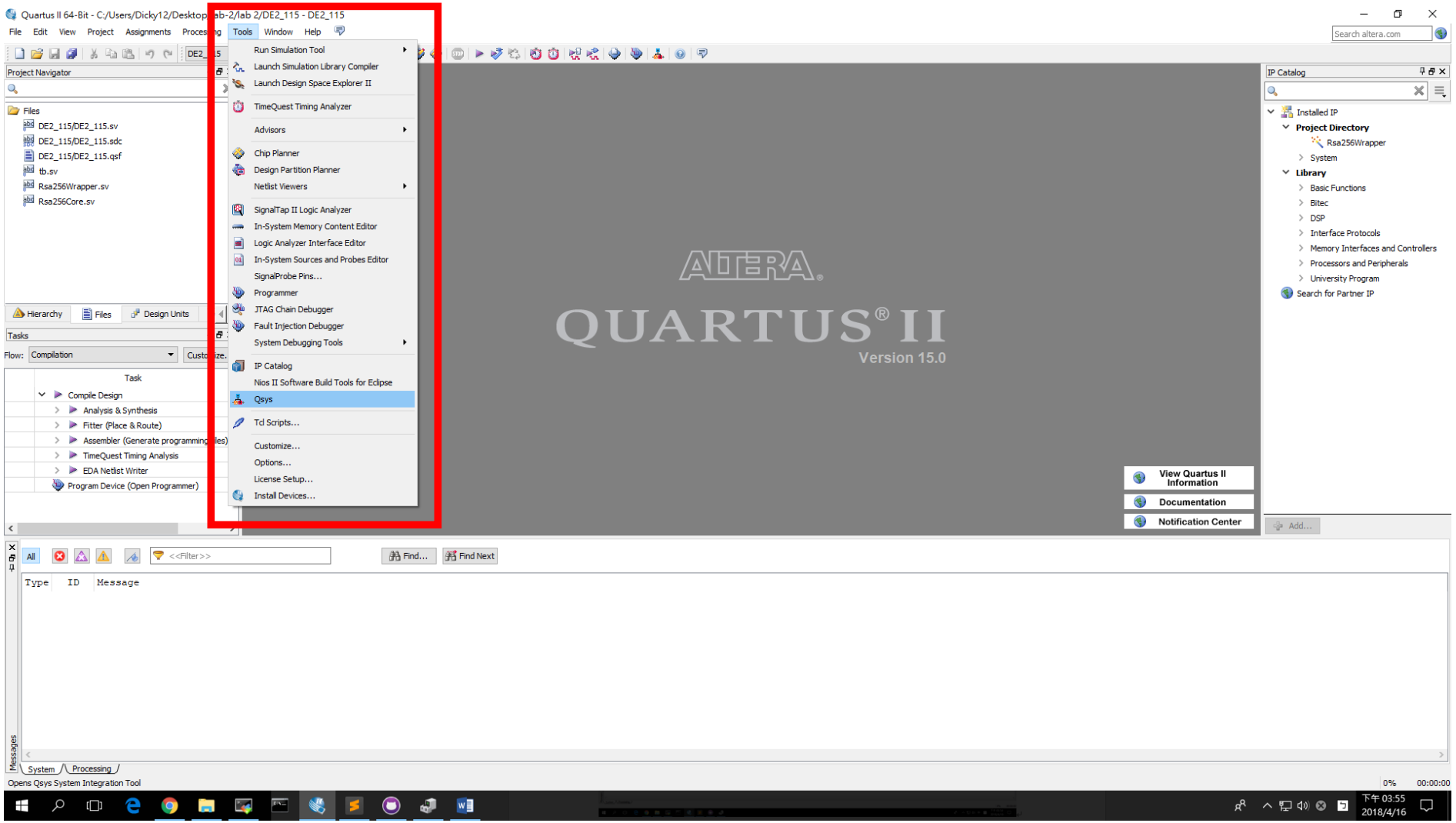
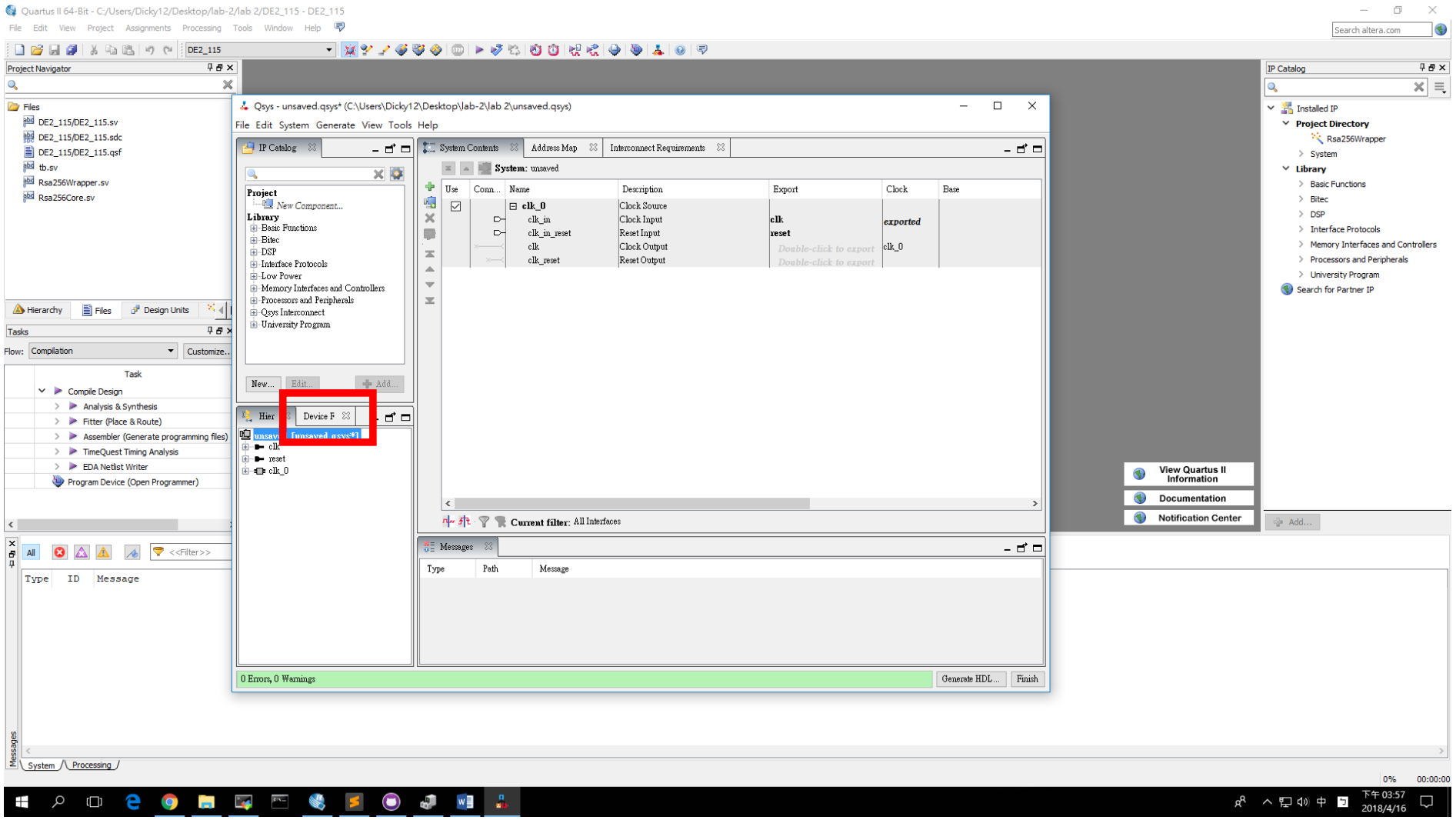
Qsys on Quartus 15.0 Tutorial

提供：董子維、楊其昇
整理：鍾杰

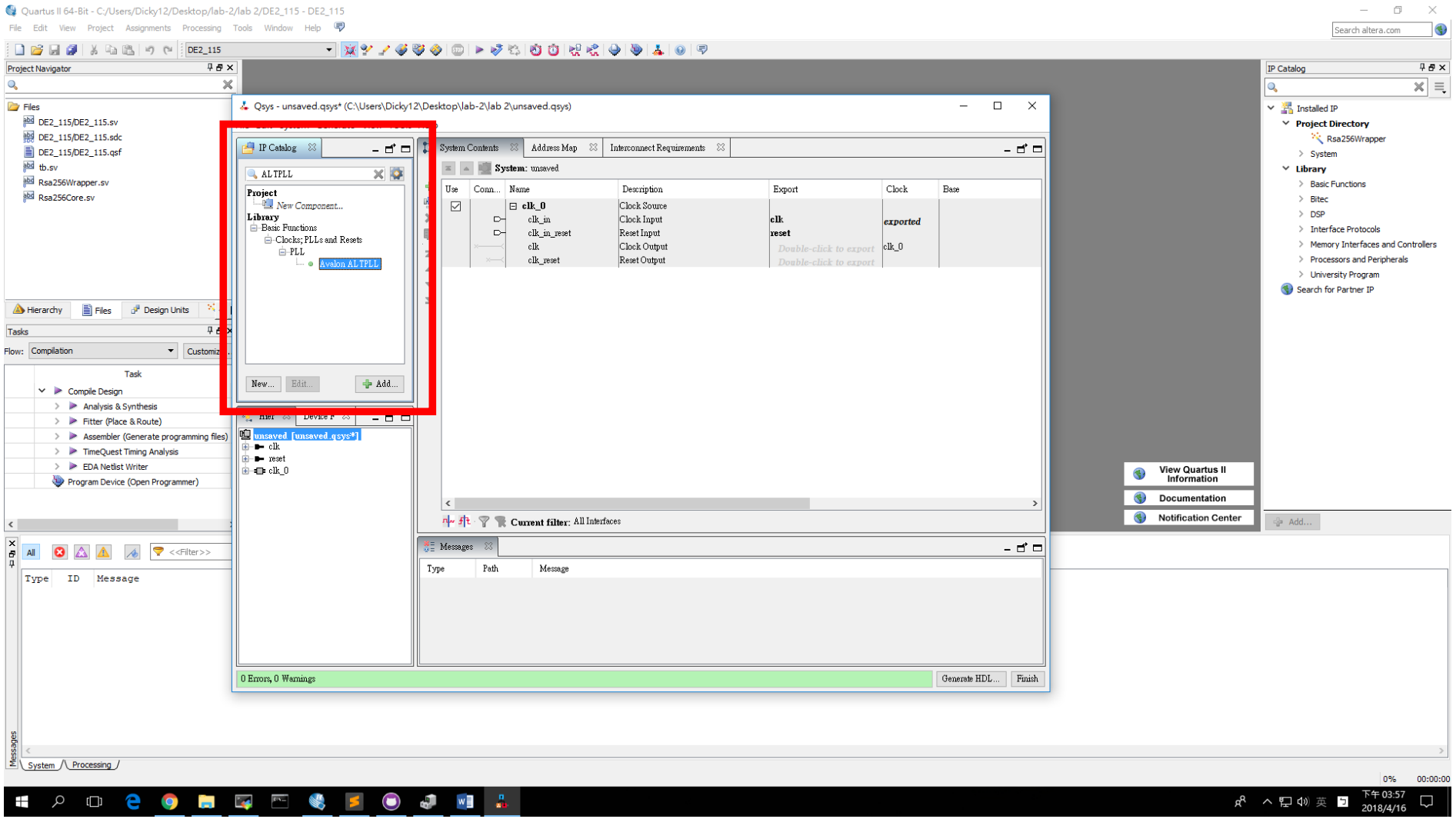
打開Qsys (Tool → Qsys)



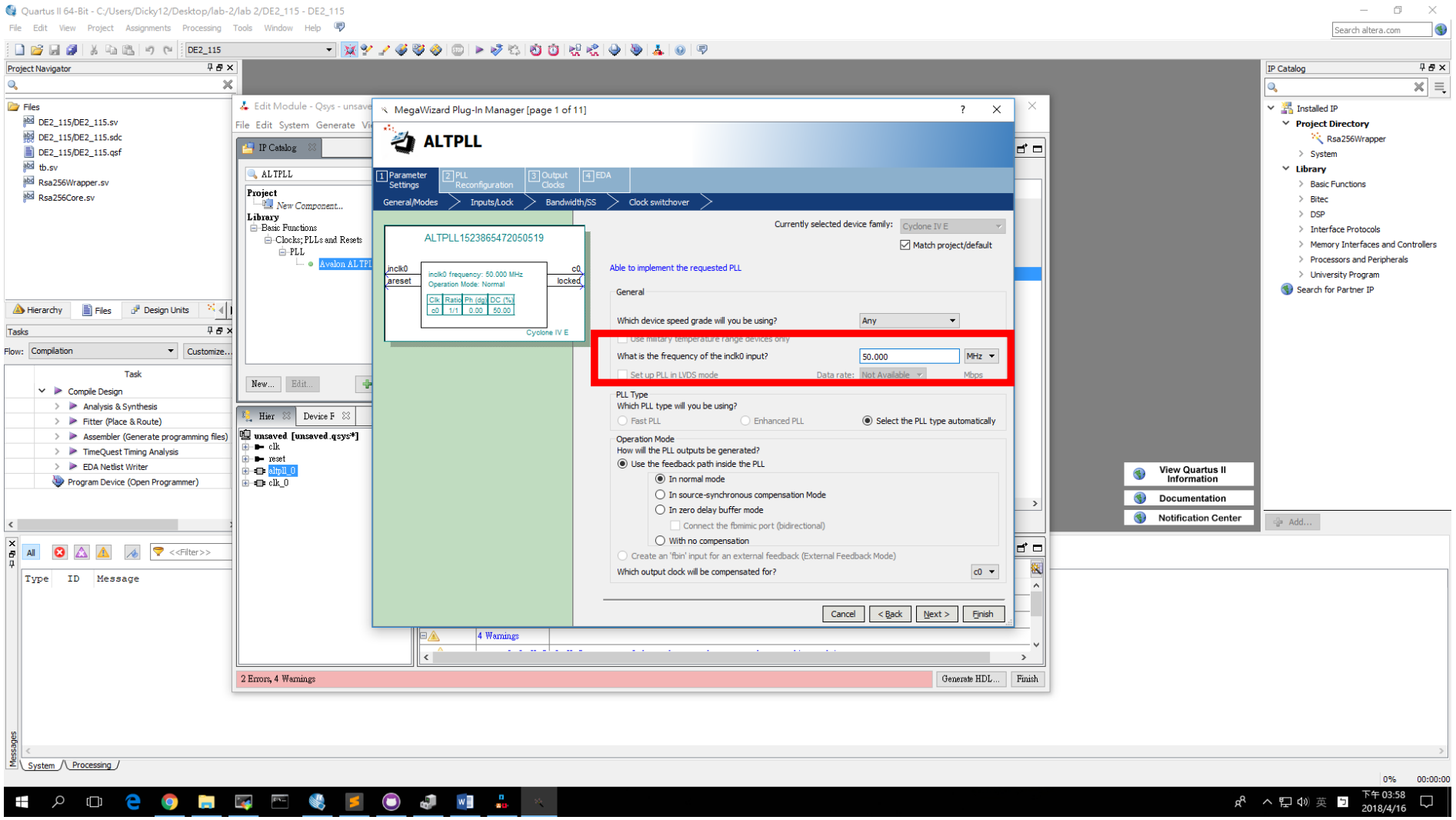
到Device Family選擇Cyclone IV E



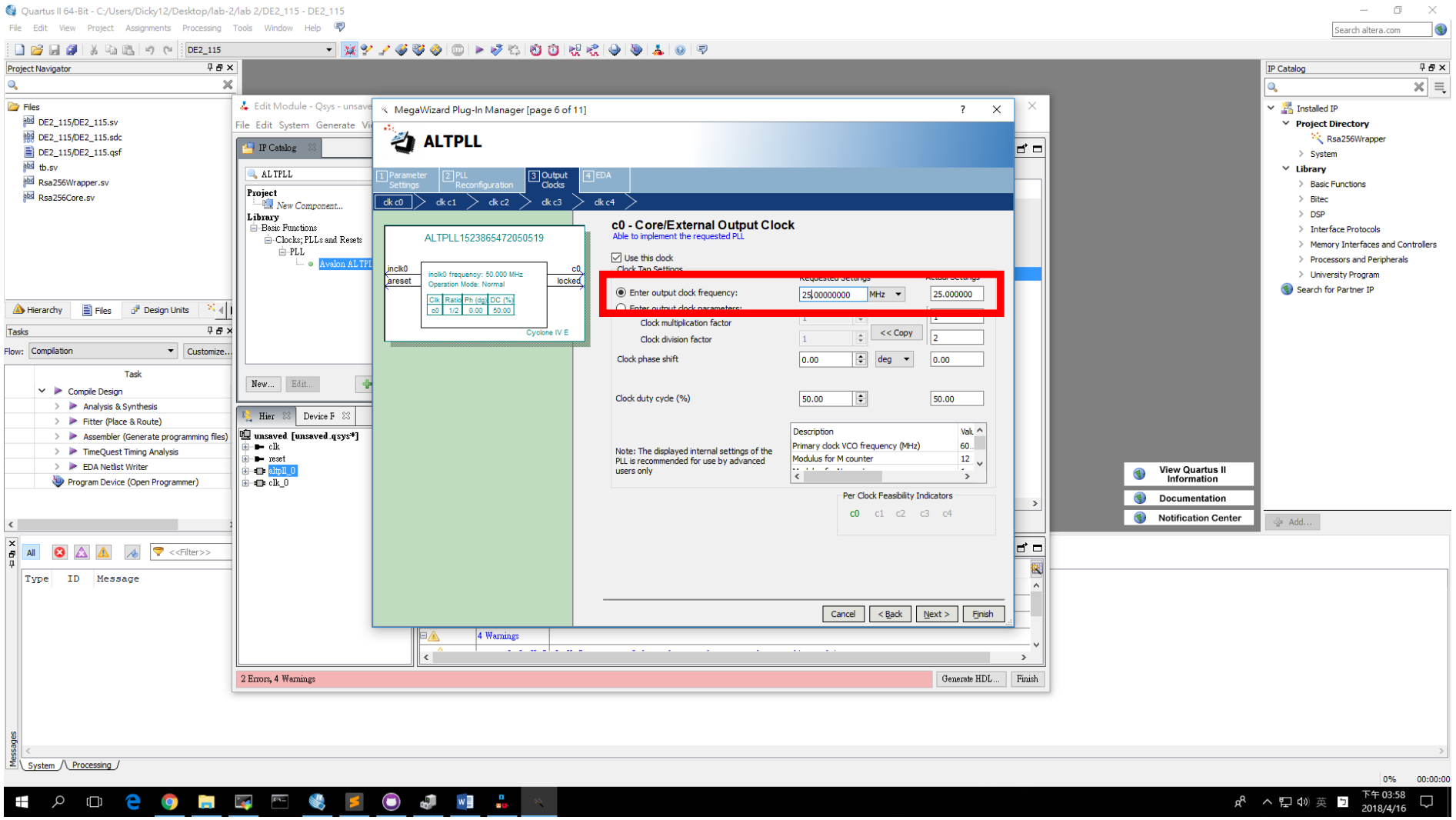
搜尋Avalon ALTPLL，雙擊新增



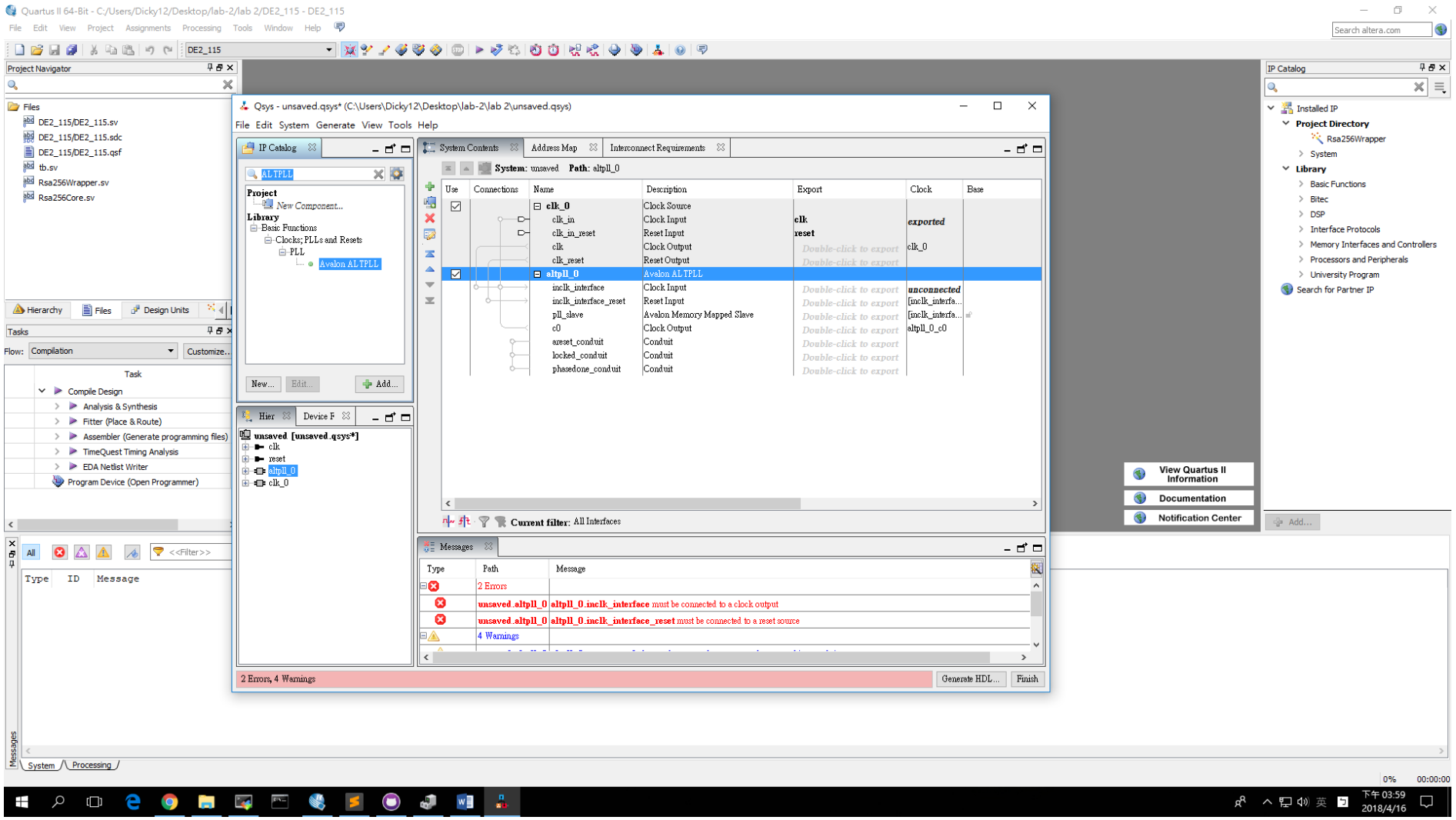
Frequency of inclk0 input = 50MHz



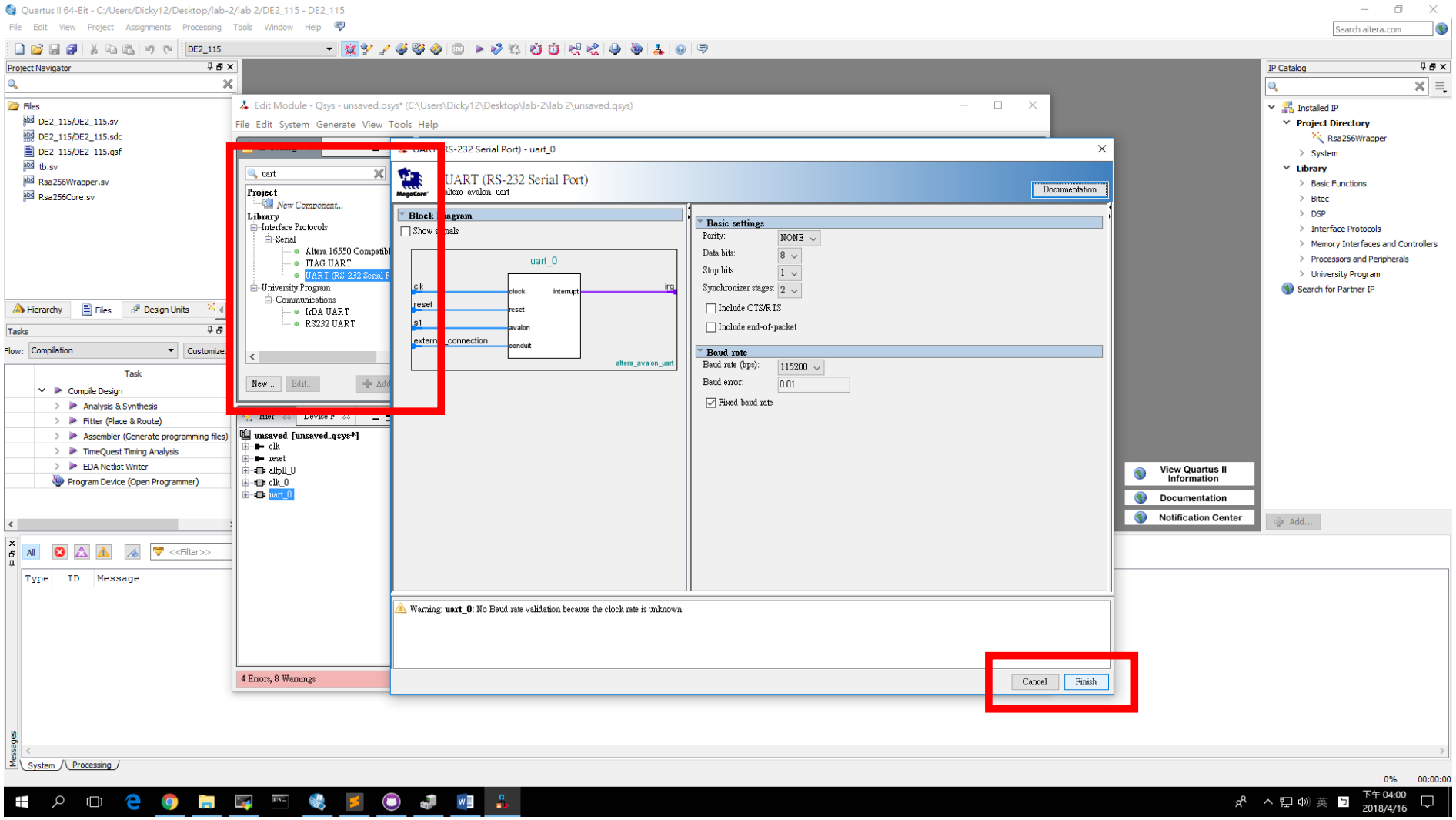
Output clock frequency = 25MHz



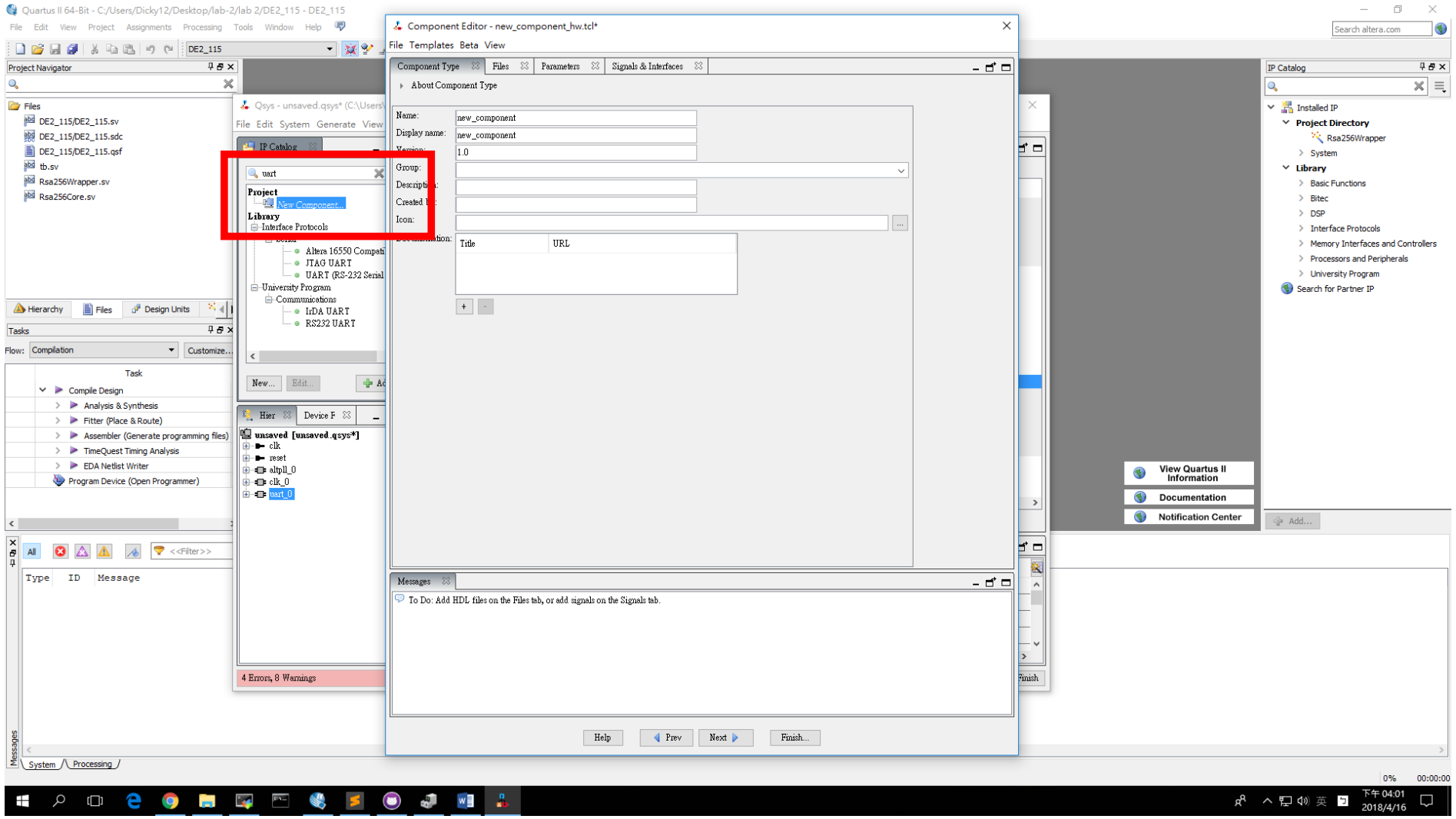
按Finish可在右側看到新增的ALTPLL



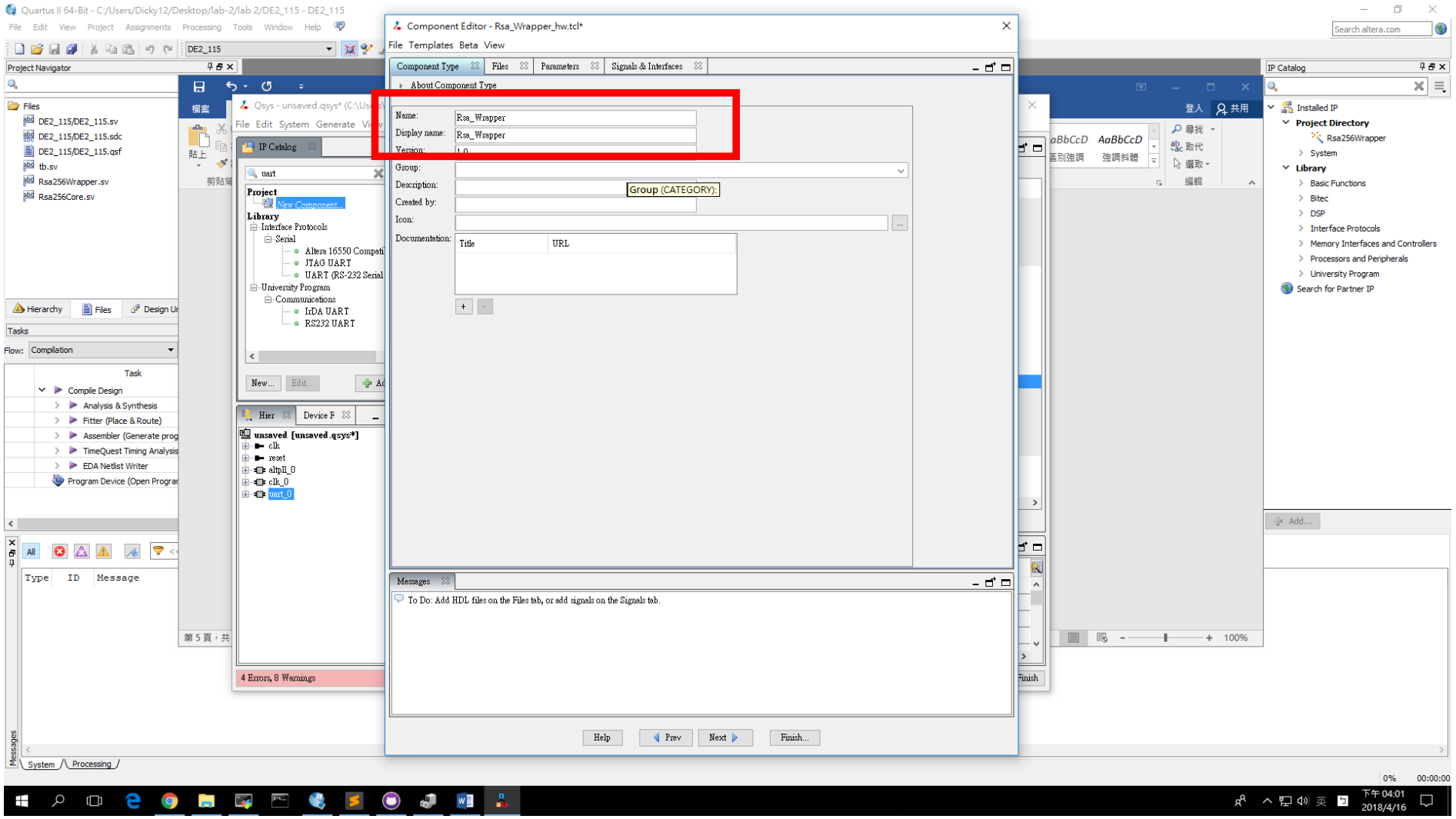
搜尋UART → UART (RS-232 Serial Port) → Finish



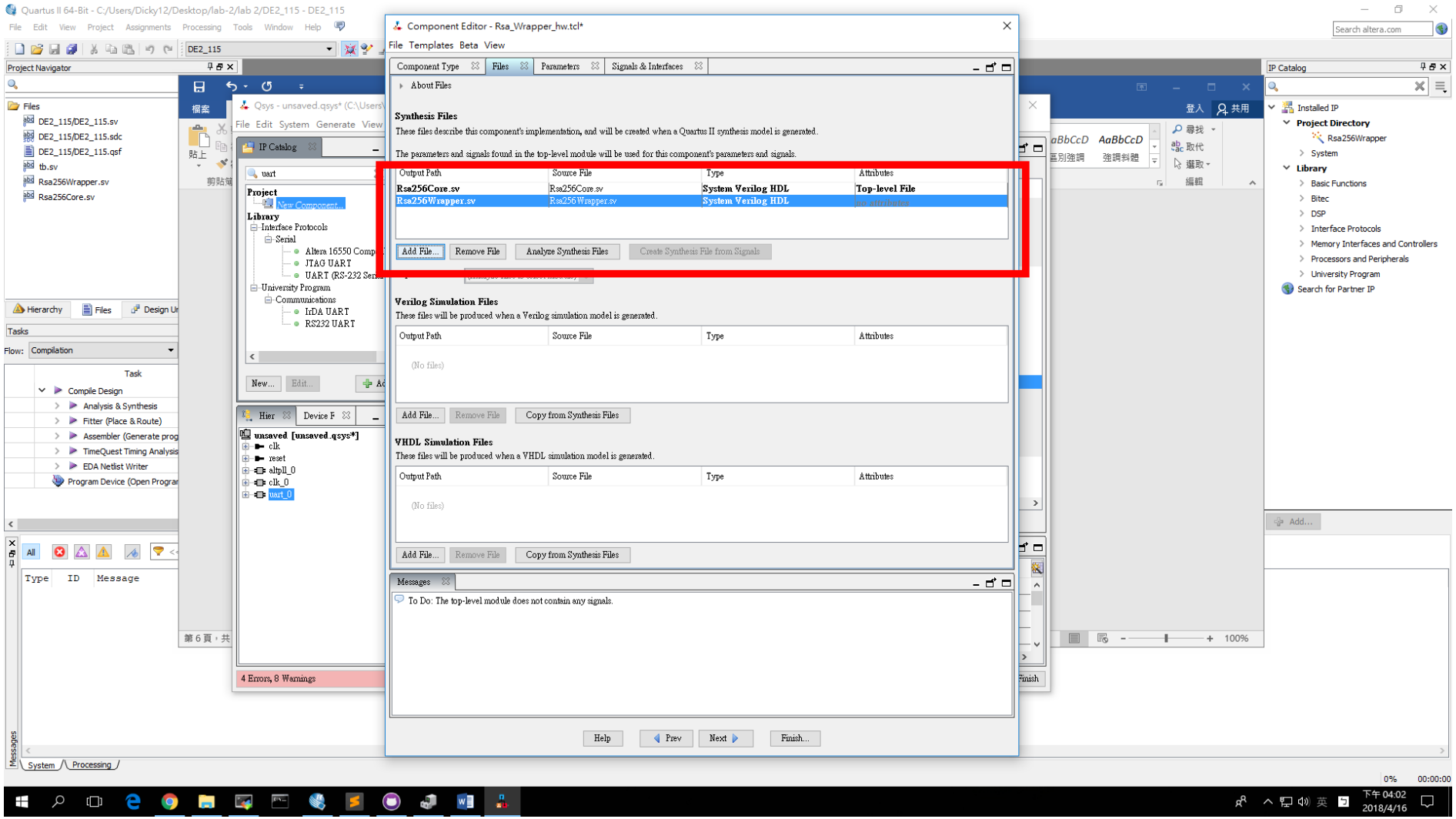
雙擊New Component



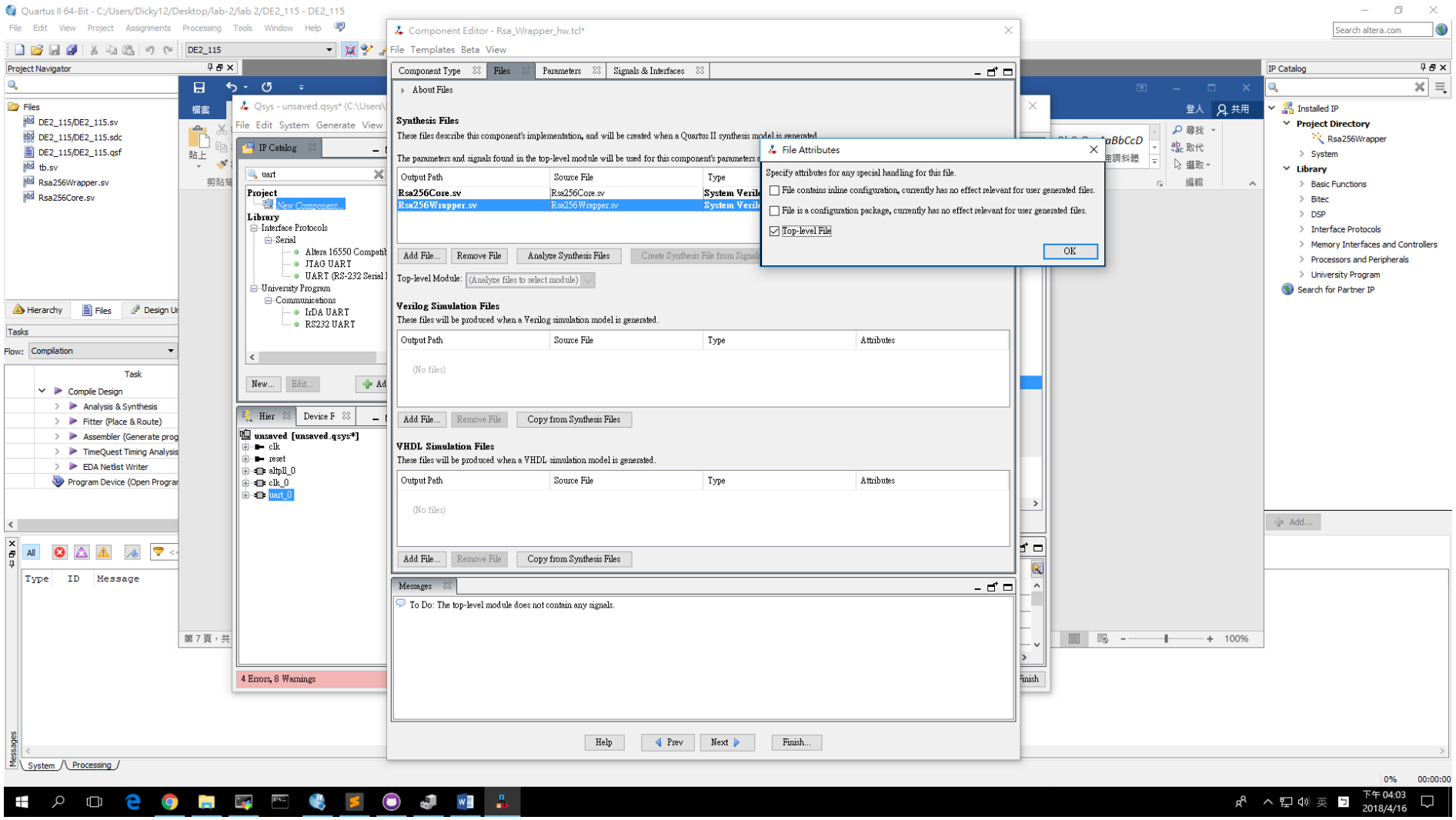
Name = Rsa_Wrapper
Display Name = Rsa_Wrapper



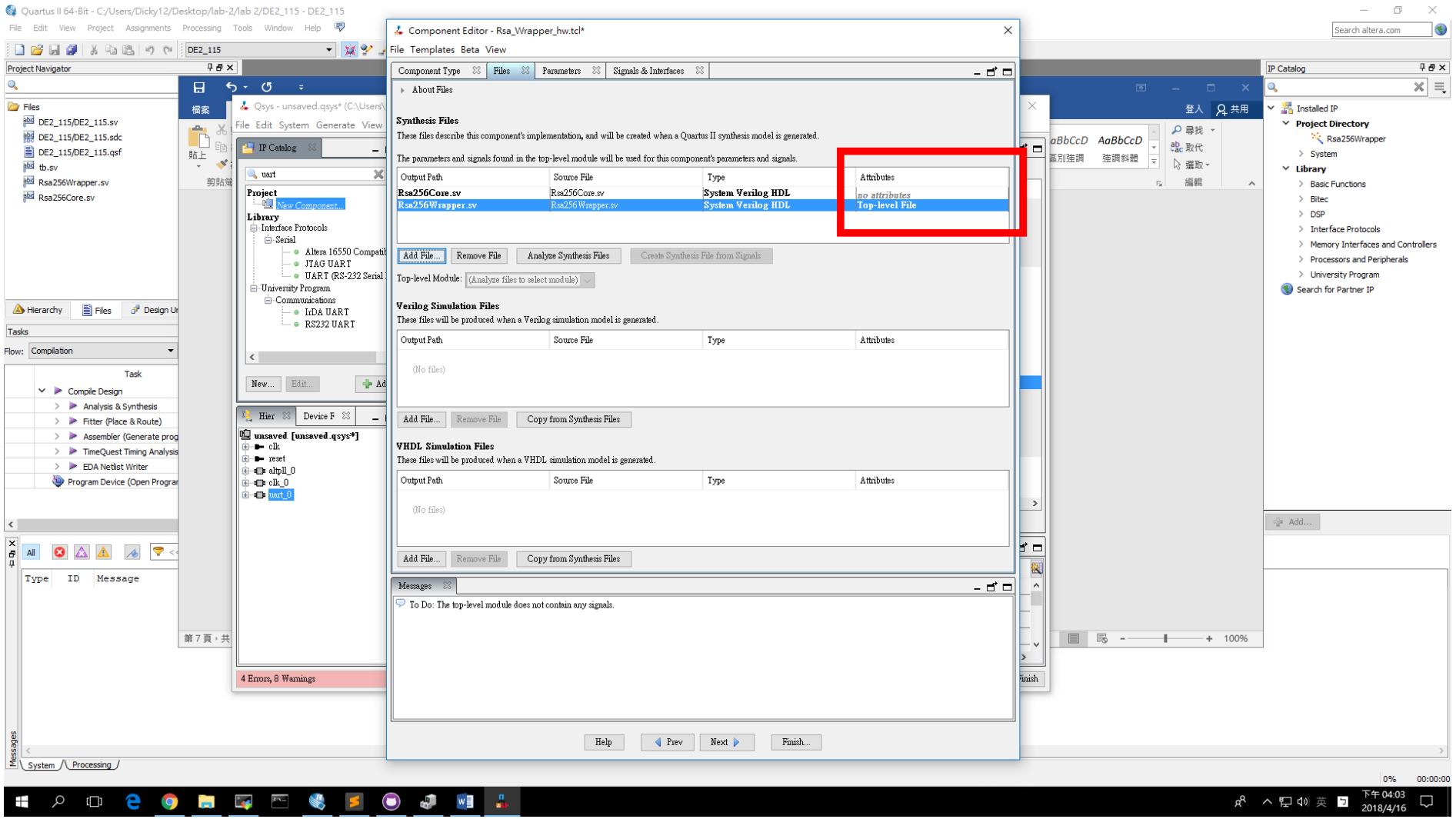
File → Add File
新增Rsa256Core.sv和Rsa256Wrapper.sv



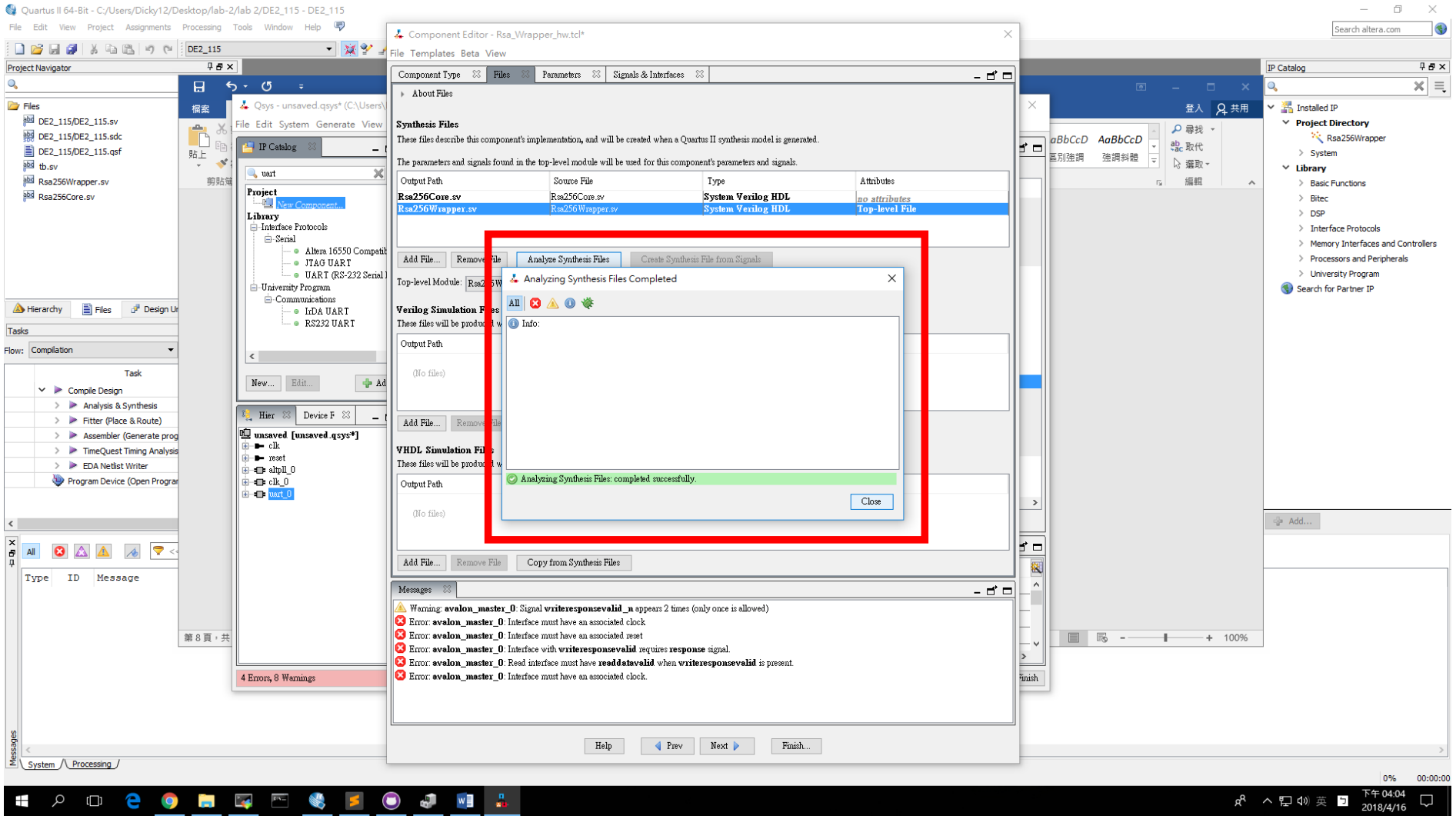
將Rsa256Wrapper改成Top level file



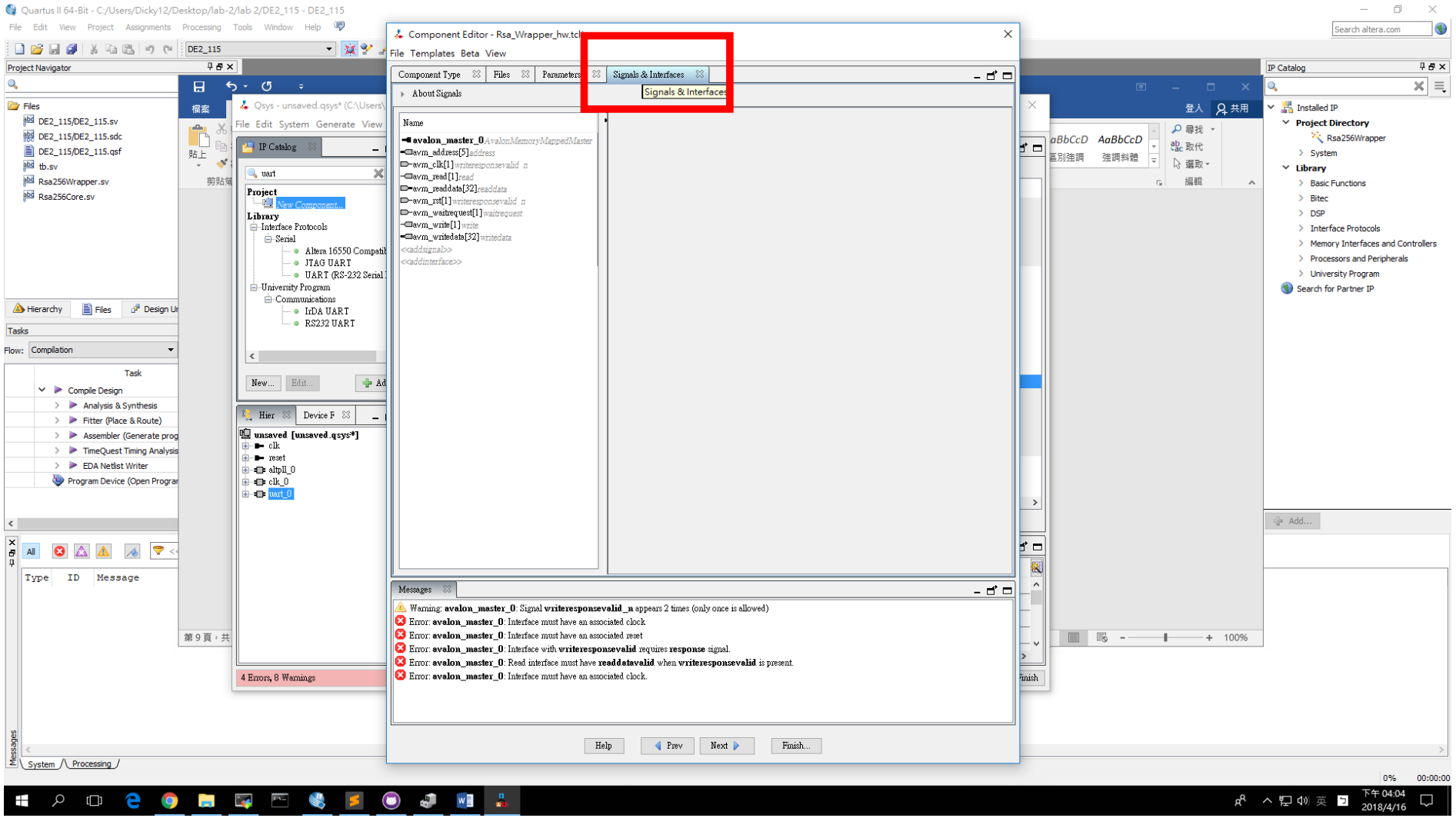
將Rsa256Wrapper改成Top level file



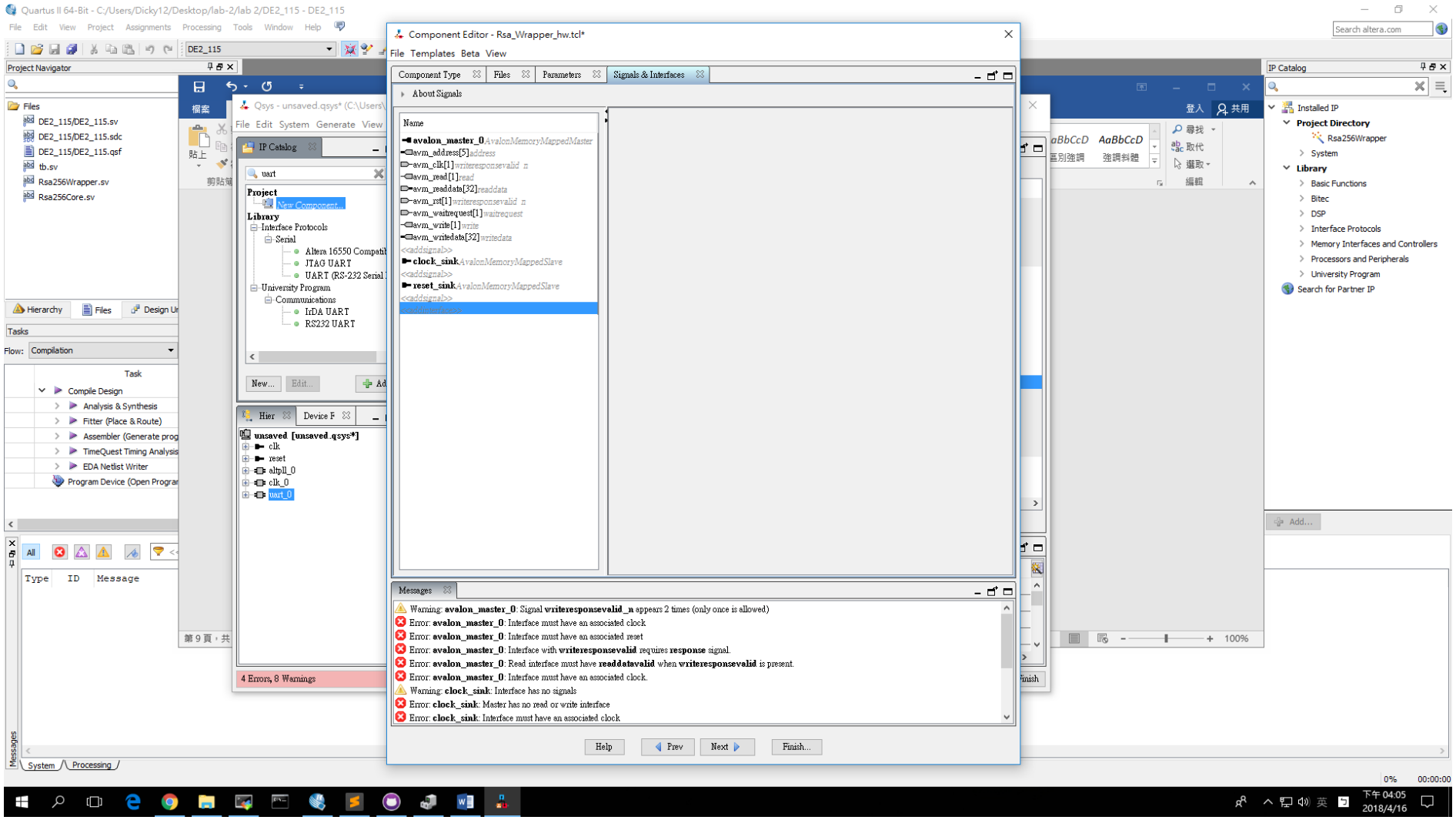
Analyze Synthesis File → Close



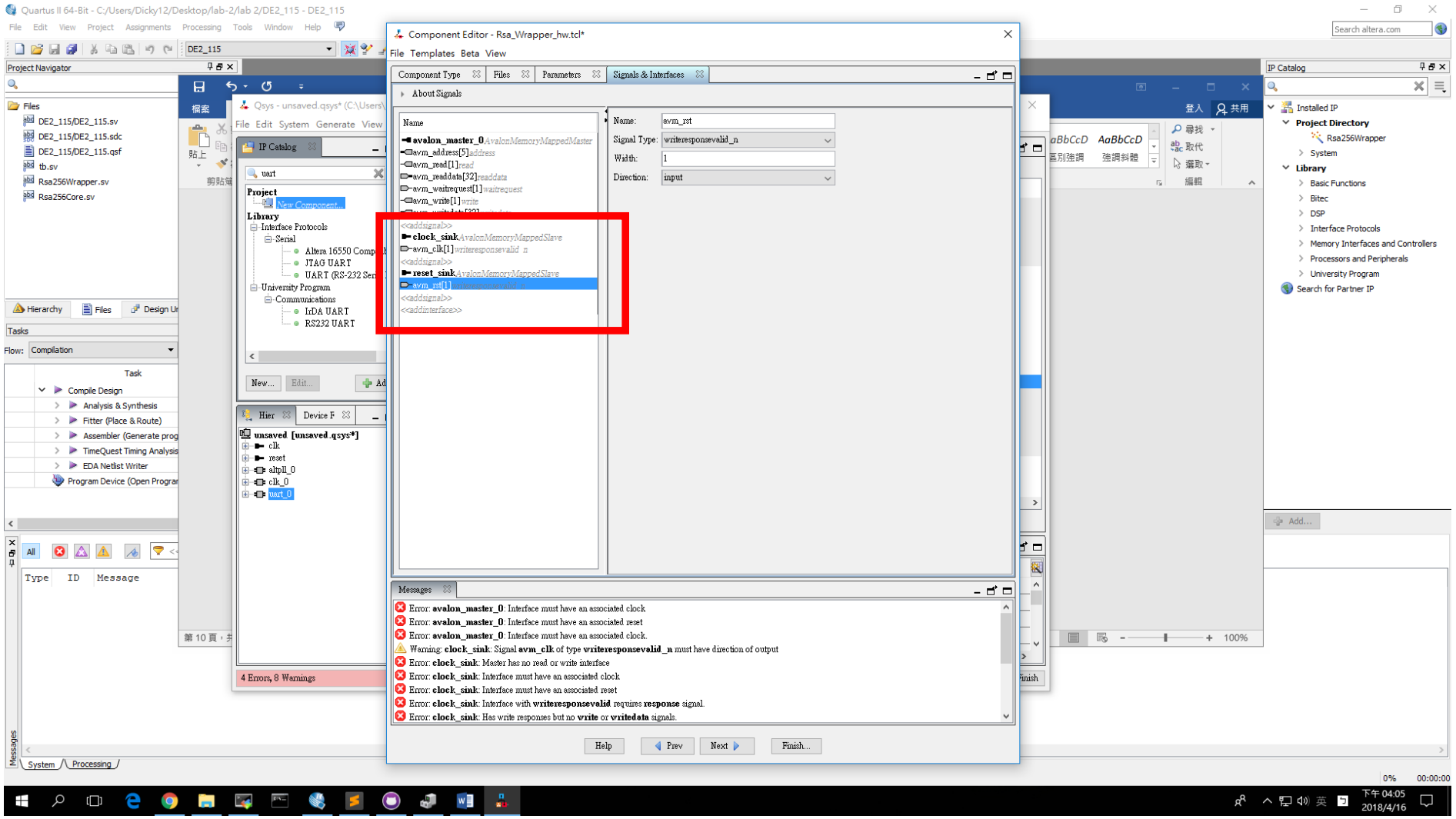
選 Signal Interface



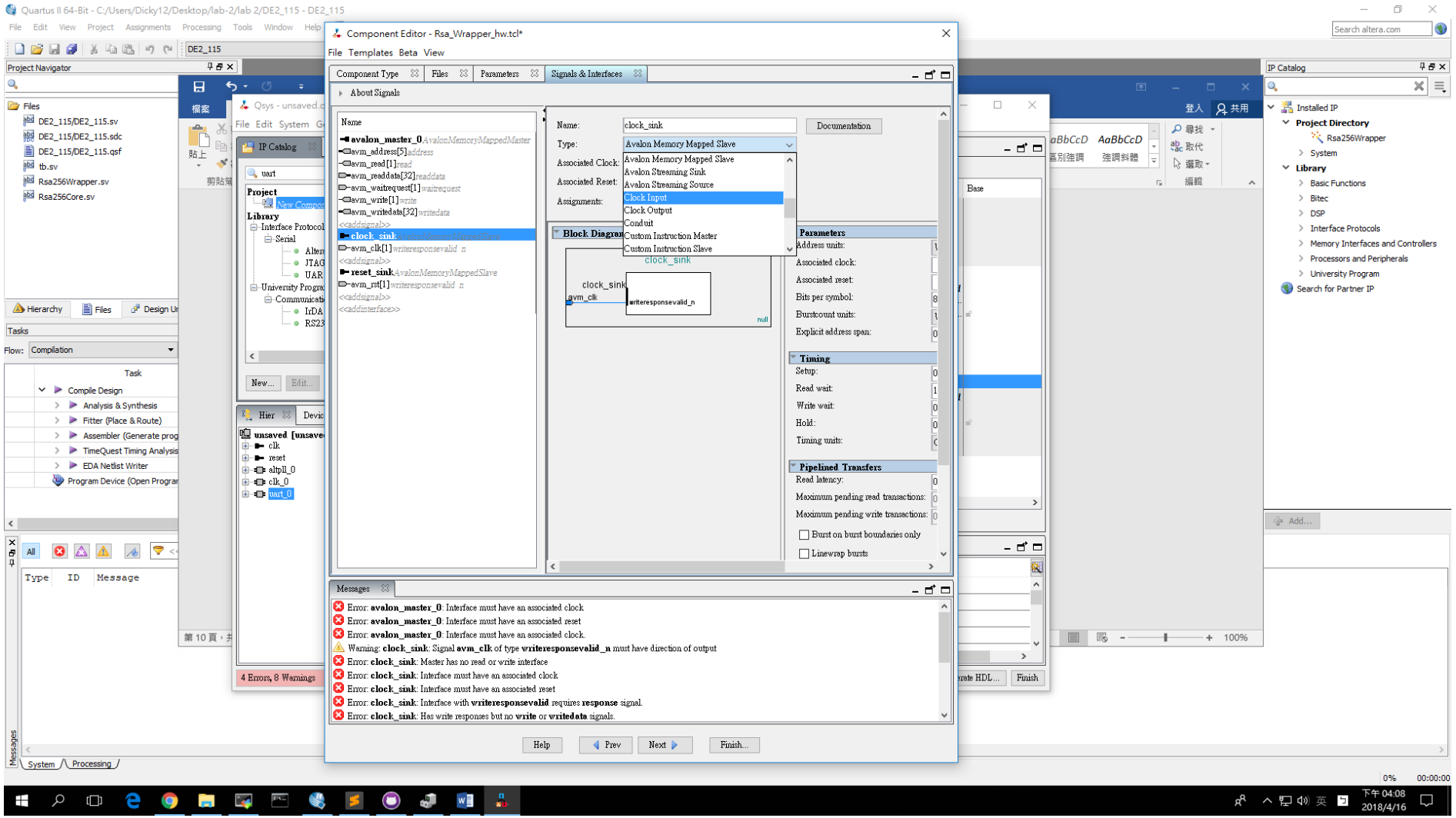
雙擊 Add interface → clock_sink
雙擊 Add interface → reset_sink



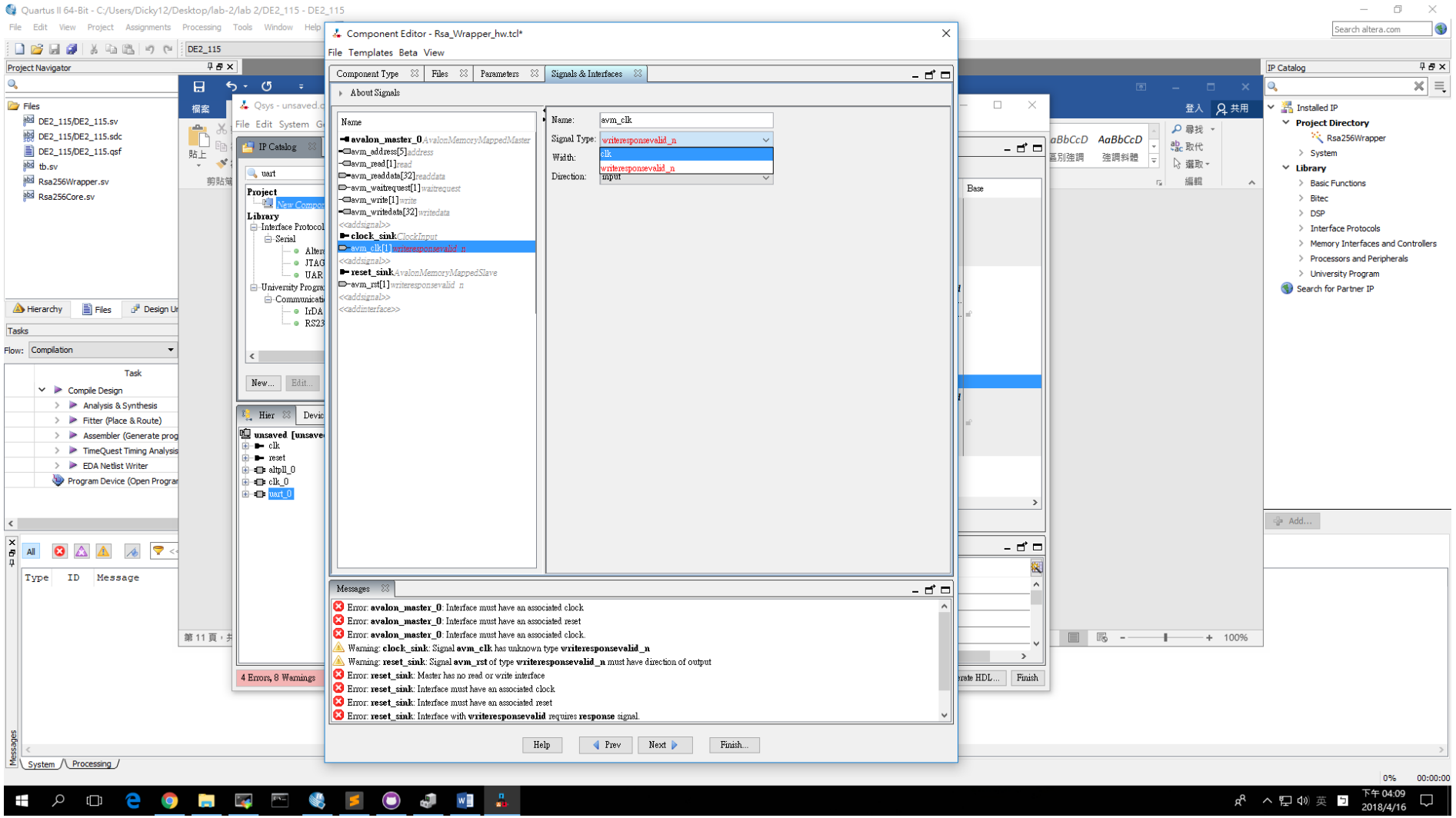
avm_clk拖曳至clock_sink下方
avm_rst拖曳至reset_sink下方



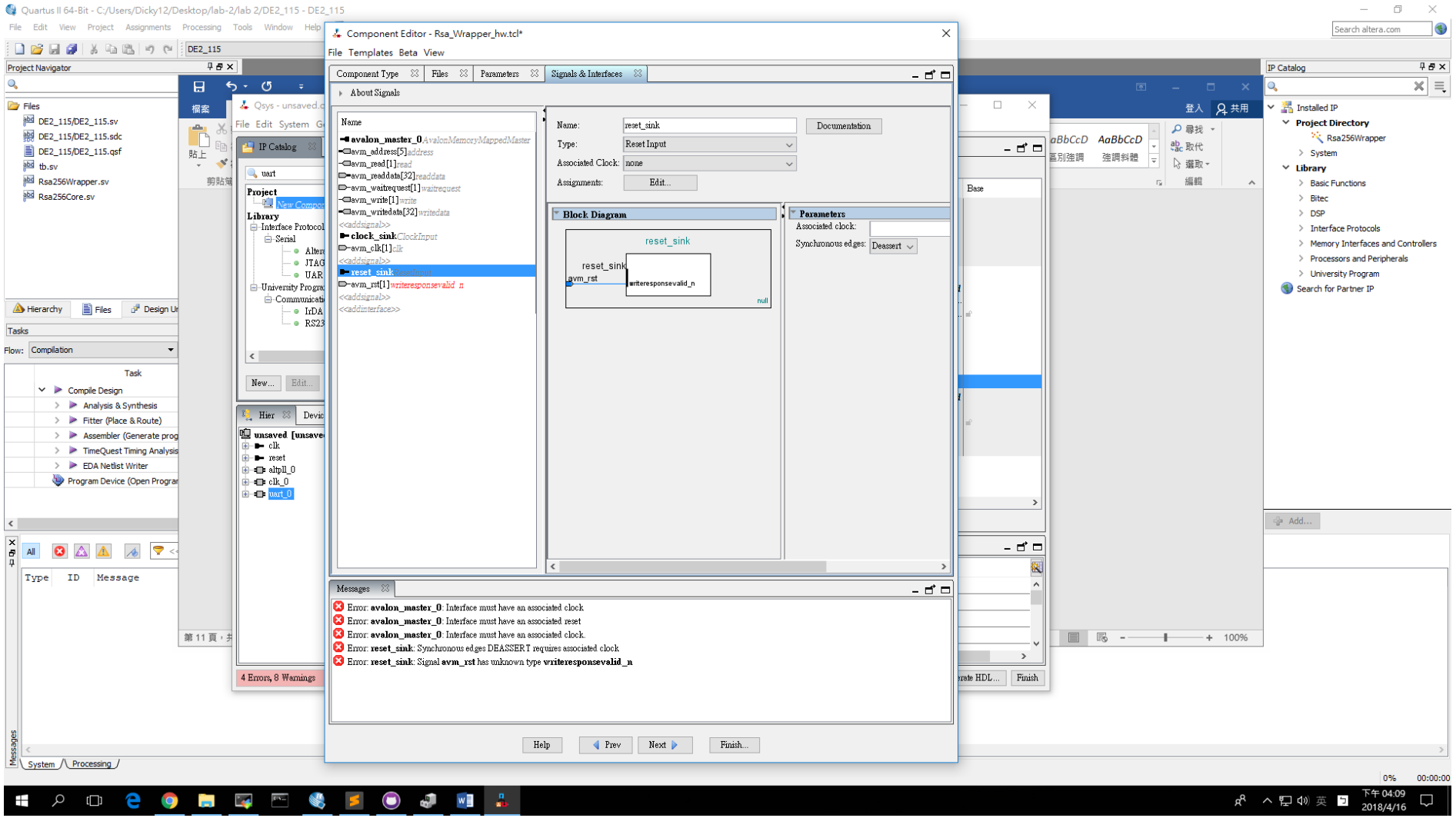
將clock_sink的Type改成Clock Input



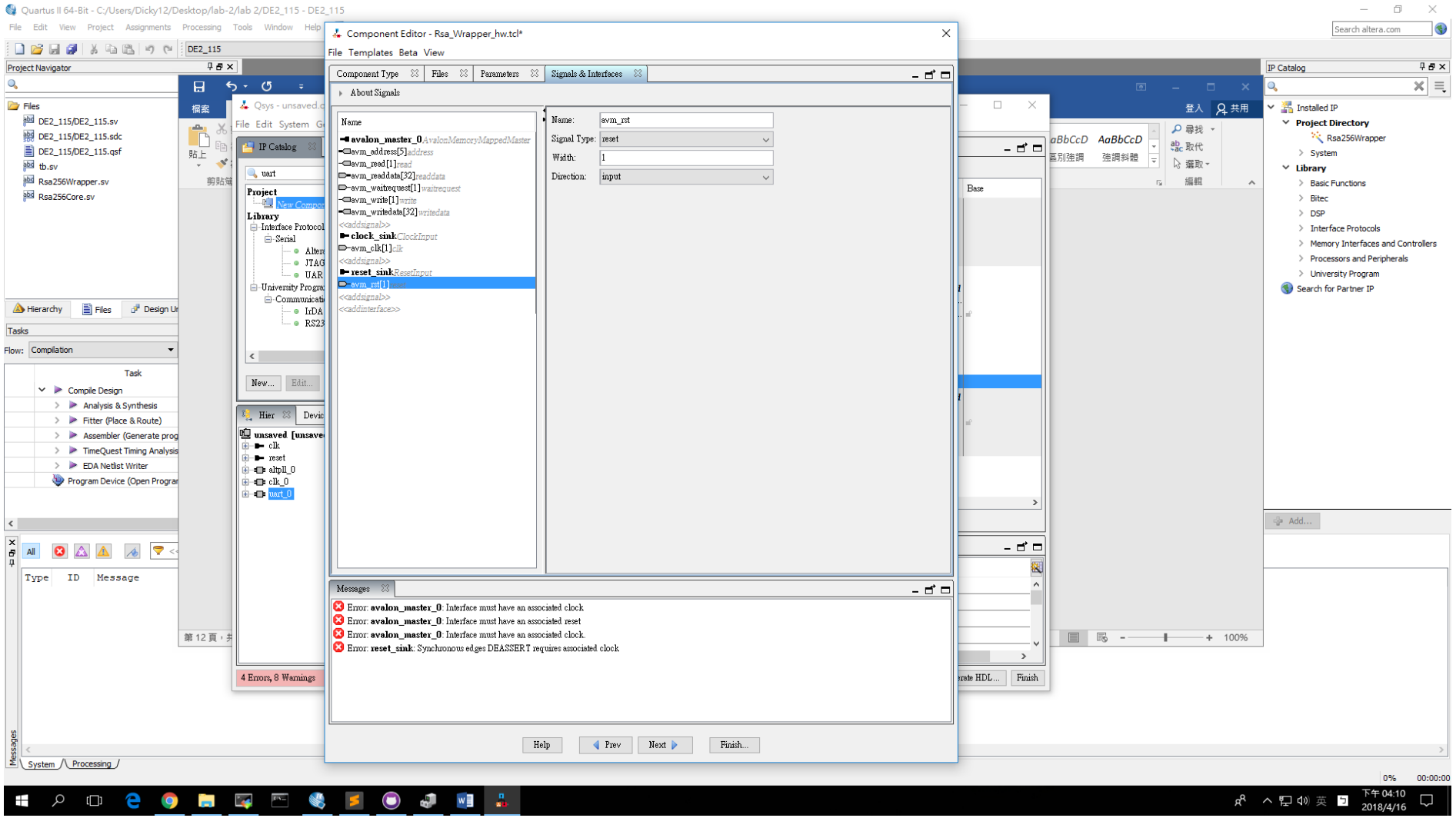
將avm_clk的Signal Type改成clk



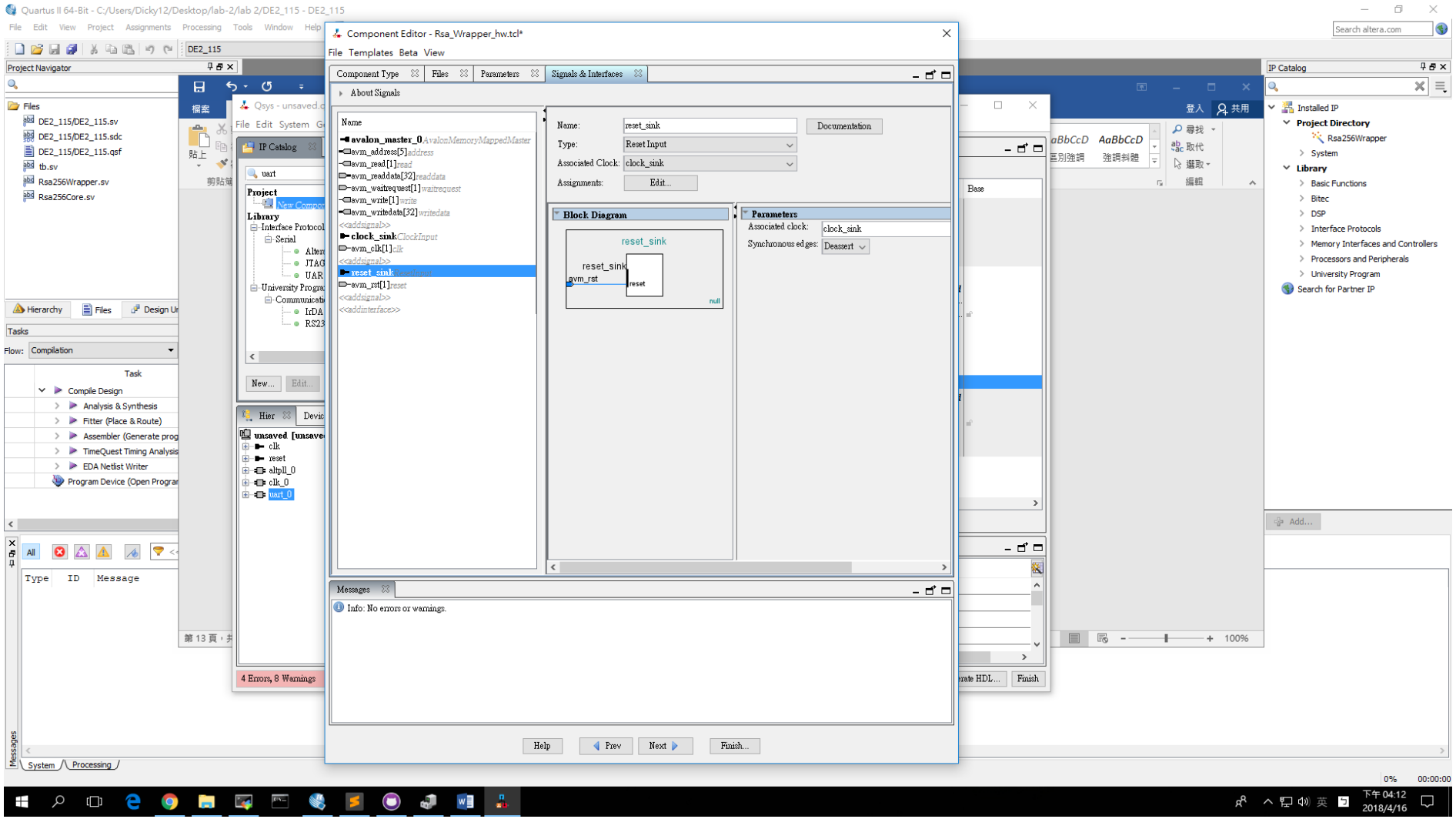
將reset_sink的Type改成Reset Input



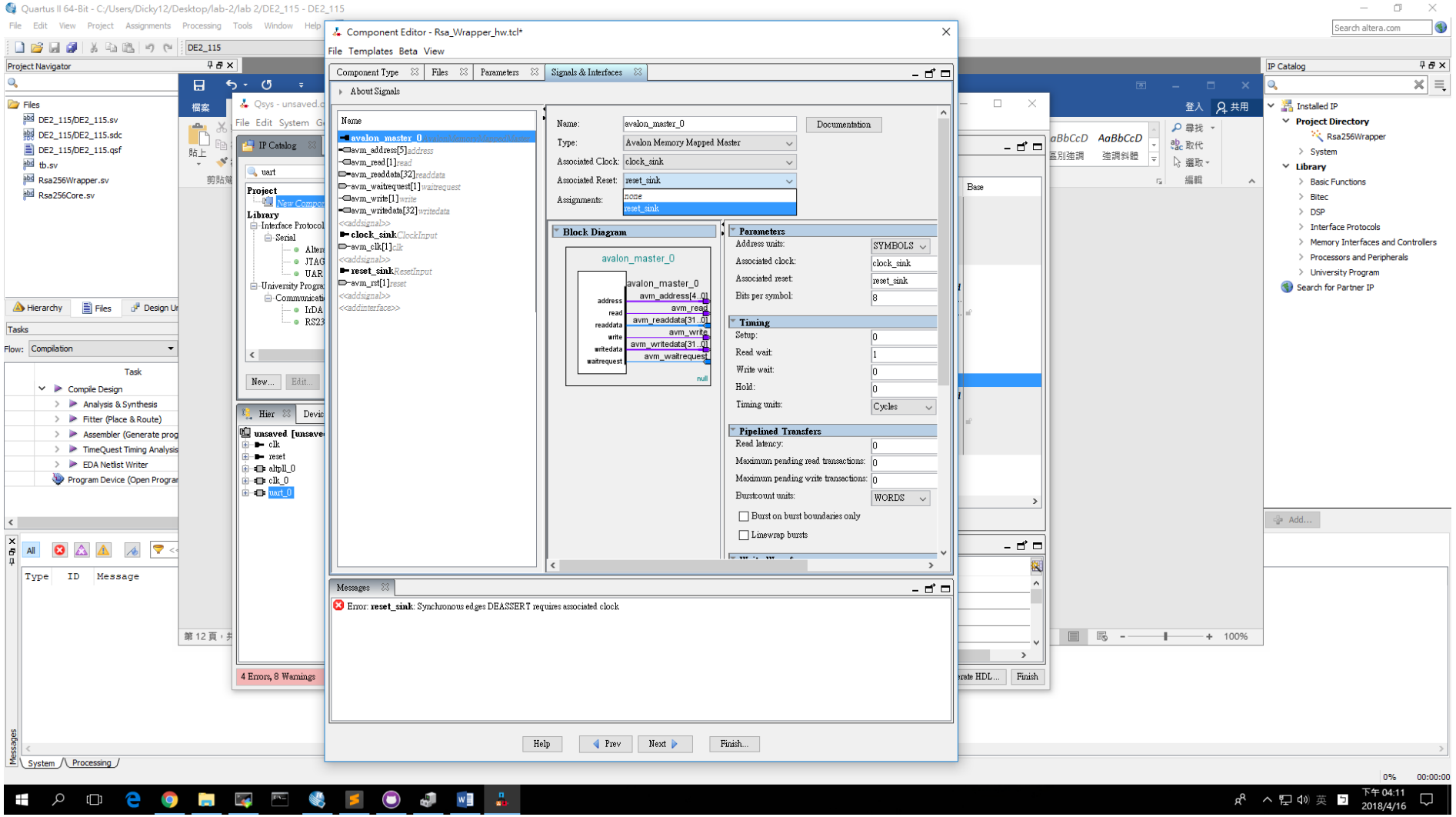
將avm_rst的Signal Type改成reset



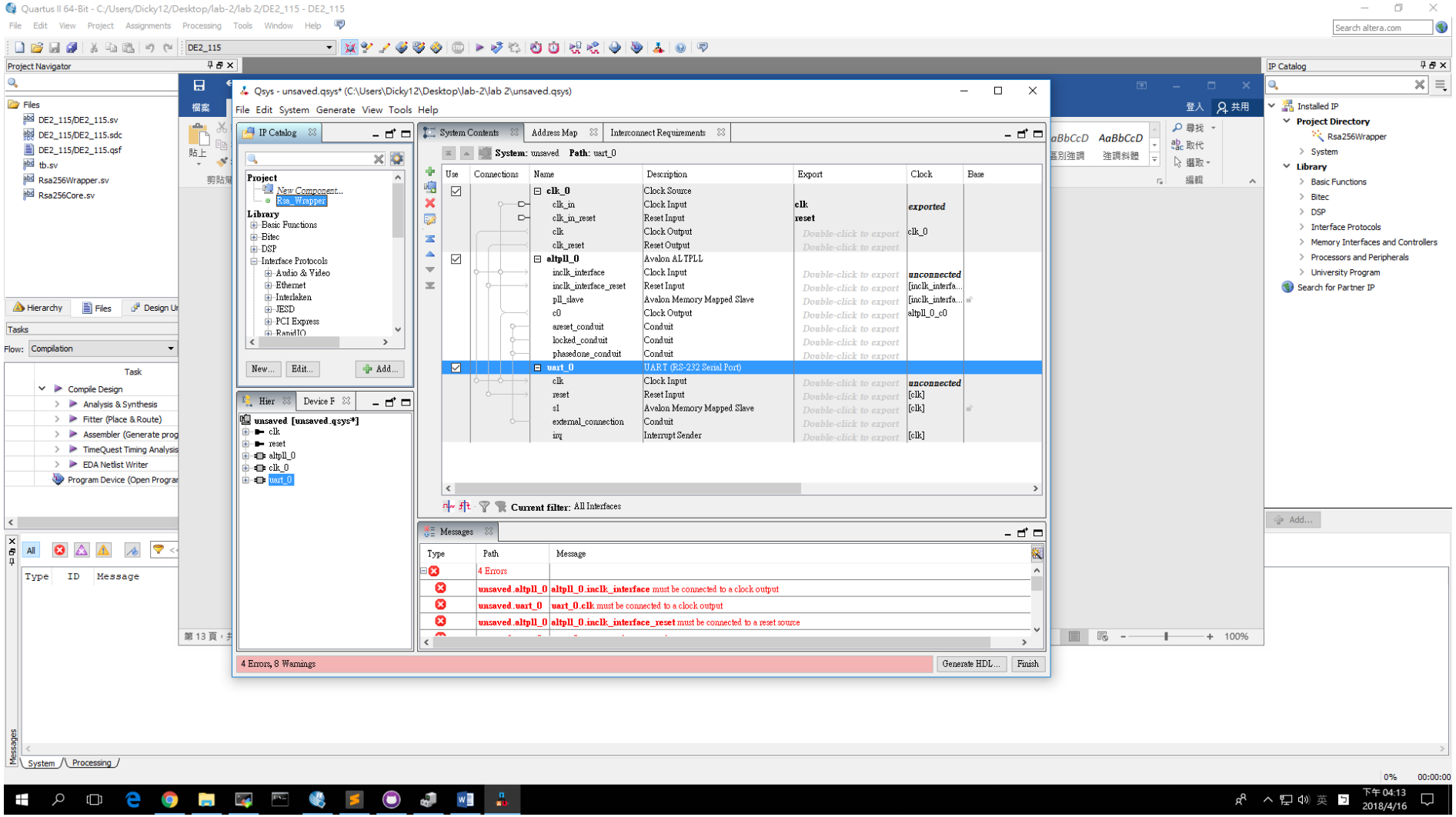
將reset_sink的associate clock改成clock_sink



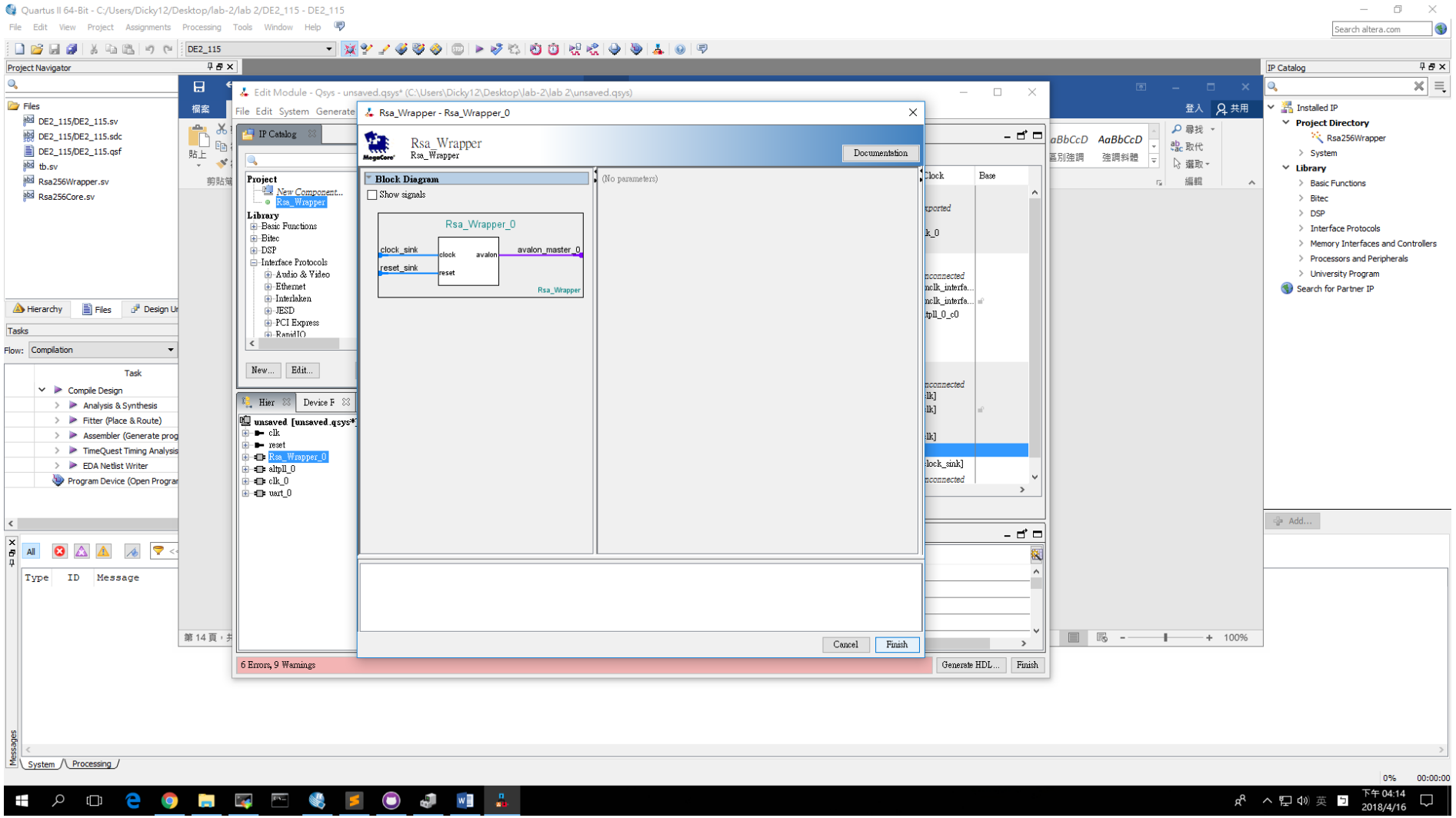
將avalon_master_0的associate clock改成clock_sink
將avalon_master_0的associate reset改成reset_sink



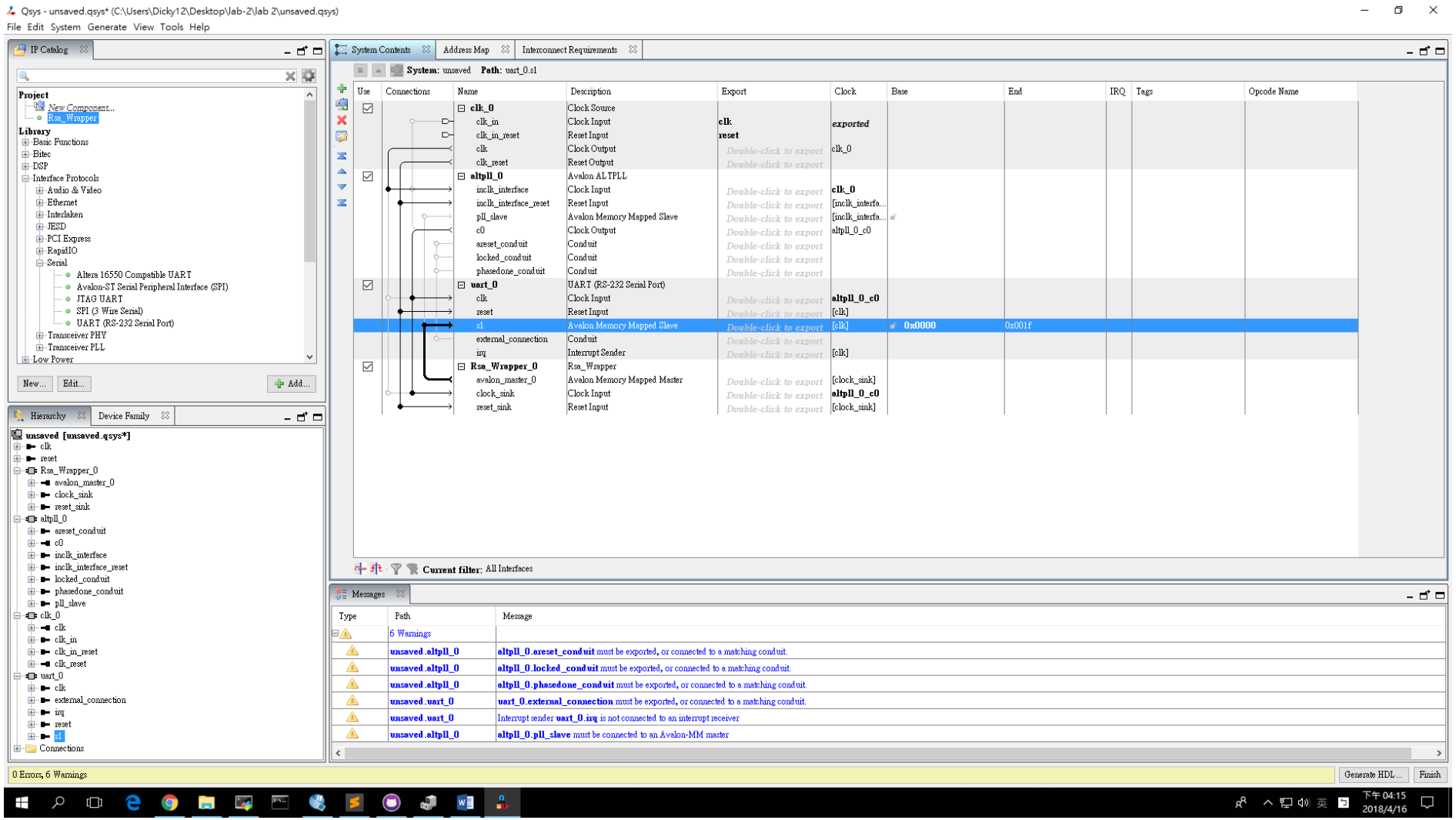
Finish → Yes, save
將搜尋列字串清空，可見RsaWrapper在New Component底下



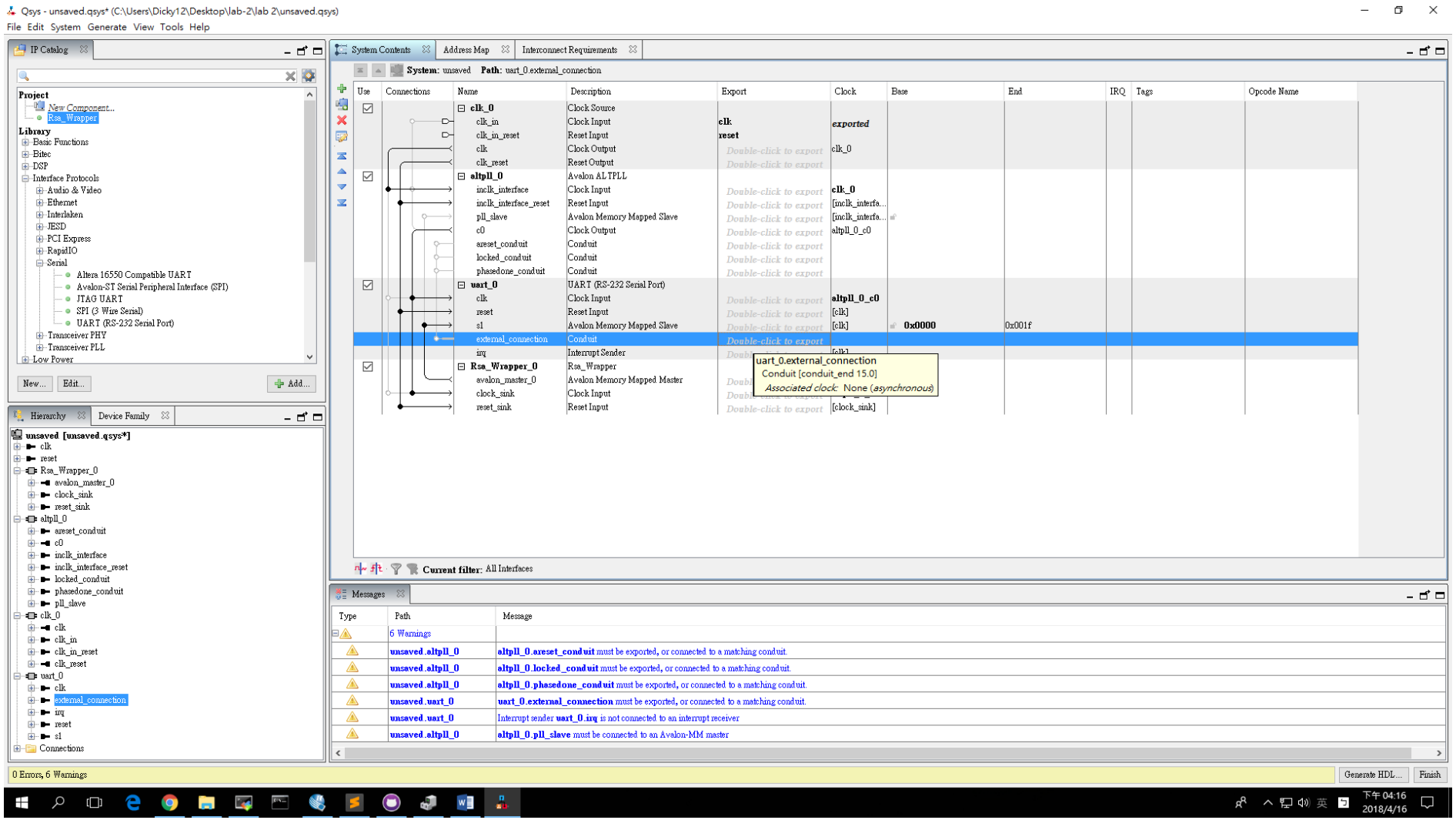
雙擊RsaWrapper → Finish



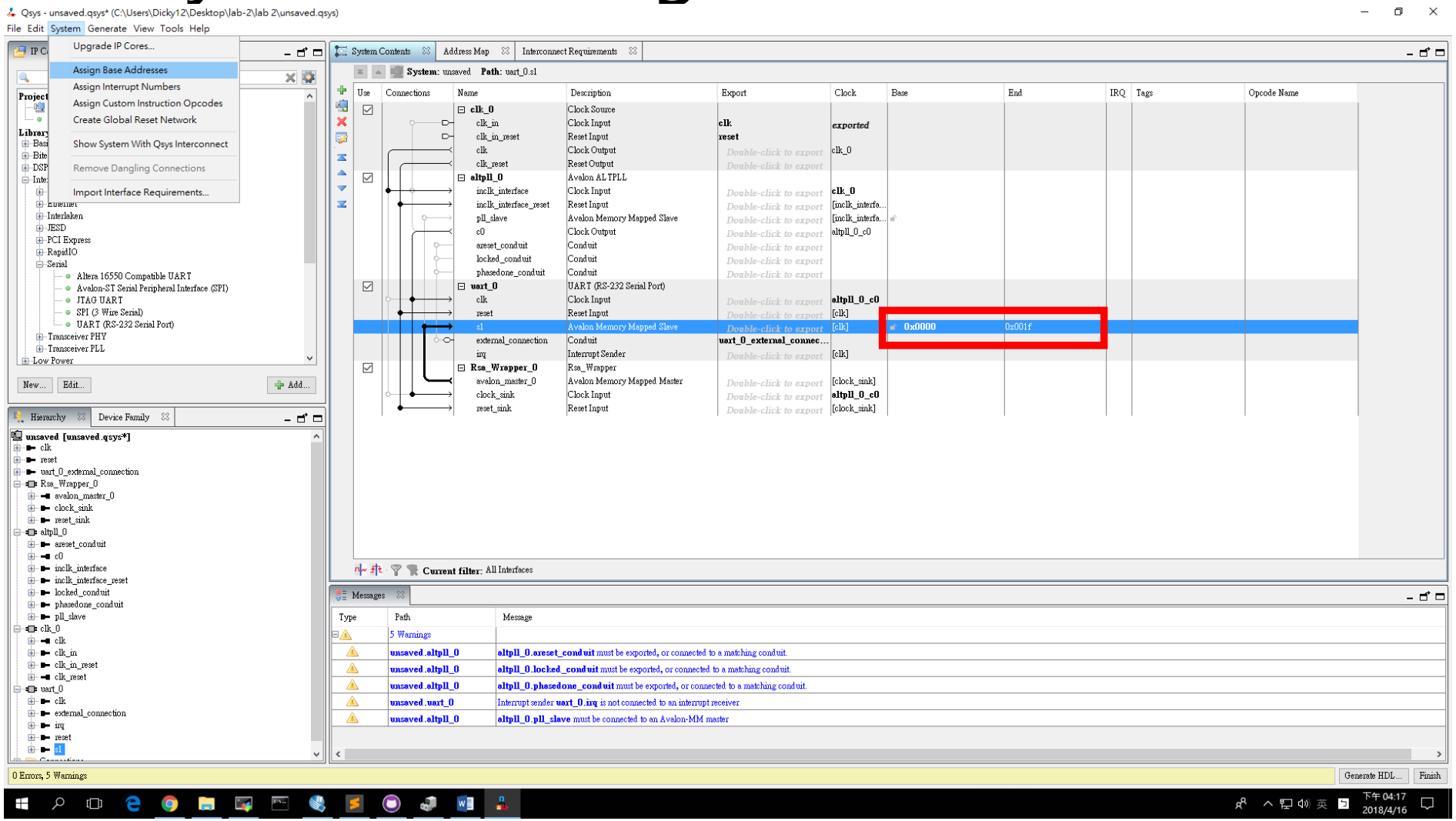
請照圖例接線 (下面Message內紅字會不見)



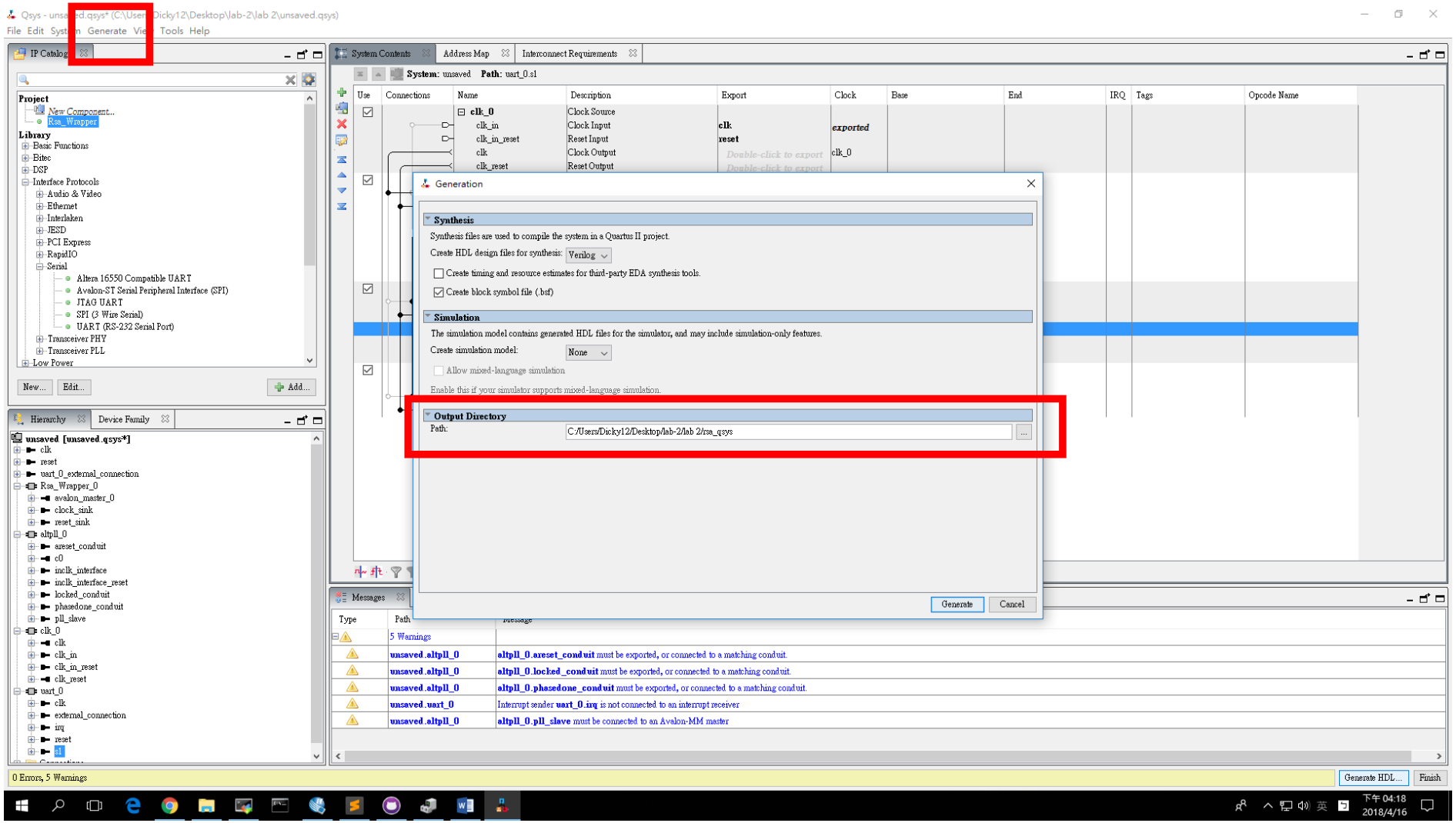
雙擊external_connection的Export欄位，Enter



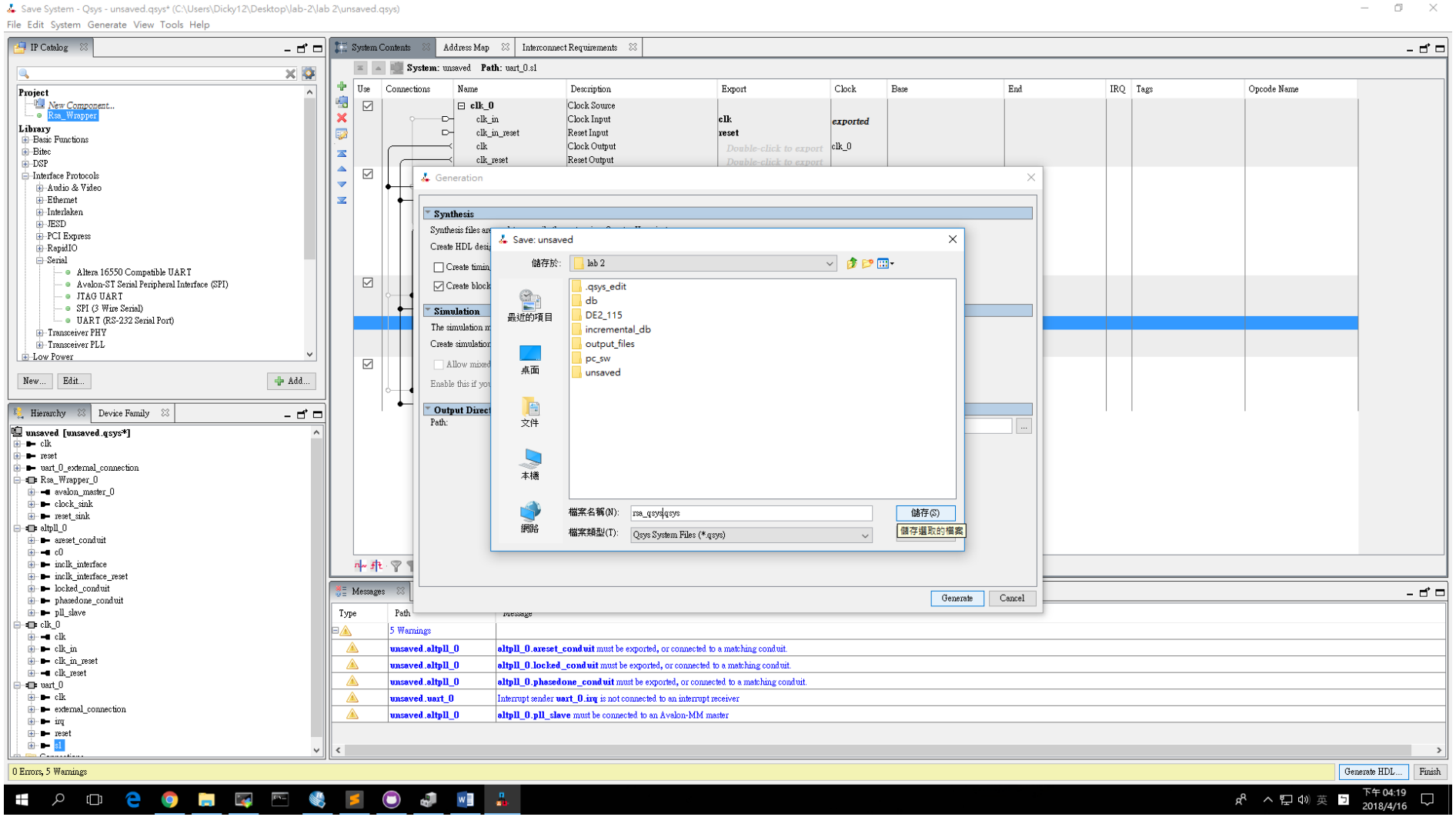
點s1的base欄位 → s1被反白選取
System → Assign Base Addresses



Generate → Generate HDL …
→ 將Output Directory的最後一層改成rsa_qsys

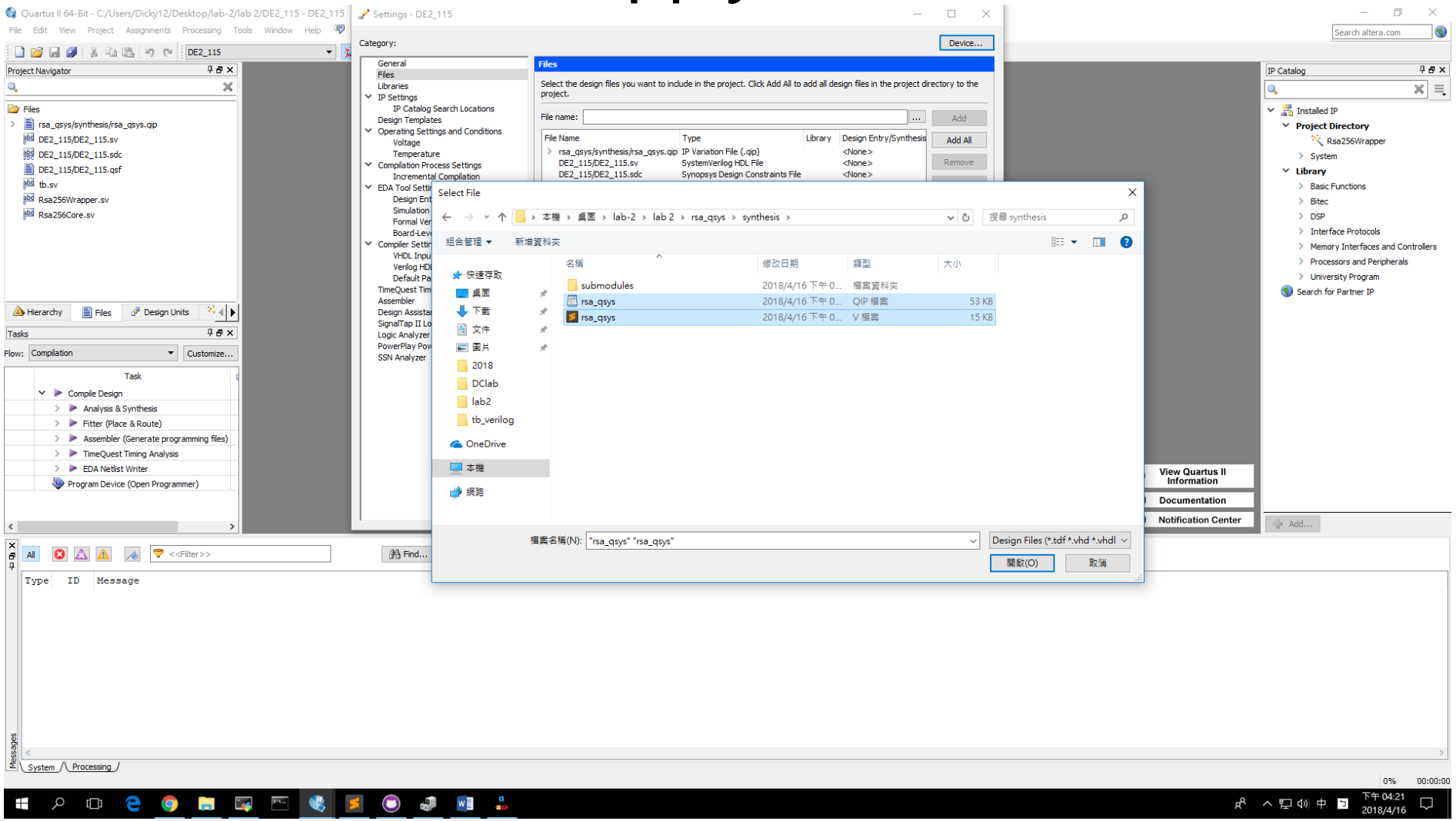


Generate → Save
檔案名稱改成rsa_qsys.qsys，儲存，完畢後按Close



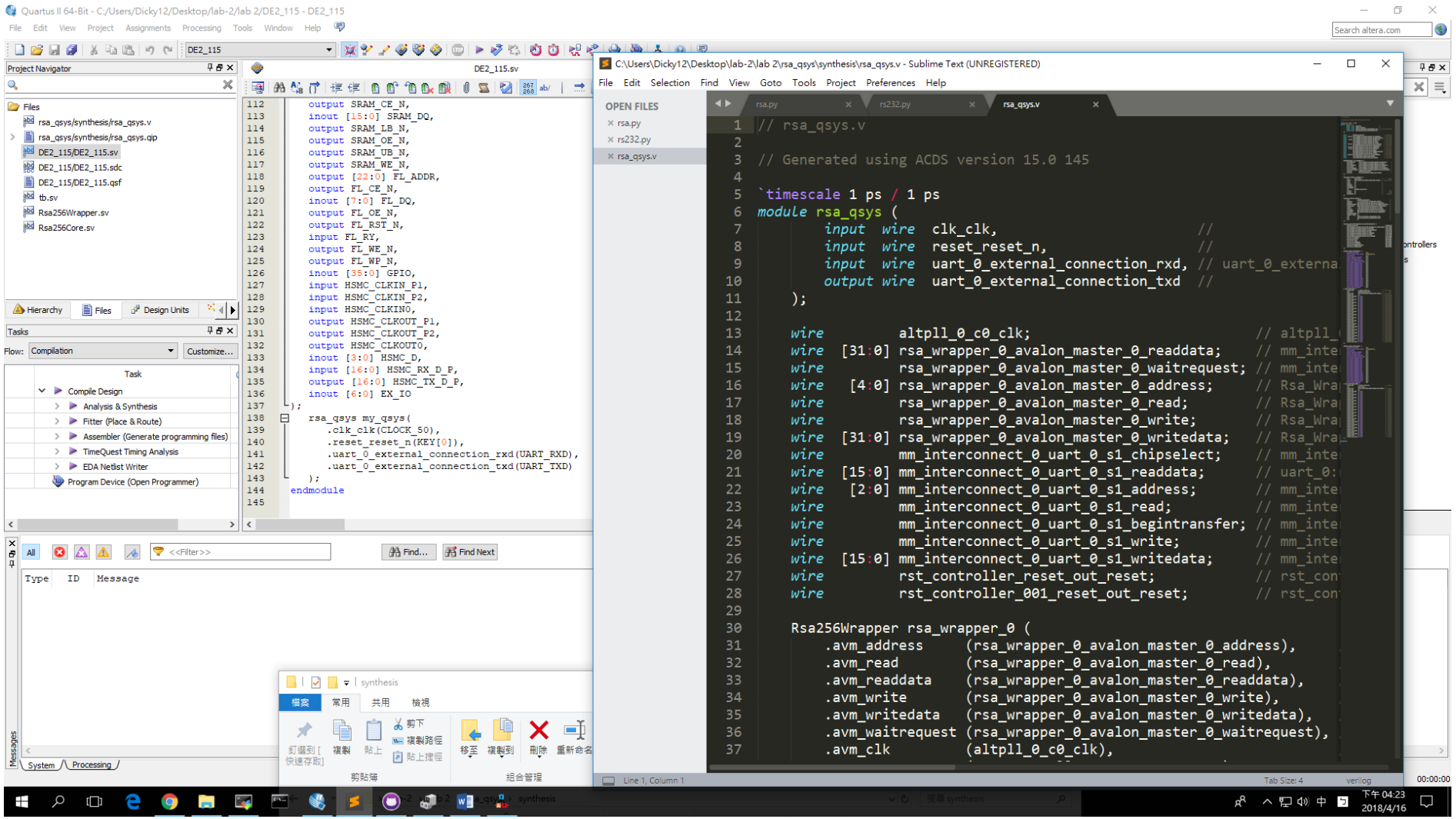
回到Quartus視窗→Assignment → Settings

新增rsa_qsys/synethesis內的rsa_qsys.qip和rsa_qsys.v → Apply → OK



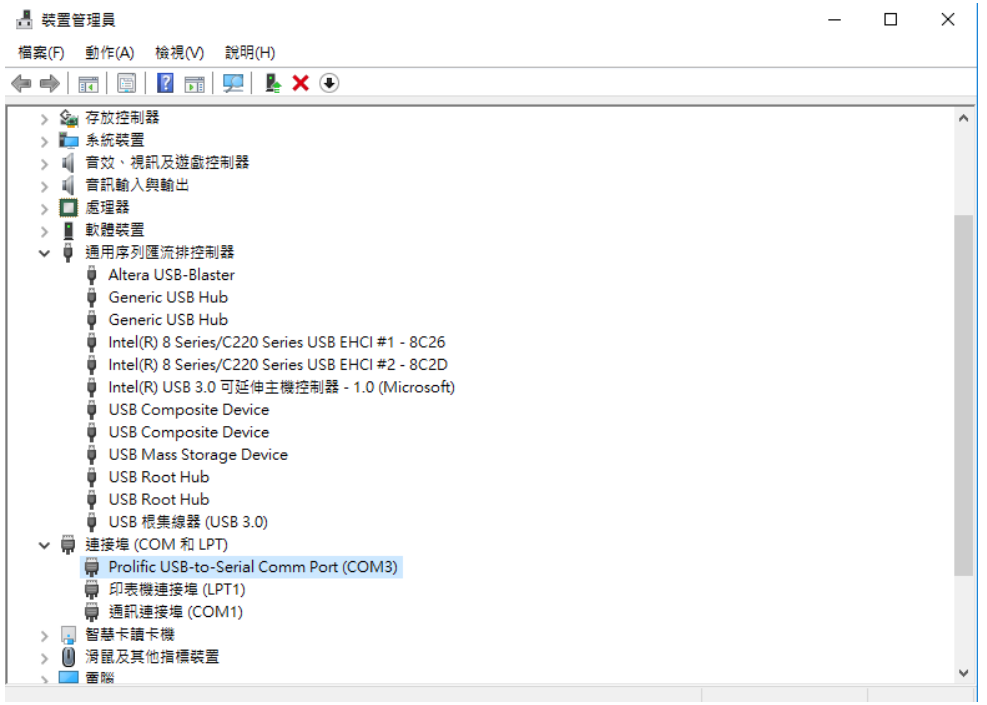
完成後可以見到Files內多出rsa_qsys.v和rsa_qsys.qip

檢查DE2_115.sv內使用rsa_qsys和rsa_qsys.v的port要相同



Appendix: Compile (Windows)

1. 裝置管理員→連接埠 (COM和LPT)→Prolific USB-to-Serial Common Port (COM?)
   1) 若沒有發現類似的裝置，則需要安裝對應型號的驅動程式
   2) COM?即為OS指派的port代號

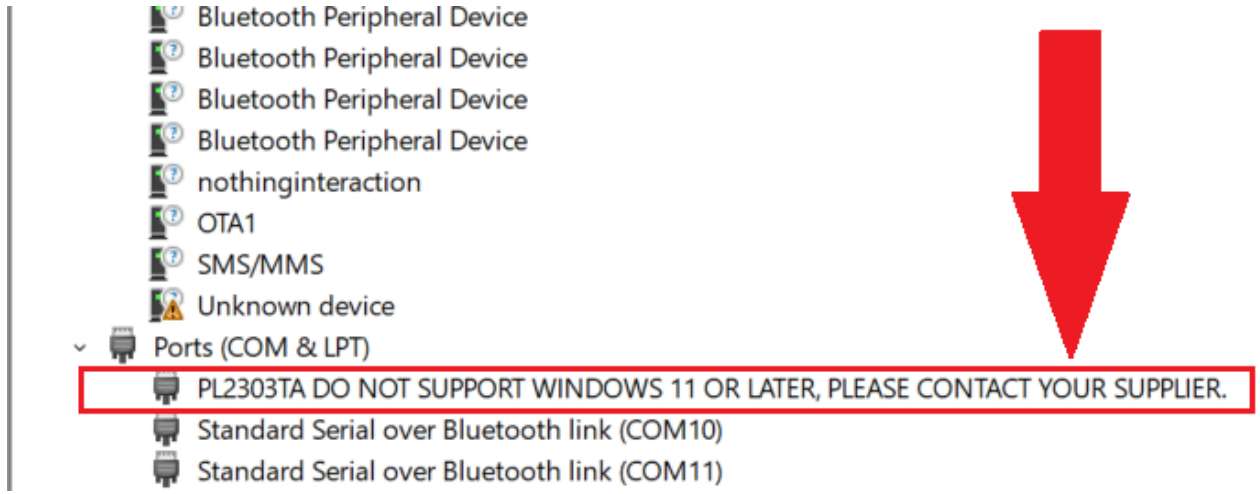


Appendix: Compile (Windows)

1. 裝置管理員→連接埠 (COM和LPT)→Prolific USB-to-Serial Common Port (COM?)

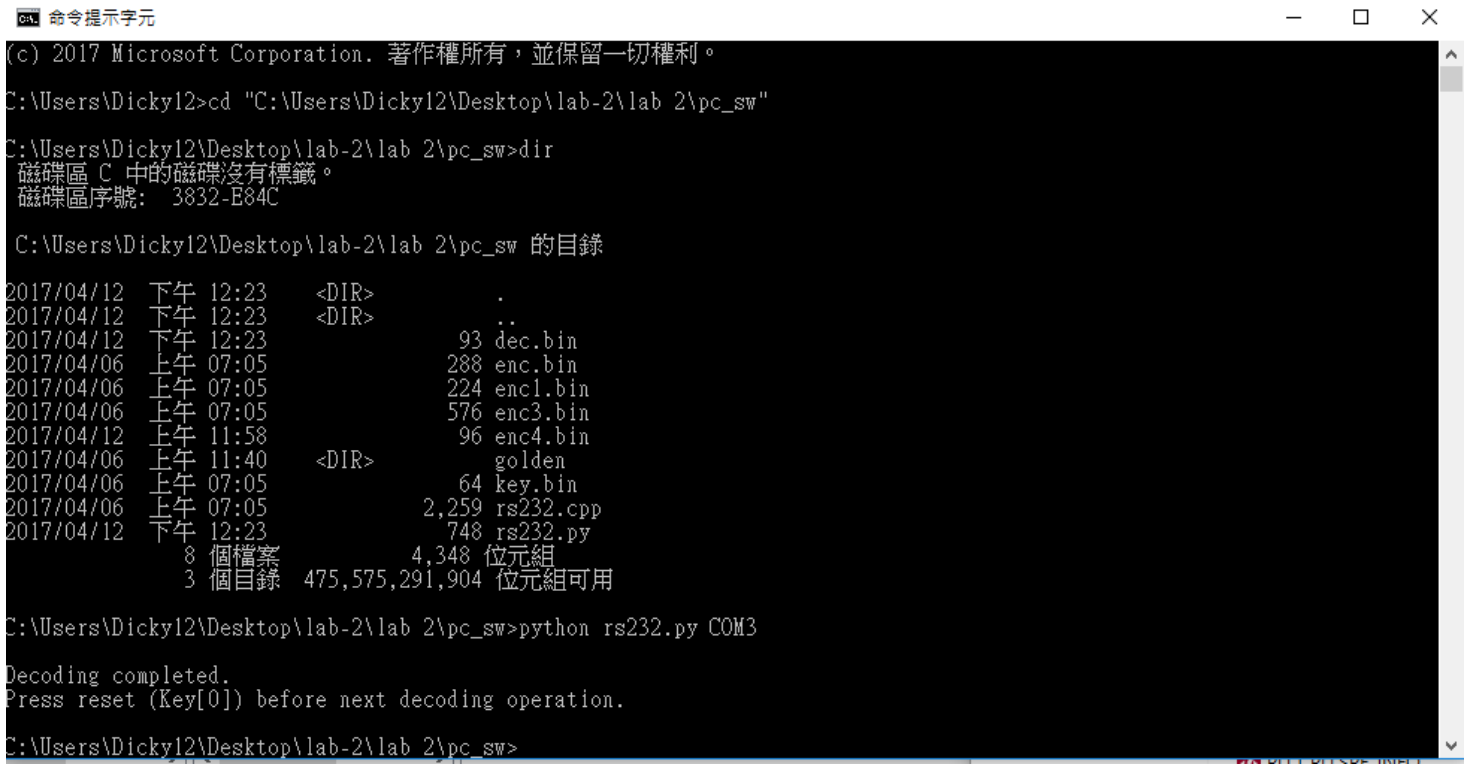
   3) 如果遇到DO NOT SUPPORT WINDOWS 11可以參考

   https://embetronicx.com/uncategorized/fixed-prolific-pl2303ta-usb-to-serial-and-windows-11/



Appendix: Compile (Windows)

2. 按下FPGA上的KEY[0] (做reset)
3. $> python rs232.py COM?，?從步驟1.可以得知



Appendix: Compile (Windows)

4. 若要測試不同的enc檔，則將rs232.py內的fp_enc = open()的檔案路徑改成golden/enc?.bin
5. 完成後，請以sublime等編輯器打開dec.bin(或對應檔名)
6. 經驗法則
    1) Compile時間過短或使用的logic elements數量過少，就算compile successful也可能出錯
    2) 重新qsys的話，可以將qsys這個資料夾砍掉直接重來
    3) Critical warning: Timing requirement not met代表qsys無法滿足timing的要求。有時候可能導致每一次compile的結果不盡相同