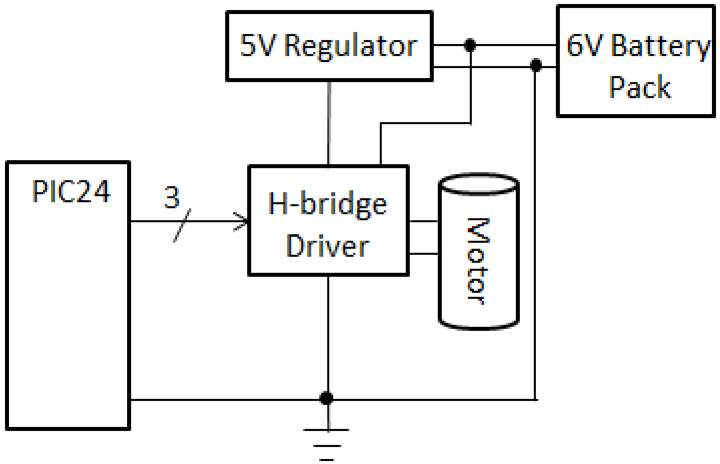
Exercise 7 Prep

DC Motor Control and Speed Monitoring

Exercise & Overview

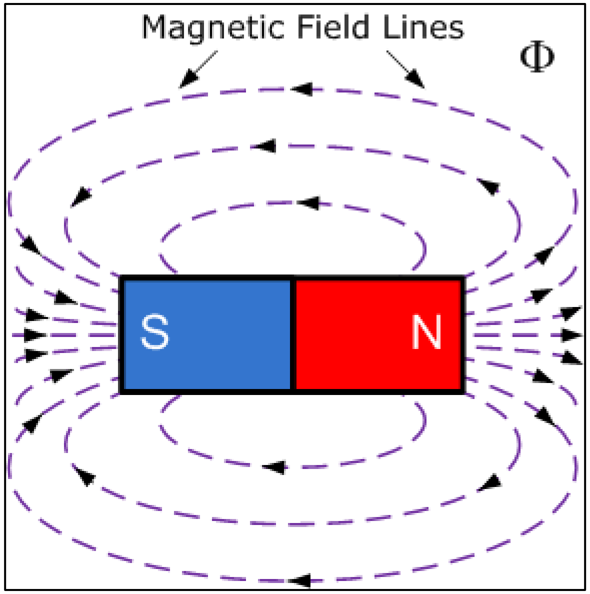
- Hardware Components
  - DC gear motor
  - H-bridge motor driver
  - Voltage regulator



- Software
  - Part A - simple on/off control of motor
  - Part B – speed control with PWM
  - Part C – measure speed using motor encoder
- <u>Work in your Project 3 teams</u>

DC Motor Basics

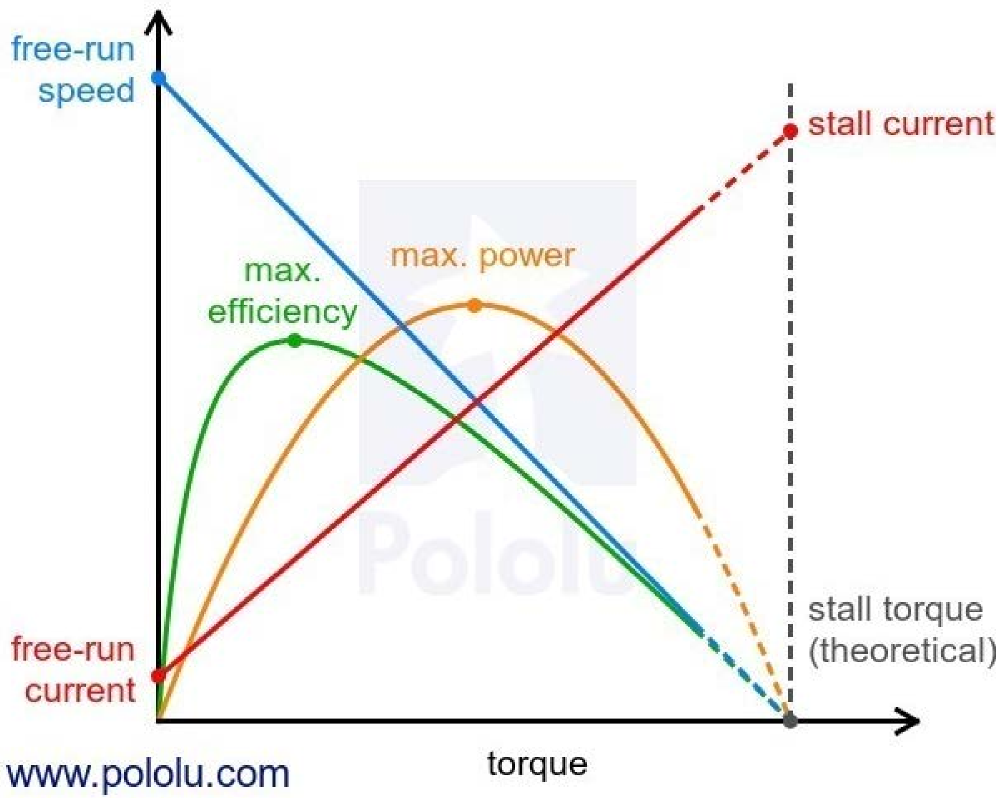
An element conducting current will experience a mechanical force when in a magnetic field



Gear Motor

- DC motor with non-removable gear reducer (gearhead).
- Available in many gear ratios for different speed and torque requirements
- Do not have the positional control of servo motors, only speed/direction control, similar to continuous motion servos.

Gearmotor Characteristics



Torque = force that causes rotation (N*m)

Stall – situation when applied torque stops motor spinning

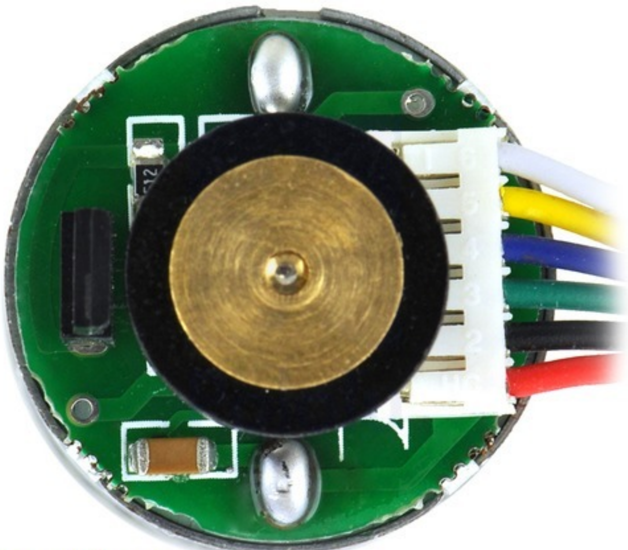
Stall current and torque and free run speed and current for our motors available on spec sheet on Nexus

4 Motors Available

- All have different speeds, based on gear ratio
- All have 250mA current draw at no load
- All have 2.4A stall current (current draw when stalled)

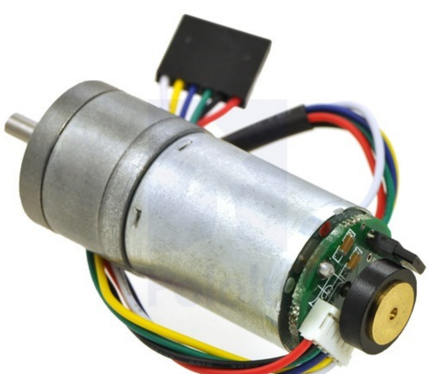
Number		Item Description
2282		9.7:1 Metal Gearmotor 25Dx48L mm LP 6V with 48 CPR Encoder
2284		34:1 Metal Gearmotor 25Dx52L mm LP 6V with 48 CPR Encoder
2281		4.4:1 Metal Gearmotor 25Dx48L mm LP 6V with 48 CPR Encoder
2283		20.4:1 Metal Gearmotor 25Dx50L mm LP 6V with 48 CPR Encoder

Built In Encoder



www.pololu.com

Color	Function
Red	motor power (connects to one motor terminal)
Black	motor power (connects to the other motor terminal)
Green	encoder GND
Blue	encoder Vcc (3.5 – 20 V)
Yellow	encoder A output
White	encoder B output



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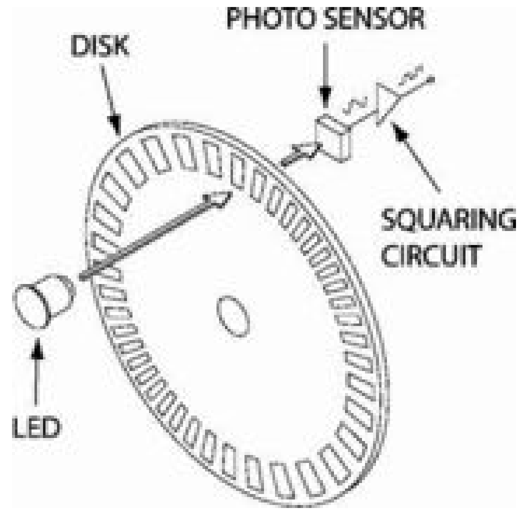
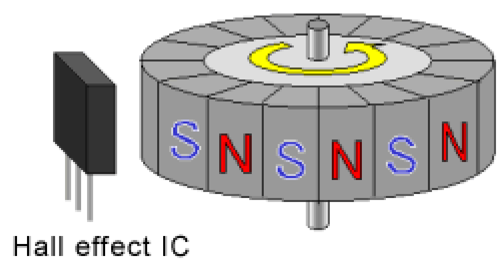
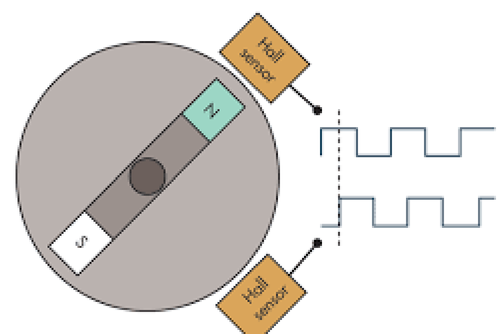
Motor Shaft Encoder

- “Rotary Encoder”
  - Optical



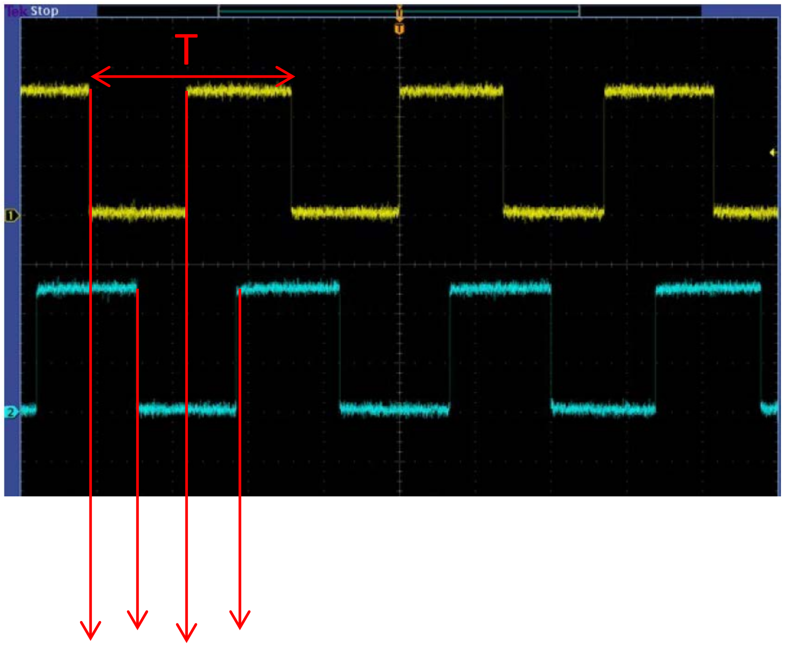
  - Magnetic





Our Gearbox Motor

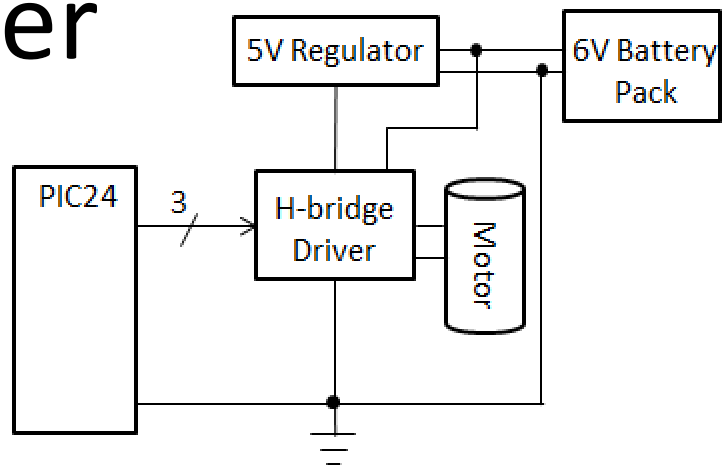
- Two sensors, 90 degrees out of phase
- 48 Counts Per Revolution (CPR) Encoder*
- 12 Periods Per Revolution (PPR)
- **For gear ratio 9.68:1**
  - <u>Periods</u> per revolution of gear shaft = 12(9.68) = 116.16

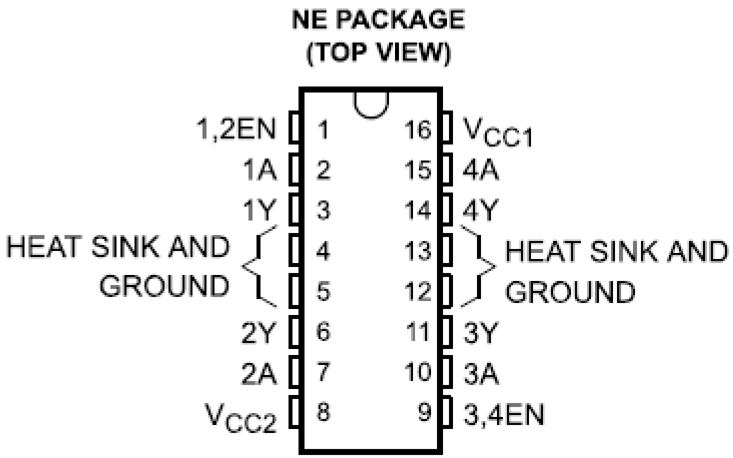


Gear Ratio	PPR
4.4:1	52.8
9.68:1	116.16
20.4:1	244.8
34:1	408.17

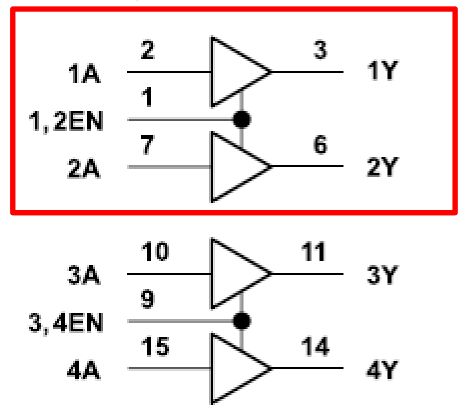
* Note that a “count” is specified as a rising or falling edge of both decoder signals, so to get the number of PERIODs of a single decoder, we would need to divide this by 4, and so there are 12 encoder PERIODS per revolution.

Motor Driver





Logical behavior



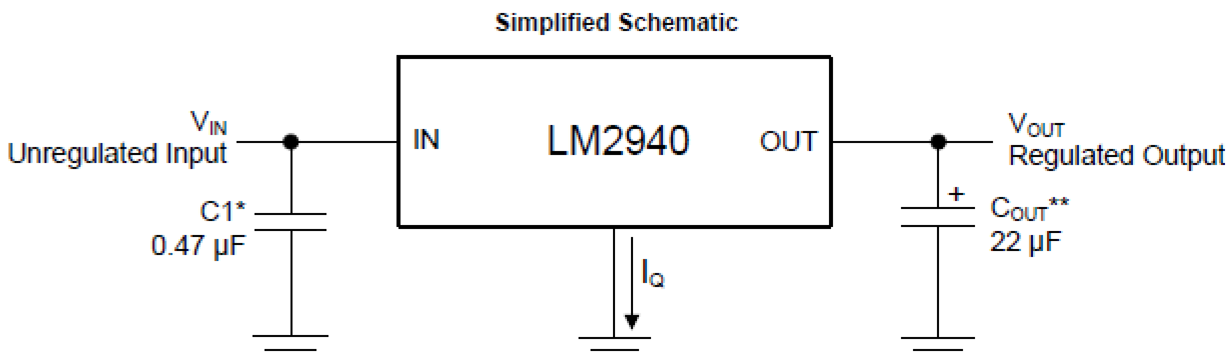
Details of electronics in datasheet

7.2 Recommended Operating Conditions

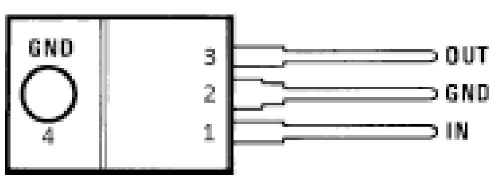
over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC1}	Logic supply voltage	4.5	5.5	V
V_{CC2}	Output supply voltage	4.5	36	V
V_{IH}	High-level input voltage	2	5.5	V
V_{IL}	Low-level input voltage	–0.3[1]	0.8	V

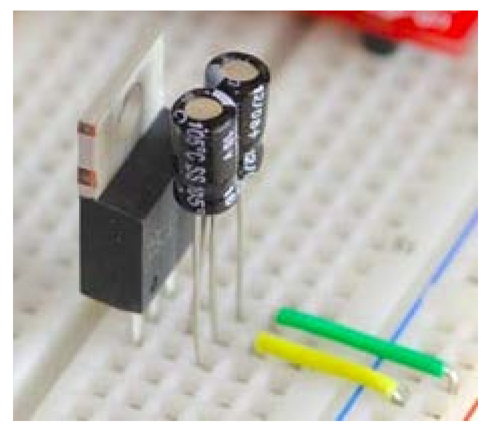
5V Regulator



TO-220 (NDE) Package
4 Pins
Front View



Connect capacitors very close to the regulator

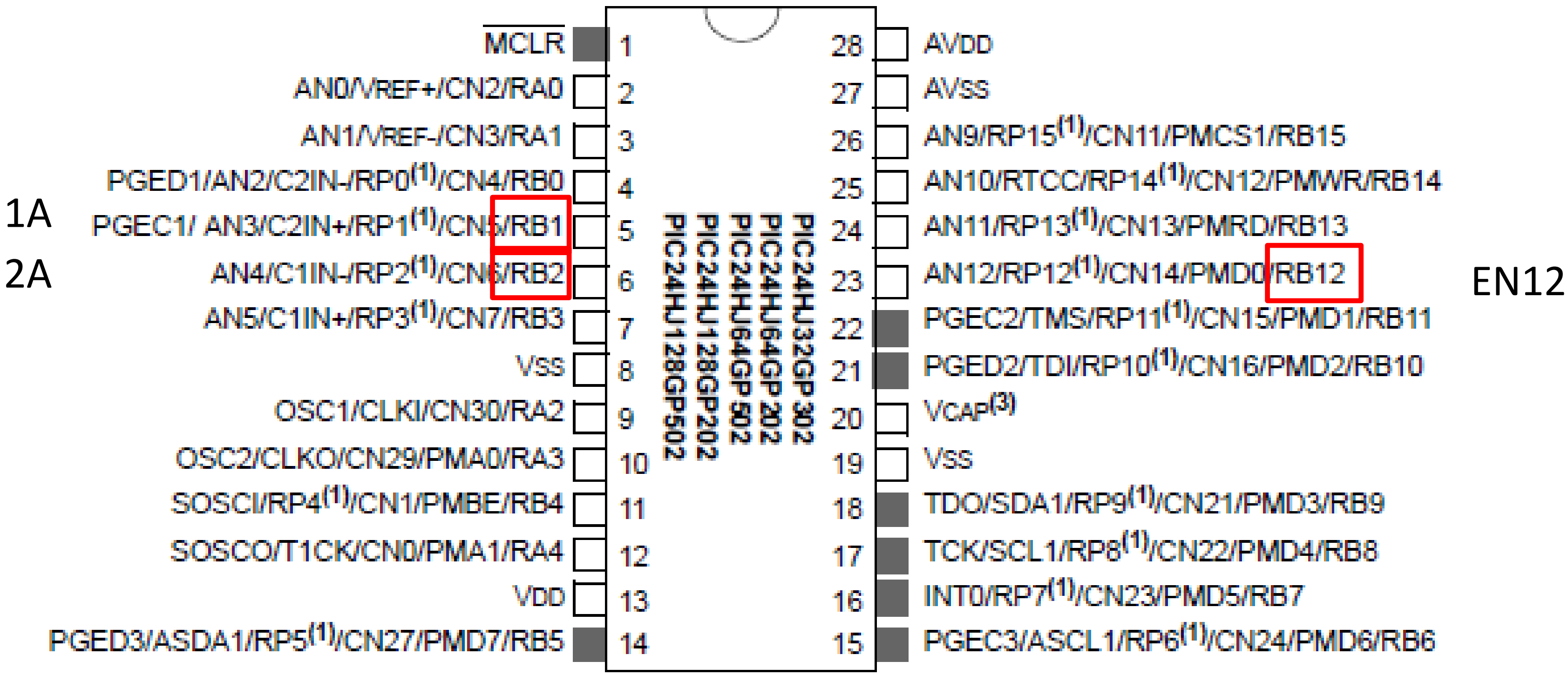


Software

Part A – Simple on-off control using Port B pins

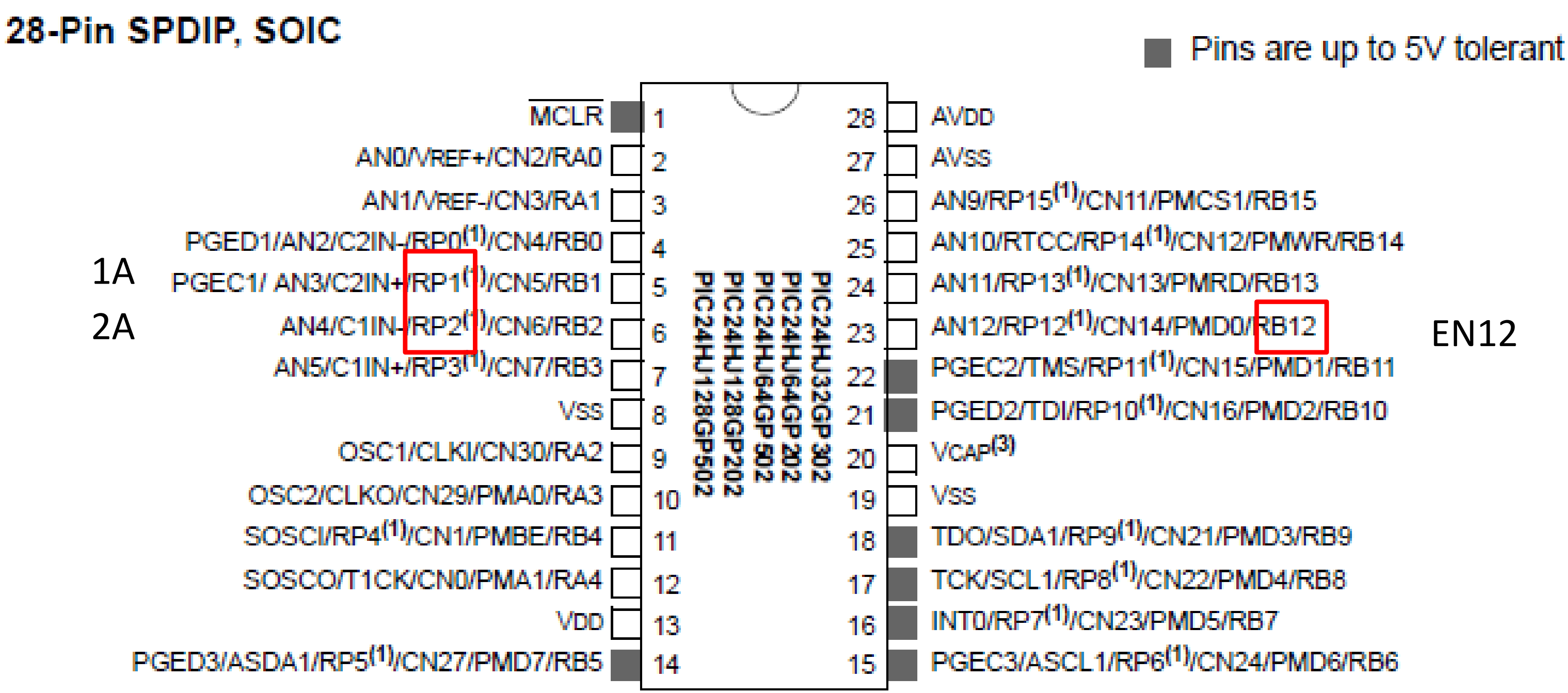
28-Pin SPDIP, SOIC

Pins are up to 5V tolerant



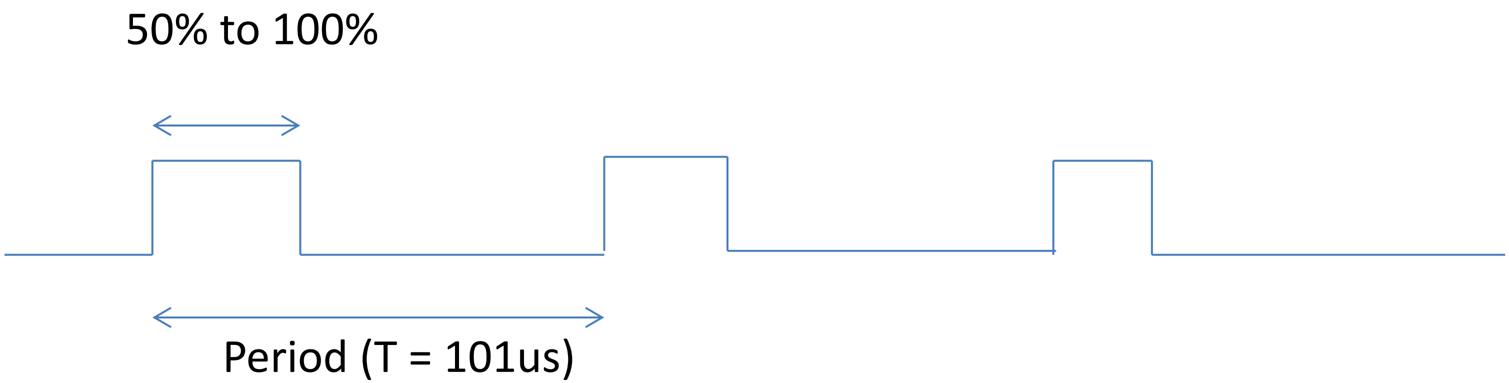
Software

Part B – PWM control using OC1 and OC2, similar to Project 2



Variable "duty cycle"

PWM Signal for DC Motor



Recommended PWM frequency is 9.8KHz for our DC Motor.

Pulse widths should vary between 50% and 100% of the full period.

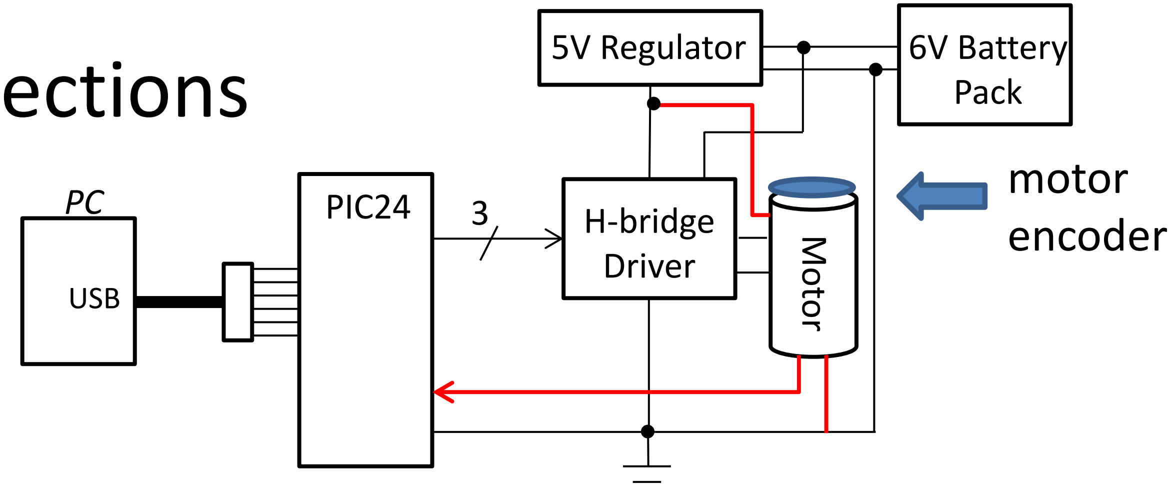
Project 3 Teams

P3_W A	Celina Munoz, Natalia Pezzuco
P3_W B	Amanda Ashmen, Ian Krause
P3_W C	Nils Carlson, Spencer Paradis-Fichtner
P3_W D	Alexander Bruno, Di Wu
P3_W E	Brian Zick

P3_T A	Marlie Norbrun, Ethan Oswald
P3_T B	Yusen Meng, Kyle Meza
P3_T C	Nikolaos Papaioannou, Conor Willsie
P3_T D	Alexis Juarez, Xavier Quinn
P3_T E	Andrew James, Jacob Karaul
P3_T F	Miles Duncan, Dale MacLeod

Part C – Using Motor Encoder

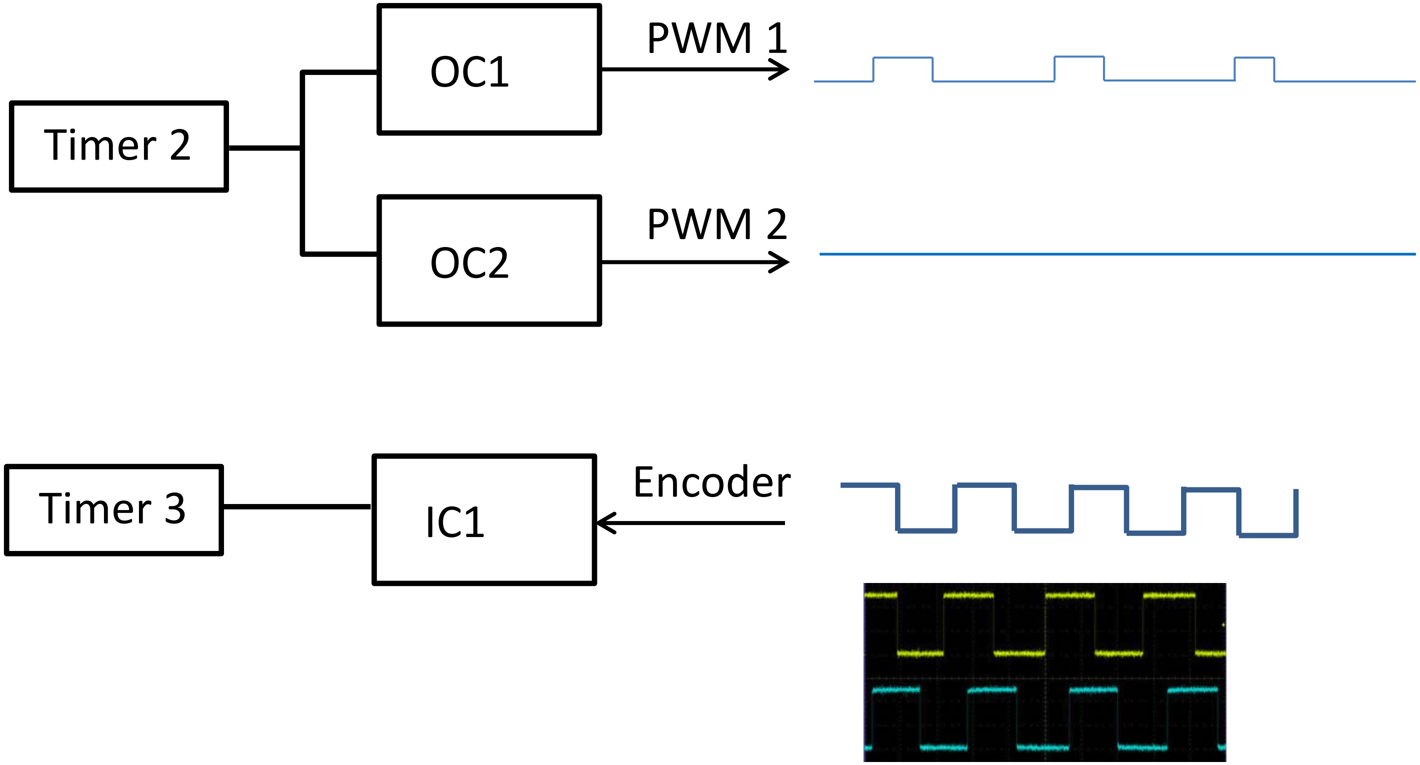
3 new connections



Color	Function
Red	motor power (connects to one motor terminal)
Black	motor power (connects to the other motor terminal)
Green	encoder GND
Blue	encoder Vcc (3.5 – 20 V)
Yellow	encoder A output
White	encoder B output

Output Compare and Input Capture

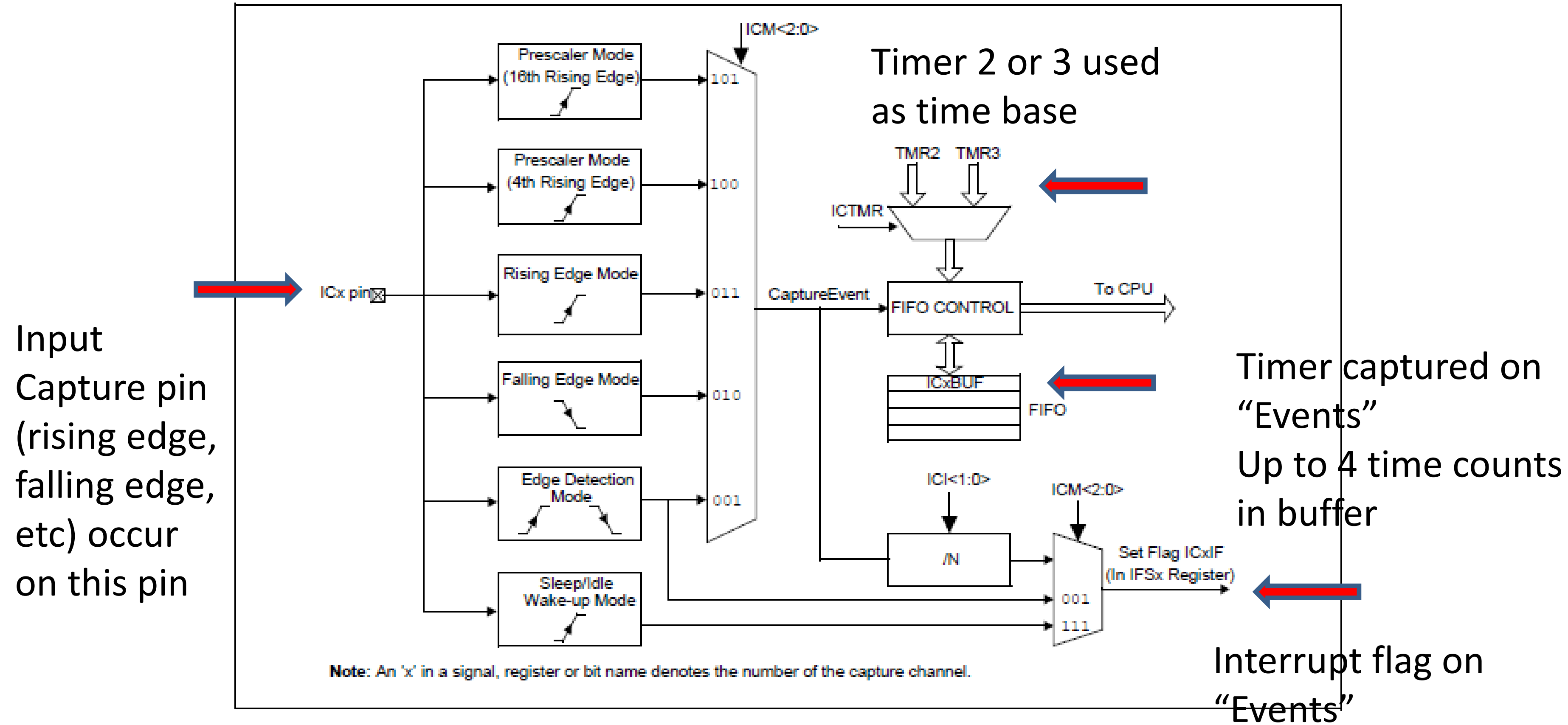
- Output Compare – used to control PWM to motor
- Input Capture – used to capture pulse edges from motor encoder
- Need to have separate timers



Input Capture Module

(Think of a stop watch)

FIGURE 14-1: INPUT CAPTURE BLOCK DIAGRAM



Note: An 'x' in a signal, register or bit name denotes the number of the capture channel.

Each capture channel available on dsPIC33F/PIC24H family devices has these registers:

- ICxCON: Input Capture Control register
- ICxBUF: Input Capture Buffer register (see Table 12-3 for bit information)

Input Capture “Event”

- The Input Capture module captures the 16-bit value of the selected timer (Timer2 or Timer3), when a capture event occurs.
- A capture “event” is defined as a write of a timer value into the capture buffer.
- The capture “mode” determine what causes the “event” (rising edge, falling edge, etc)

Input Capture Modes

- Simple Capture Event modes:
  - Capture timer value on every falling edge of input at ICx pin
  - Capture timer value on every rising edge of input at ICx pin
- Capture timer value on every edge (rising and falling)
- Prescaler Capture Event modes:
  - Capture timer value on every 4th rising edge of input at ICx pin
  - Capture timer value on every 16th rising edge of input at ICx pin

Choose a mode that will provide enough accuracy, but not be more Timer Tcks than the 16-bit IC1BUF register will hold. Depends on the input signal frequency.

ICxCON IC Control Register

Register 12-1: ICxCON: Input Capture x Control Register

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	ICSIDL	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-0, HC	R-0, HC	R/W-0	R/W-0	R/W-0
ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		
bit 7							bit 0

Legend:	HC = Cleared in Hardware		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **ICSIDL:** Input Capture x Stop in Idle Control bit
1 = Input capture halts in CPU Idle mode
0 = Input capture continues to operate in CPU Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **ICTMR:** Input Capture x Timer Select bit
1 = TMR2 contents are captured on capture event
0 = TMR3 contents are captured on capture event

bit 6-5 **ICI<1:0>:** Select Number of Captures per Interrupt bits
11 = Interrupt on every fourth capture event
10 = Interrupt on every third capture event
01 = Interrupt on every second capture event
00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture x Overflow Status Flag bit (read-only)
1 = Input capture overflow occurred
0 = No input capture overflow occurred

bit 3 **ICBNE:** Input Capture x Buffer Empty Status Flag bit (read-only)
1 = Input capture buffer is not empty, at least one more capture value can be read
0 = Input capture buffer is empty

bit 2-0 **ICM<2:0>:** Input Capture x Mode Select bits
111 = Input capture functions as interrupt pin only when device is in Sleep or Idle mode detect only, all other control bits are not applicable)
110 = Unused (Input Capture module disabled)
101 = Capture mode, every 16th rising edge
100 = Capture mode, every 4th rising edge
011 = Capture mode, every rising edge
010 = Capture mode, every falling edge
001 = Capture mode, every edge – rising and falling (ICI<1:0> bits do not control interrup for this mode)
000 = Input Capture module turned off

References for Exercise 7

All Available on Nexus

- Motor driver chip
- 5V regulator
- DC motor specifications

– P24HJ128GP502 Datasheet

- Section 14 describes Input Capture

– Input Capture Datasheet