

Brian Connor Liau

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Education

Tufts University, School of Engineering

Bachelor of Science in Electrical Engineering, Minor in Embedded Systems

Medford, MA

Cumulative GPA: 3.92/4.0

Sept. 2023 – May 2027

Relevant Coursework: Digital Signal Processing, Feedback Control Systems, Digital IC Design

Dean's List: Spring 2025, Fall 2024, Spring 2024, Fall 2023

Work Experience

Silicon XPandas

Electrical Engineering Intern

Taipei, Taiwan

May 2025 – Aug. 2025

- Developed a graphical shell script runner that enhanced IC testing efficiency by 40%
- Designed, debugged, and implemented a C program to validate the I3C interface of ICs
- Engineered a motor control system for 3D photogrammetry using a stepper motor

Dept. of Electrical and Computer Engineering, Tufts

Teaching Assistant for Digital Logic

Medford, MA

Sept. 2025 – Present

- Lead weekly lab sessions consisting of 80+ students, assisting SystemVerilog debugging in Lattice Radiant
- Graded assignments, providing 1-on-1 support on combinational/sequential logic, FSMs, and timing

Projects and Student Organizations

Axis Guitar Project from the IDEA Lab

Embedded Hardware Engineer

Medford, MA

Sept. 2025 – Present

- Collaborate with six peers to develop systems that control sensors and audio signal communication
- Integrate microcontroller-based systems to process user inputs, manage real-time data, and support dynamic sound modulation
- Troubleshoot and debug embedded hardware and software, improving the responsive rate by 35%

Tufts Solar Vehicle Project

High Voltage Team Member

Medford, MA

Sept. 2024 – Present

- Assemble high voltage startup system and optimize motor/auxiliary power systems
- Utilize spot welding and 3D printing to fabricate a battery holder and assemble the high-voltage system

Line Following Robot

Robotics Engineer

Medford, MA

Sept. 2025 – Present

- Design and program motor control algorithms that enable precise movement
- Partner with a team of three engineers to create and implement robot movement states using a finite state machine (FSM) framework
- Optimize collision detection algorithms using infrared sensors, increasing reactivity by 15%

VHDL-Based Mini Golf Game on an FPGA

Lead Hardware Engineer

Medford, MA

Nov. 2024 – Dec. 2024

- Led the development of the VGA component, enabling 2D graphics display on an external monitor
- Implemented 2D graphics rendering focusing on reducing resource use by 15% by utilizing an overlay system

Professional Skills and Languages

Skills: SystemVerilog, VHDL, C++, C, Digital/Analog Circuit Design, MATLAB, Test Engineering

Tools/Software: Lattice Radiant, LTspice, Altium, Oscilloscopes, Multimeters, and Jira

Languages: English (Fluent), Mandarin (Advanced)