Wave Analysis using FPGAs on Marine Buoys

by

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This Report is submitted in partial fulfilment of the requirements of the Honours Degree in Computer and Communications Engineering (DT081) of the Dublin Institute of Technology

February 3, 2017

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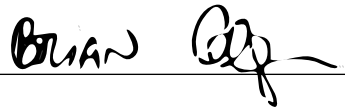
Company Supervisor: Mr. Paul Drum

Declaration

I, the undersigned, declare that this report is entirely my own written work, except where otherwise accredited, and that it has not been submitted for a degree or other award to any other university or institution.

Signed:



Date:

February 3, 2017

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Chapter 1

Introduction

1.1 Objectives

The key objectives of this project are to create a hardware design that can mathematically process wave data and wirelessly transmit this data using a Field Programmable Gate Array (FPGA). The Nexys4 DDR board will be used throughout the project. It is a complete, ready-to-use digital circuit development platform based on the latest Artix-7™ FPGA from Xilinx®.[1] The project will be completed over a 16-week period in collaboration with CréVinn Teoranta with the intention to demonstrate skills in hardware design and mathematical methods.

The FPGA must read in acceleration measurements using the on-board three axes accelerometer. This information will then be used to calculate velocity. Over a set amount of time, displacement data can be saved to a memory block in Random Access Memory (RAM). This data can then be mathematically processed to determine wave height, period and energy. The main challenge in this project is to design a Fast Fourier Transform (FFT) in the Hardware Design Language (HDL), SystemVerilog. The FFT is essential in calculating wave energy. Other algorithms to calculate wave height and period will be required, the approach to calculating this displacement data will be outlined in the Research chapter. Like the FFT, these will be implemented using HDL as opposed to implementing a soft-processor on the FPGA.

The height, period, energy from the above calculations must then be formed into a packet to be wirelessly transmitted. An on-board temperature sensor is also used to measure temperature of the water which will be appended to the final data packet in degrees Celsius. The received transmission will be a human-readable message which will outline sea state, weather conditions and water temperature based on the measured data to the end-user.

An overview of this system can be seen in Figure 1.1 below:

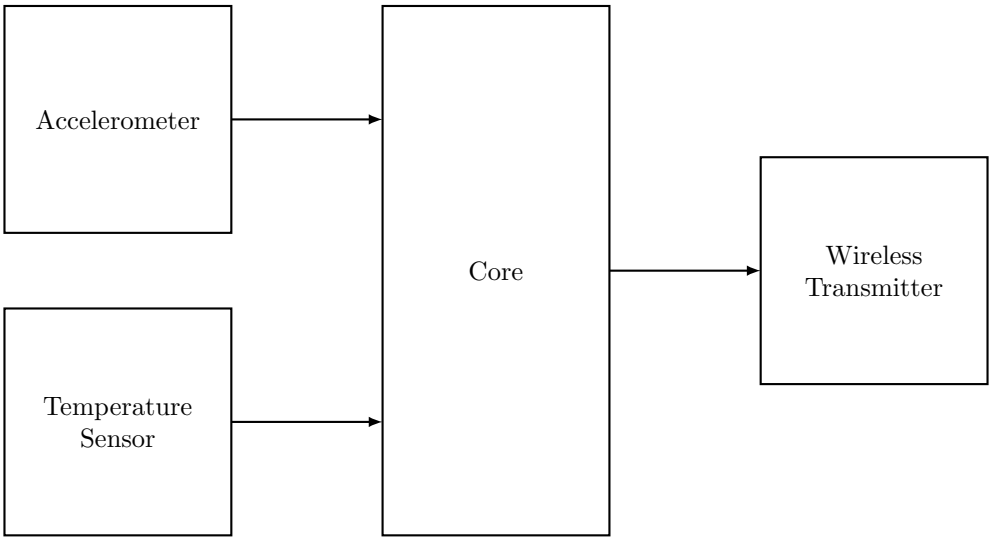

Figure 1.1: System Overview

For this design, the Core is the Intellectual Property (IP) block. The accelerometer and temperature sensor are inputs to the system and calculations will be output to the wireless transmitter.

Chapter 2

Research

2.1 Design

A Top-Level Block Diagram can be seen in Figure 2.1 below.

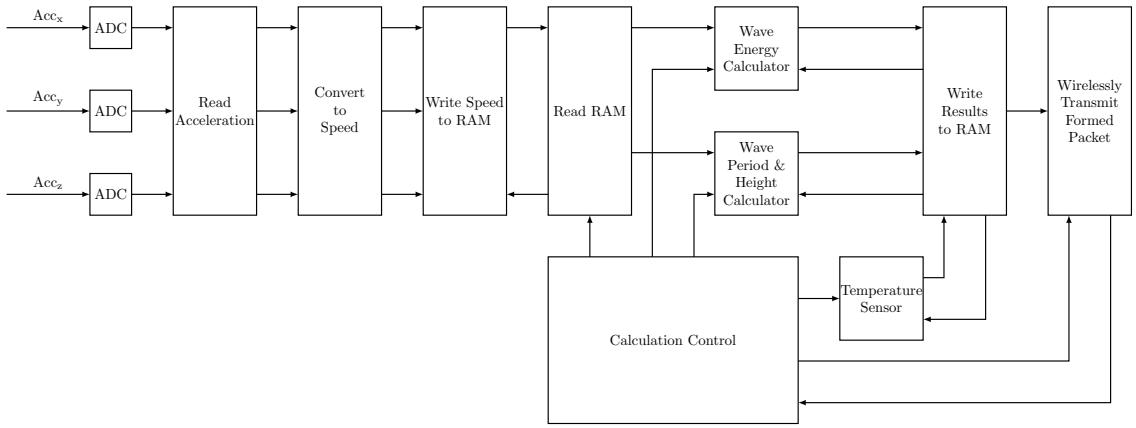

Figure 2.1: Top Level Block Diagram

ADC:
Analogue-to-digital converter to be used with accelerometer measurements as an input.

Read Acceleration:
Read in acceleration in all 3-axes

Convert to Speed:
Calculate speed from acceleration. ($v = u + at$)

Write Speed to RAM:
Store speed values in memory block until a sizeable array is built over time.

Read RAM:
When array is full, read values to be used for calculation.

Wave Energy Calculator:
Read in x, y and z measurements over time to calculate Wave Energy, this can be done with an FFT.

Wave Period & Height Calculator:
Read in x, y and z measurements to calculate displacement. ($s = ut + \frac{1}{2}at^2$) Only z-axis is required for Wave Height. Period can also be calculated with an FFT.

Temperature Sensor:
Read in water temperature to be transmitted.

Calculation Control:
Initiates calculation modules when value array is full.

Write Speed to RAM:
Energy, Height, Period and Temperature stored to a memory block.

Wireless Transmit Formed Packet:
Build data block in packet and transmit wirelessly.

2.2 Data Processing

To process the data the design will perform an FFT by implementing the Cooley-Turkey algorithm, this is the most common form of FFT. It is a recursive algorithm which breaks the Discrete Fourier Transform (DFT) into smaller DFTs. This design will divide the DFT of size $n = 2m$ into two interleaved DFTs of size m, this is known as radix-2.

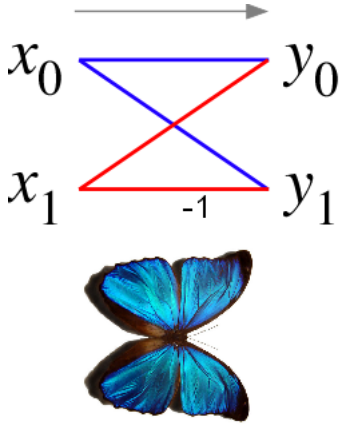

Figure 2.2: Butterfly Diagram[2]

These smaller DFTs are then combined via size-2 DFTs (known as butterflies in this context, due to the shape of the data flow) pre-multiplied by roots of unity (which are known as twiddle factors). The butterfly operation takes the form:

$$y_0 = x_0 + x_1 * tw$$

$$y_1 = x_0 - x_1 * tw$$

The above form is known as Decimation In Time (DIT). However, one can have a process where the butterflies come first and are post-multiplied by the twiddle factors, which is known as Decimation In Frequency (DIF).

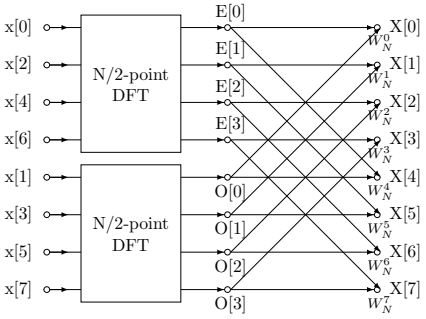

Figure 2.3: Data flow diagram for N=8: a decimation-in-time radix-2 FFT[3]

2.3 Wireless Transmission

To transmit the data wirelessly the design requires a specific wireless technology. Data will be sent via a Short Message Service (SMS). The design will have a Xilinx MicroBlaze soft-processor with a Universal Asynchronous Receiver/Transmitter (UART) port which will be used to send relevant Attention (AT) commands (from the Hayes command set) and drive the Global System for Mobile Communications (GSM) module. This design can be used in many applications.[4, 5] A block diagram of the design can be seen in Figure 2.4.

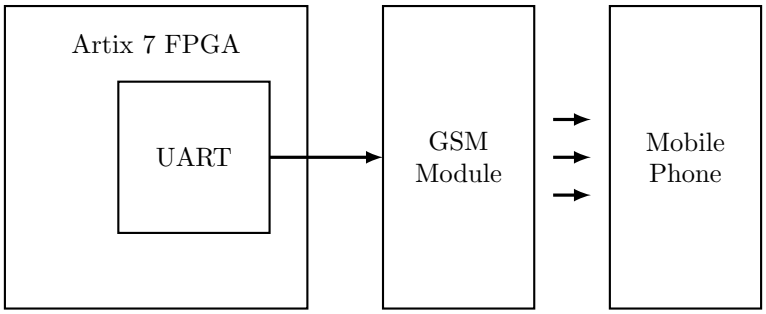

Figure 2.4: Wireless embedded system built around Artix 7 FPGA

Data will be transmitted using the RS-232 standard for serial communication. This interface can be seen in Figure 2.5.

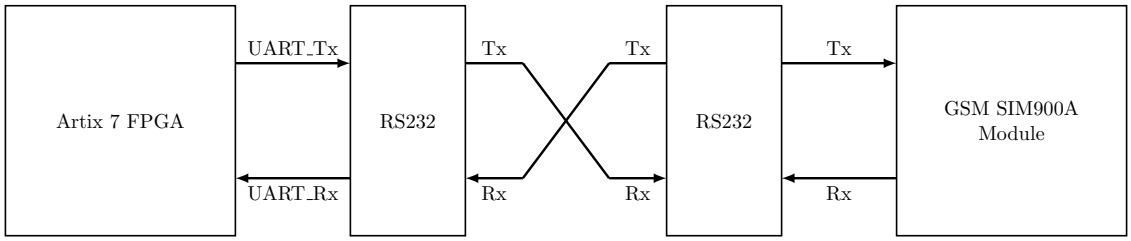

Figure 2.5: Interfacing UART and GSM SIM900A Module

2.4 Testing

The testing of the FFT will be done by entering a sinusoid as stimulus to the design. The output of this system will be measured against expected results. These test-cases will be done with a SystemVerilog test-bench. Wave data will also be obtained to measure against pre-determined results.

Initially the GSM module will be tested by sending an SMS to a personal mobile phone. Once this functionality is achieved, a new Subscriber Identity Module (SIM) card will be put into the GSM module. This allows texts to be sent to third-party services, e.g. Twitter.

Chapter 3

Ethics

The information obtained in this project is particularly useful for two groups within society; marine users and wave power researchers. As such, the ethical requirements of this project can be divided into two parts;

- Relations with colleagues, clients, employers and society in general
- Environmental and social obligations

both of which are set out by Engineers Ireland in its Code of Ethics.[6]

With regards to societal relations, the intention of the project is to provide safety information to marine users. In this context, the project is a demonstration of skill/expertise being applied to the common good as well as advancing human welfare with proper regard for the health and welfare of the public. It is important to note that this project is designed to be non-hazardous and have zero military applications so as to not result in a serious detriment to any person or persons.

Environmental and social obligations are also a primary motive for this project. As outlined above wave power researchers would, understandably, have significant interest in wave energy estimations. The design of this project is intended to promote the principles and practises of sustainable development and the needs of the present and future generations. The project shall also foster environmental awareness within the profession of engineering among the public.

The reason an Artix®-7 FPGA was selected was due to it being the highest performance-per-watt fabric offered by Xilinx.[7] This allows the design to accomplish the objectives outlined in the Introduction with the most efficient consumption of natural resources which is practicable economically. This includes the maximum reduction in energy usage, waste and pollution.

As FPGAs already have low power consumption (in comparison to microprocessors) it would also be possible to power the design itself with a renewable energy source e.g. solar energy. Execution of the project in this way eliminates any adverse impact on the natural environment.

Chapter 4

Work Plan

Time management is vital within a project, as such the project is broken down into phases and then again into tasks. Each task is allotted a predicted amount of time and this allows schedules and deadlines to be made. Each phase and its corresponding tasks are input to a Microsoft Project file. This predicted timeline is displayed as a Gantt chart which allows for accurate tracking of tasks and resources.

4.1 Resources

Resources for this project were provided by the company sponsoring the project, CréVinn Teoranta, these include materials such as the FPGA as well as a computer to work on throughout the project.

4.2 Milestones

Milestones are the major goals within a project, these are outlined below;

- Design specification
- Register-Transfer Level (RTL) Design
- RTL Verification
- Design on FPGA
- GSM Integration

4.3 Plan

The Gantt chart for the project can be seen in Figure 4.1.

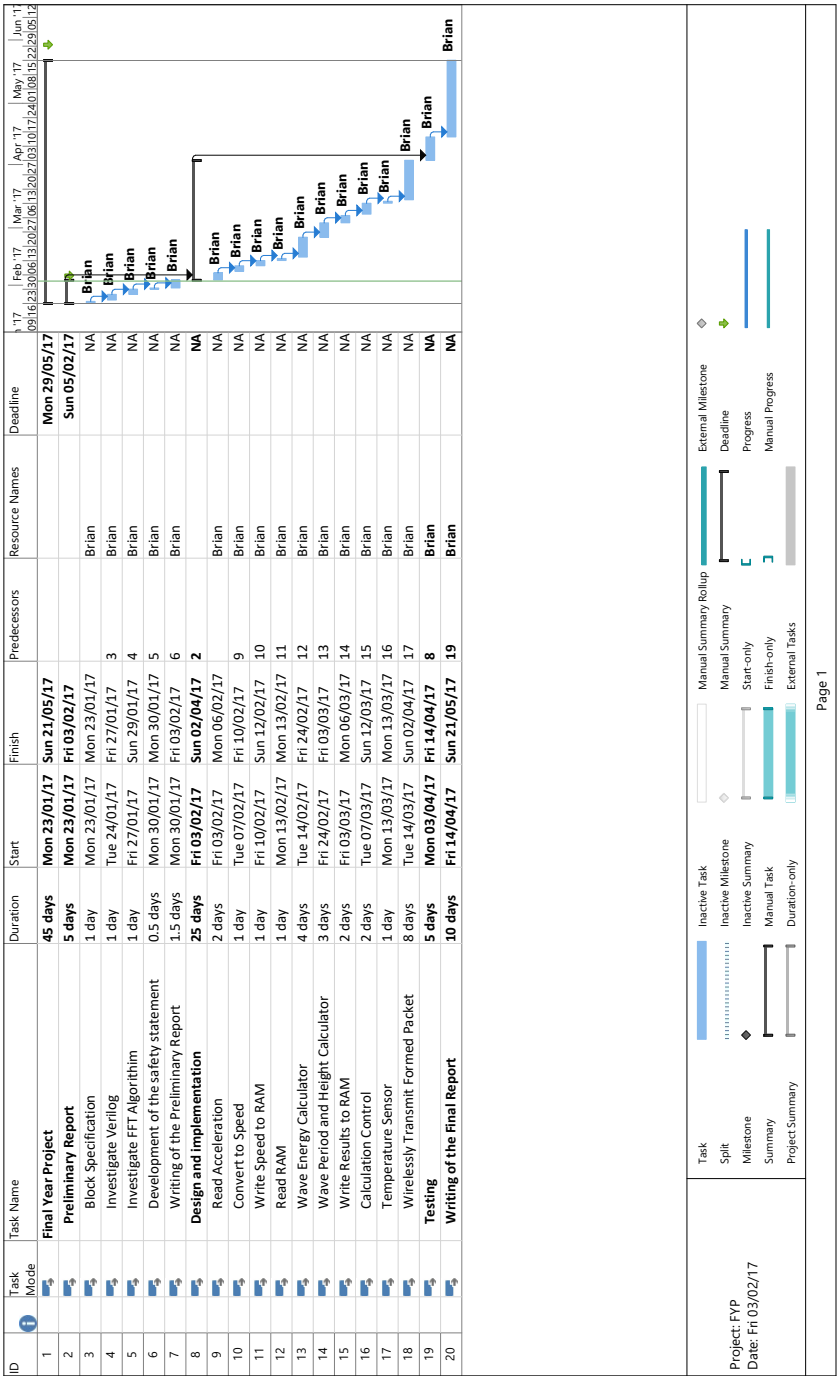

Figure 4.1: Gantt Chart

References

[1] Digilent. Nexys4 DDR™ FPGA Board Reference Manual. [Accessed 03 02 2017]. [Online]. Available: https://reference.digilentinc.com/_media/nexys4-ddr:nexys4ddr_rm.pdf

[2] S. G. Johnson. File:Butterfly-FFT.png. [Accessed 03 02 2017]. [Online]. Available: https://commons.wikimedia.org/wiki/File:Butterfly-FFT.png

[3] Virens. File:DIT-FFT-butterfly.png. [Accessed 03 02 2017]. [Online]. Available: https://commons.wikimedia.org/wiki/File:DIT-FFT-butterfly.png

[4] P. K. Gaikwad, "DEVELOPMENT OF FPGA MICROBLAZE PROCESSOR AND GSM BASED HEART RATE MONITORING SYSTEM," *International Journal of Computer Science and Mobile Applications*, vol. 1, pp. 24–29, 2013.

[5] N. Joshi, "Development of FPGA MicroBlaze Processor and GSM based Wireless Monitoring System for Neonatal Intensive Care Unit," *International Journal of Research in Engineering & Advanced Technology*, vol. 4, 2016.

[6] Engineers Ireland. Code of Ethics. [Accessed 03 02 2017]. [Online]. Available: http://www.engineersireland.ie/EngineersIreland/media/SiteMedia/about/Engineers-Ireland-Code-Of-Ethics-2010.pdf

[7] Xilinx. Artix-7 FPGA Family. [Accessed 03 02 2017]. [Online]. Available: https://www.xilinx.com/products/silicon-devices/fpga/artix-7.html

Appendix A

Project Risk Assessment Form

Project Risk Assessment Form

SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

Student(s) Name	Brian Colgan
Student(s) Number	C12380846
Programme Code and Year	DT081/4
Start Date of Project	23 January 2017
Supervisor Name	Dr. Andreas Schwarzbacher

Implement Wave Analyser using Nexys 4 DDR Field Programmable Gate Array (Artix-7). Project is sponsored by CréVinn Teoranta and will mostly be carried out in their Ballymount office. Hardware Design Language (HDL) will be written from a laptop/desktop.

Project Risk Assessment

Prior to starting, the Project Supervisor and Student(s) must identify the hazards which may be present and state what control measures they will be put in place to control the Risk. Below is a ***non exhaustive list*** *of the potential Hazards which* ***may be*** *present, these can be used as a starting point. Ensure you identify the controls needed. These can include using a less dangerous chemical, training on use of equipment, good lab or workshops practices, reporting defects, first aider present, following the out of hours access and off campus activities procedures and other procedures, use of PPE etc.*

Potential Hazards	Present (Yes/No)	Details	Controls Required
Work Equipment and Environment	Yes	FPGA Board	Adhere to all relevant company policies
Electrical Shock Hazard	No	N/A	N/A
Hand tools / Power Tools	No	N/A	N/A
Slips, trips and falls	No	N/A	N/A
Manual Handing	No	N/A	N/A
Soldering	No	N/A	N/A
Compressed Air	No	N/A	N/A
Rotating Machinery	No	N/A	N/A
Noise	No	N/A	N/A
Computer Usage	Yes	Design work done from desktop/laptop	Take breaks at regular intervals to rest eyes and avoid being sedentary

1

Lone Working	Yes	Work can be done at home or in the office without supervision	Ensure contact is maintained with colleagues and academic supervisor
Sudden Illness and/or Medical Emergencies	No	N/A	N/A
Fire/Emergency Evacuation	No	N/A	N/A
Biological Agents	No	N/A	N/A
Chemical	No	N/A	N/A
Gases	No	N/A	N/A
Heat Sources/High Temperatures/Hot Surfaces	No	N/A	N/A
Lasers	No	N/A	N/A
Vibrations	No	N/A	N/A
Working off Campus	Yes	Will be working mostly in Ballymount office	Maintain contact with academic supervisor
What other Hazards could be present and what effect will they have on the student(s), fellow students or employees? Use separate sheet if required.	N/A	N/A	N/A

Category of Supervision Required		
Category	**Level of Risk Present**	**Tick one**
Category A	The risks associated with the work and/or the inexperience of the student(s) are such that the work must be supervised **directly** by a competent person (the supervisor or his/her authorized nominee), at least until the supervisor is satisfied that the student(s) can follow correctly the appropriate scheme of work. **Note**: this might apply only to a small section of the whole project.	☐
Category B	The risks associated with the work and/or the inexperience of the student(s) is such that the work may not be started without the supervisor's or his/her authorized nominee's advice and approval.	☐
Category C	The Risks are such that the work requires considerable care but it is considered that the student(s) is adequately trained and competent in the procedures involved.	☐
Category D	The risks are low and carry no special supervision requirements.	☑

Risk Assessment Sign Off			
Student(s) Sign and Date		**Supervisor Sign and Date**	

THE SIGNED FORM SHOULD BE SUBMITTED TO _____. THE PROJECT SUPERVISOR AND THE STUDENT(S) SHOULD RETAIN A COPY OF SAME.