Intel® Technology to Power the 5G Network: An Architecture Deep Dive

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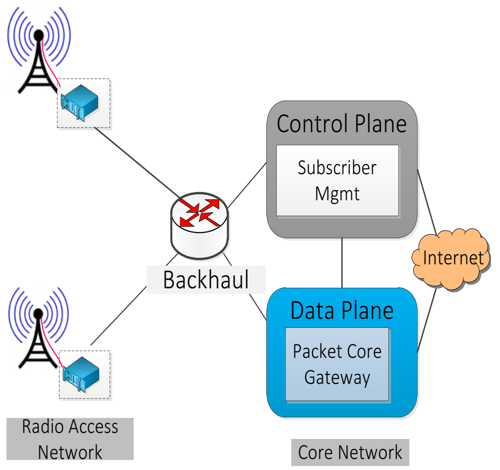
INTEL DEVELOPER FORUM

Agenda

- Background
  - Today's Network & evolving trends
- Network 2020 & beyond
  - 5G characteristics, Use cases
  - Intel investments in Network
- Key Technologies driving 5G
  - FlexRAN/FlexCORE
  - 5G RAT
  - Network Slicing
  - Massive MIMO
- Summary

Today's Cellular Network & evolving trends



Trends

Cloud-RAN, Virtual-RAN, Split RANs, Virtual Core

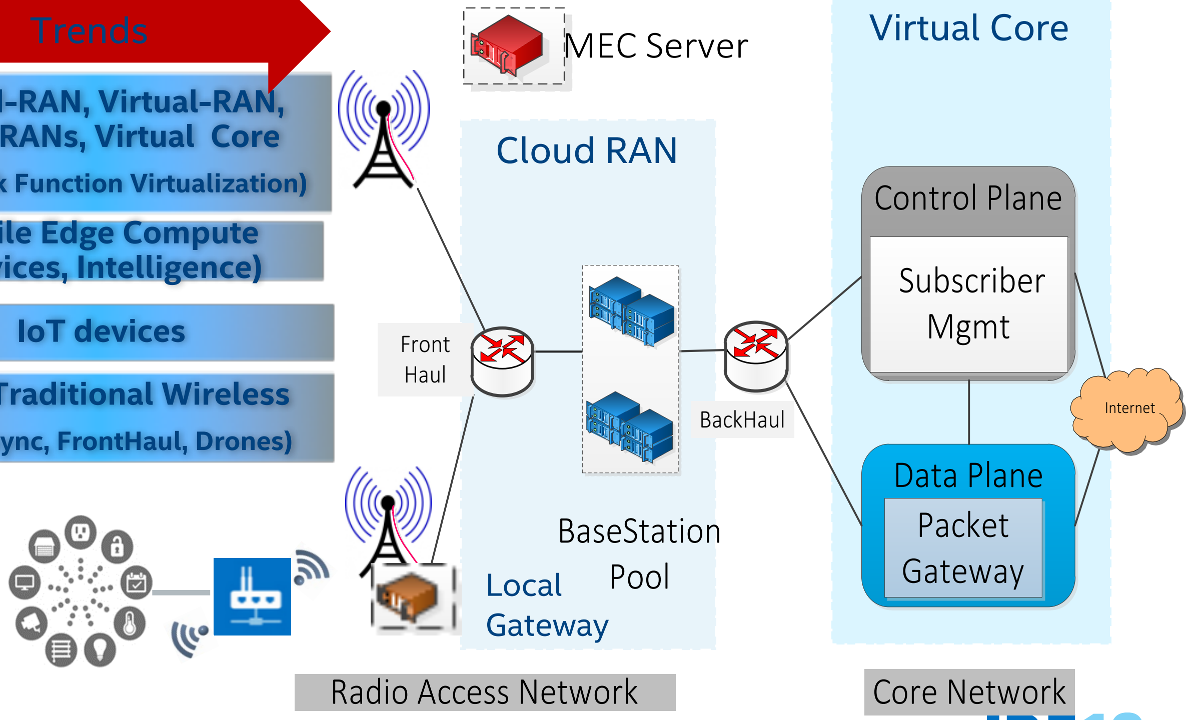
(Network Function Virtualization)

Mobile Edge Compute (Services, Intelligence)

IoT devices

Non-Traditional Wireless

(e.g. Async, FrontHaul, Drones)



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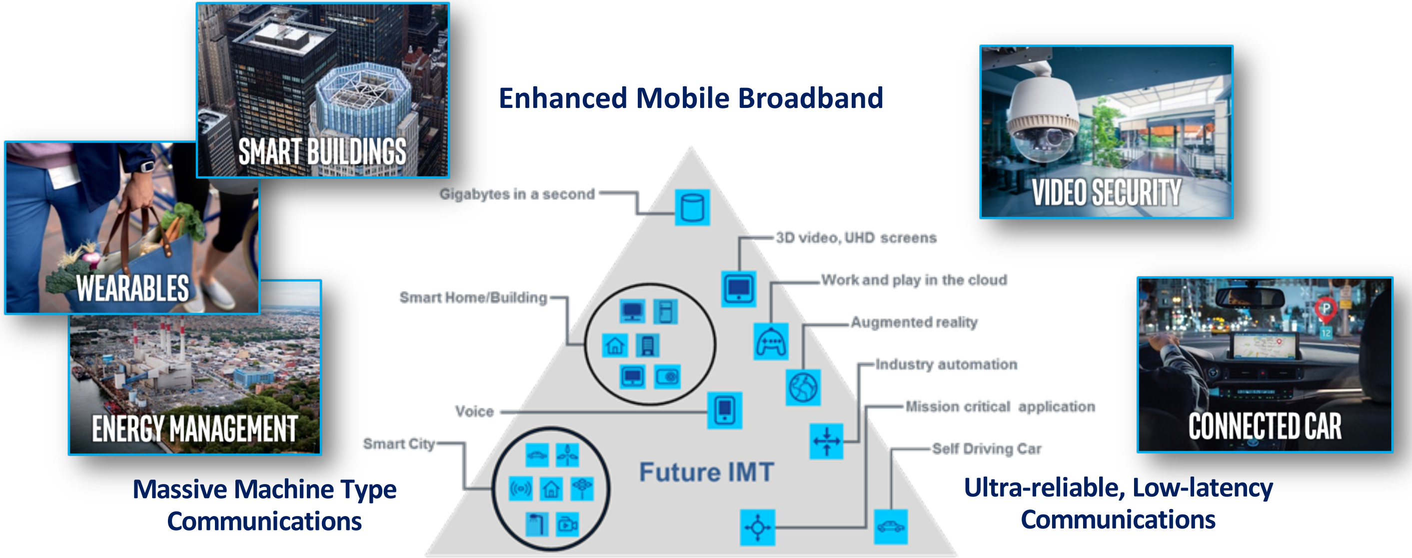
5G - Quick Recap

ITU-R Usage Scenarios for 5G



Source: Recommendation ITU-R M.2083 “IMT Vision - Framework and overall objectives of the future development of IMT for 2020 and beyond”

Intel products fuel the 5G engine by enabling
new applications in a variety of spectrum bands

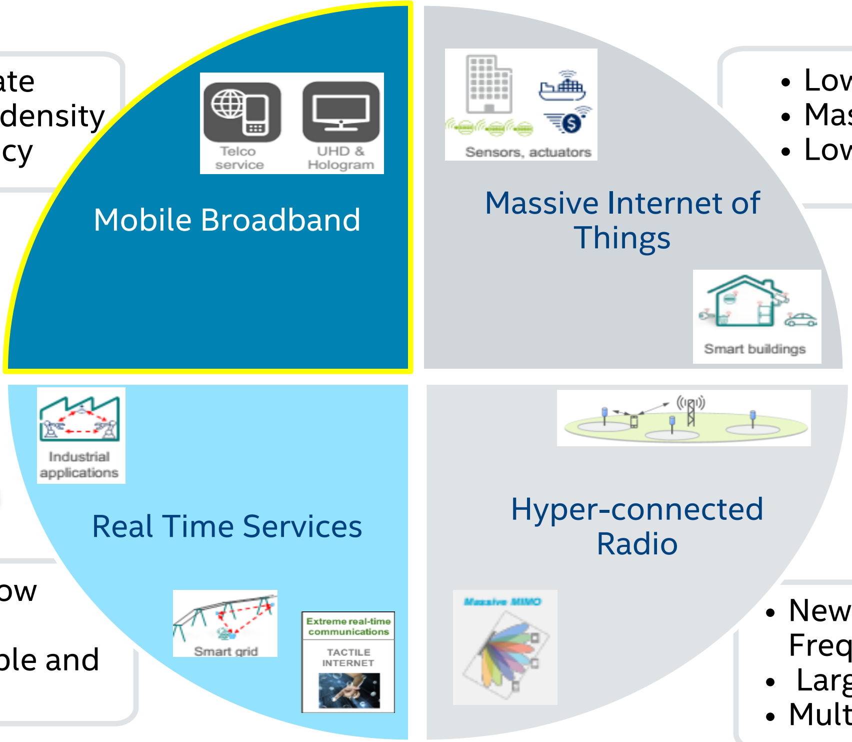
5G: Accelerates dynamically integration of compute and communications

- High data rate
- High traffic density
- Lower latency

4G is addressing mobile broadband but 5G takes it another level

Tactile Internet
Remote Health care
Industrial applications
Real time gaming

- Extreme Low Latency
- Ultra reliable and available



- Low Data
- Massive #devices
- Low Power

Smart Building, Sensors, Actuators based decision making

Anywhere Anytime
Virtual/Augmented reality
Network Densification

- New Ultra wide band Frequency Spectrum
- Large # antennas data
- Multi-RAT

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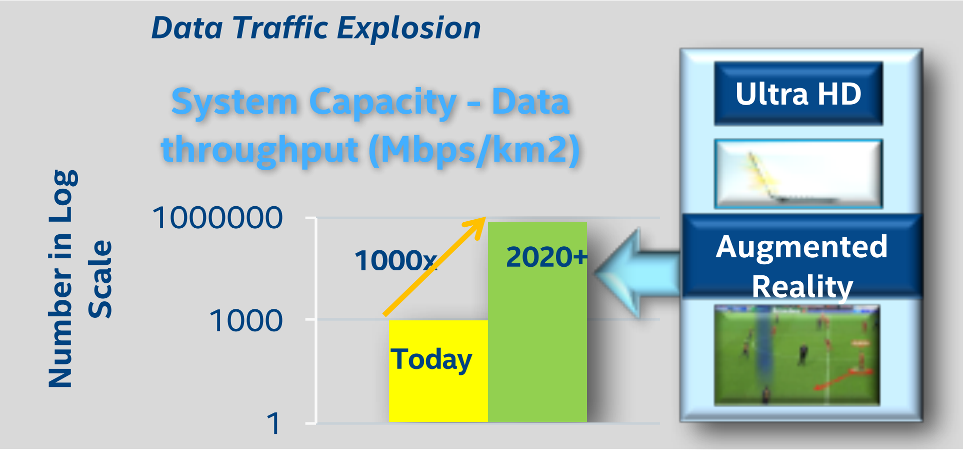
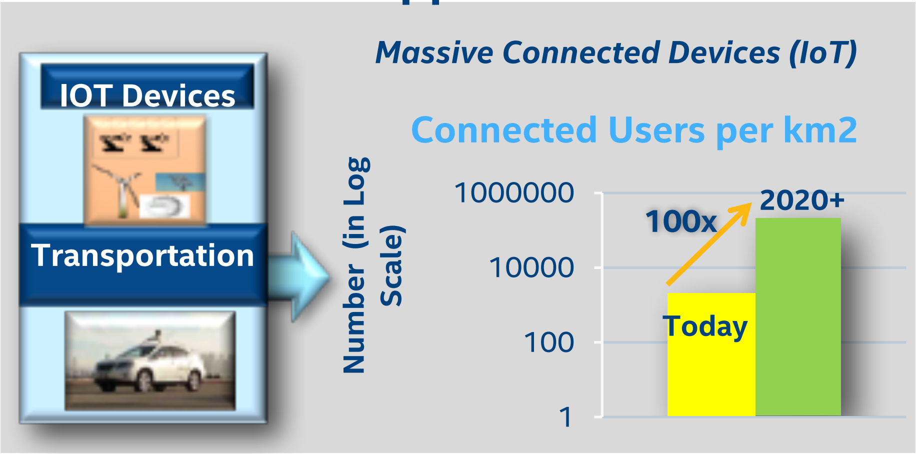
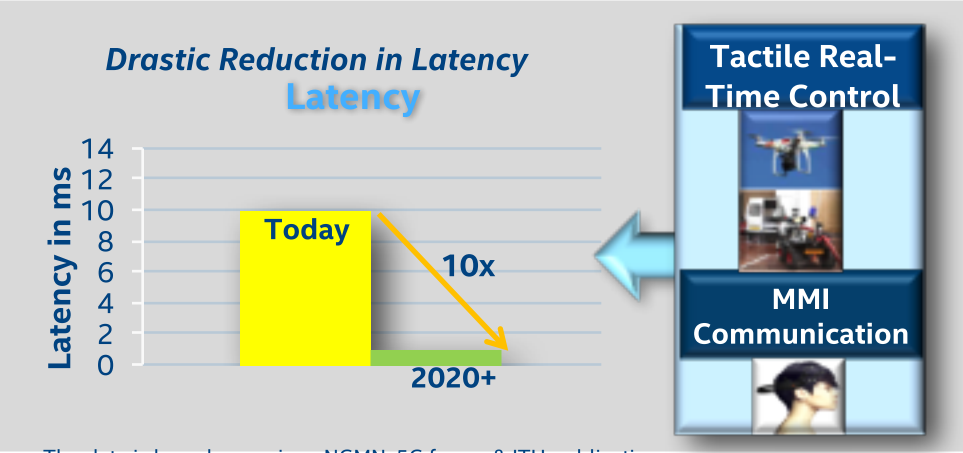
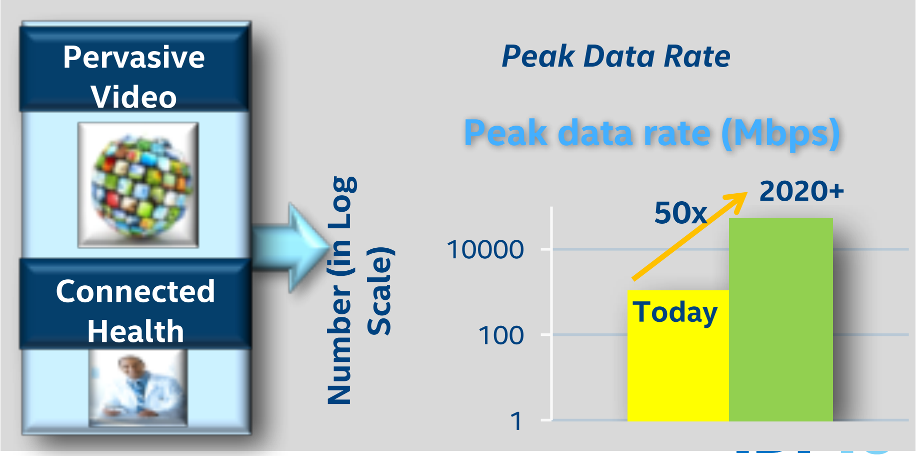
5G Network : New & diverse use cases→ New revenue opportunities



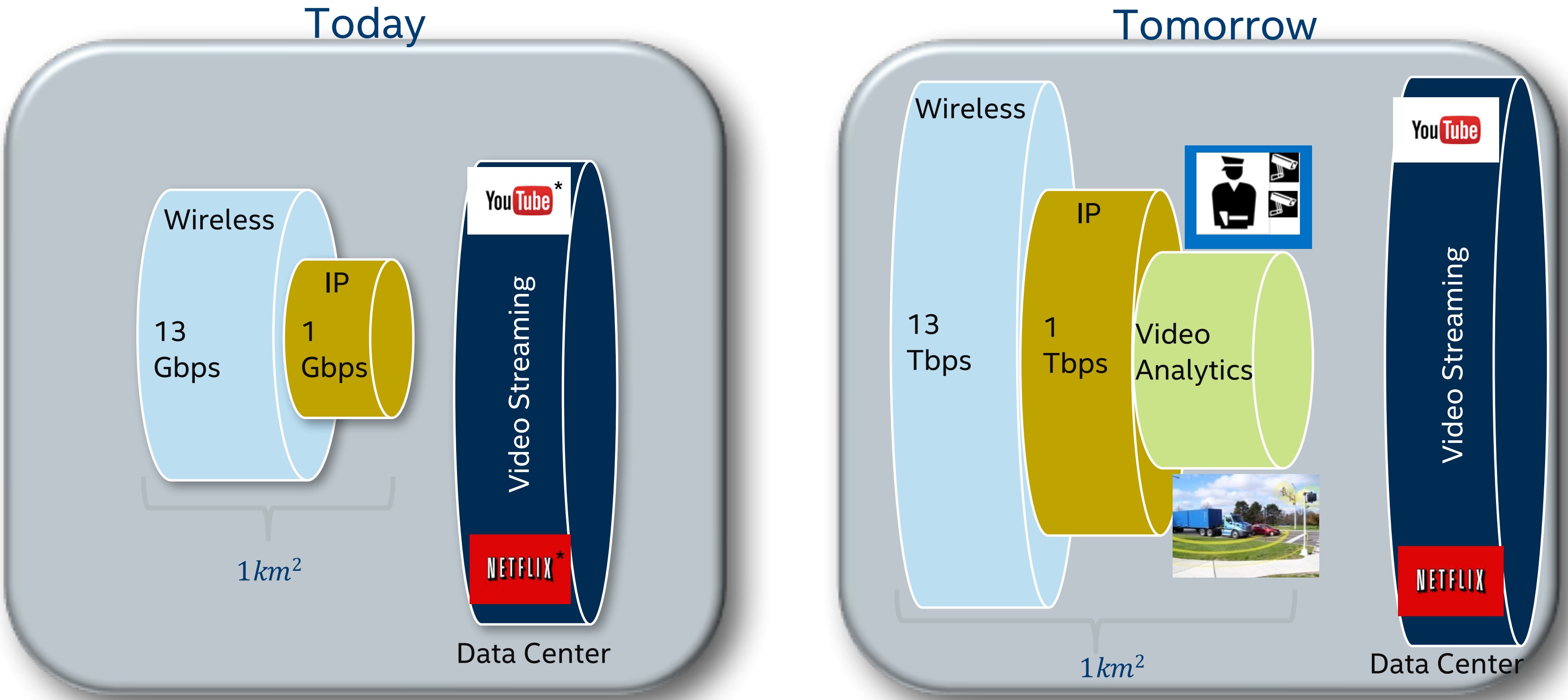






The data is based on various NGMN, 5G forum & ITU publications
https://www.itu.int/dms_pub/itu-r/oth/0a/06/R0A0600005F0001PDFE.pdf
https://www.ngmn.org/uploads/media/NGMN_5G_White_Paper_V1_0.pdf

Network of Tomorrow: Example Smart City



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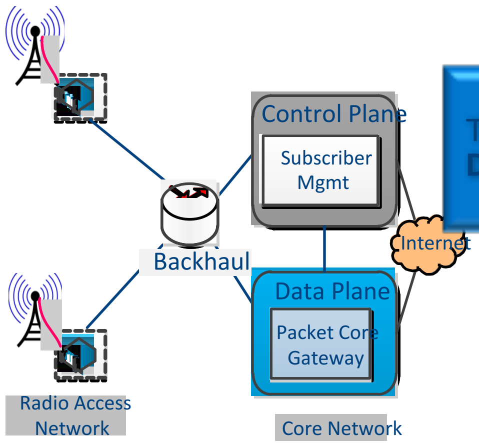
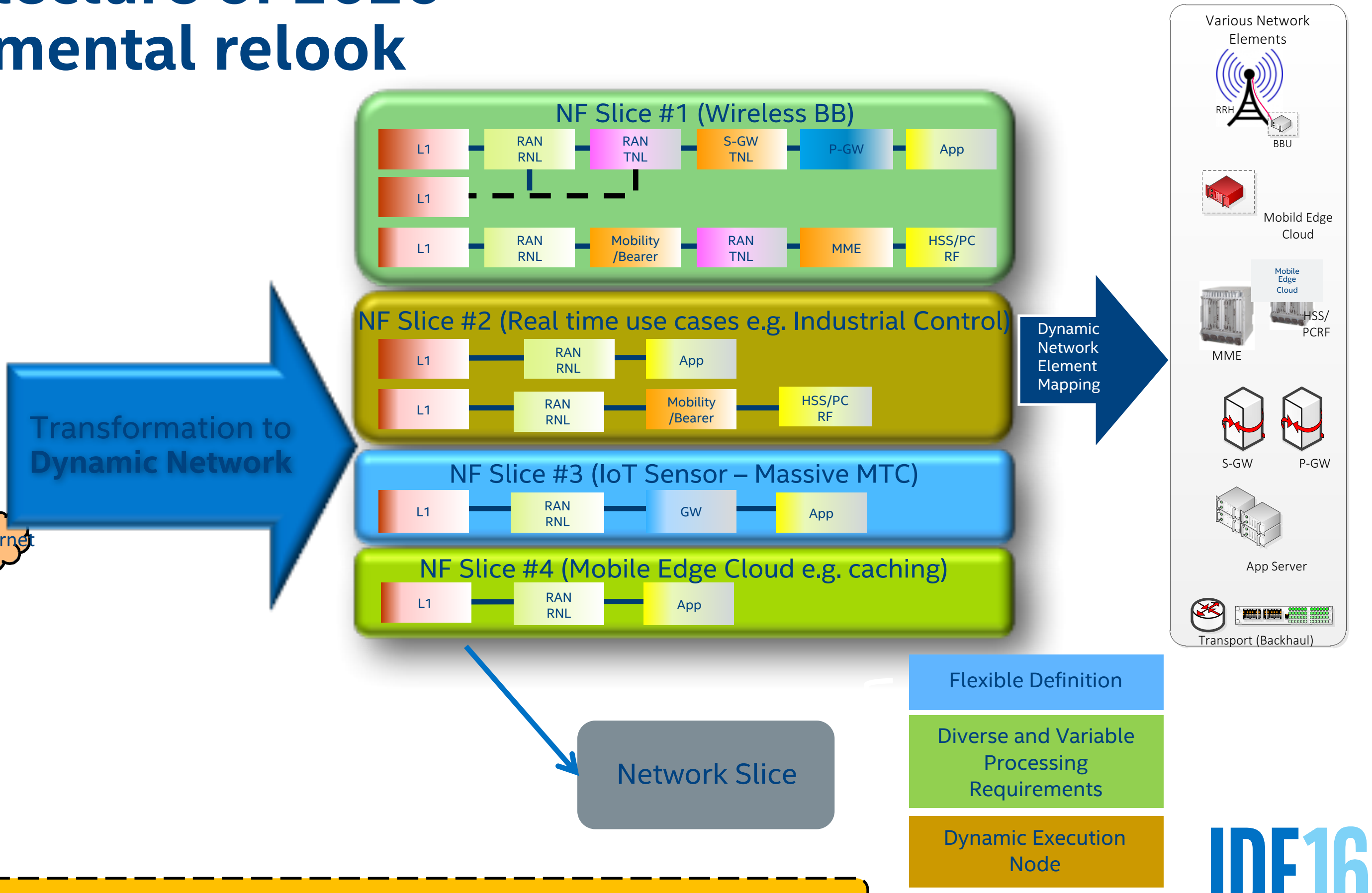
Network Architecture of 2020 Needs a fundamental relook

4G Architecture

- Dedicated, Static HW
- Simple Policy/Profile
- Vertical Silos





Diverse Use cases; Diverse network characteristics

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5G Network Infrastructure : Intel investments

Si Architecture for RAN & Core

- SoC roadmap targeted for network
- Micro architecture Extensions for wireless
- Hardware Queue Manager and QoS
- FPGA – discrete & integrated
- Si Ph & 3D Xpoint* memory

Wireless IP Integration

- Wireless IP
  FEC Encode/Decode
- Packet Acceleration IPs
  - Crypto, ciphers
- High throughput Ethernet IO
- Ethernet Switching

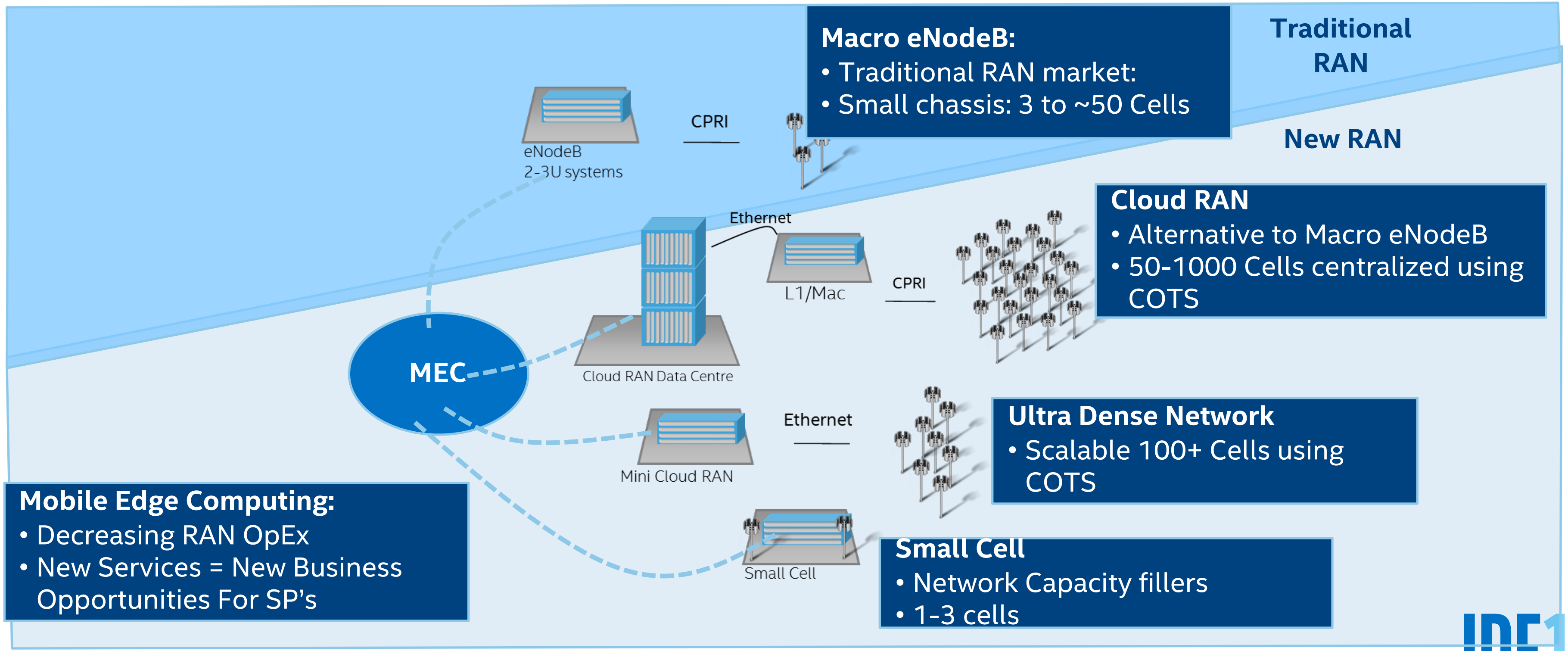
Software

- Industry Effort for Software Defined RAN
- Separation of Control & Data plane for RAN & Core
- Programmable user plane in RAN & Core
- Industry effort on Open Platform/interfaces

Proof Points & Trials

- FlexRAN: Ultra Dense RAN Platform with integrated MEC application with US operator
- FlexCORE: Distributed core network
- Joint showcase of Massive MIMO & Anchor Booster with SK Telecom. Trial in China (MIIT's IMT-2020)
- CPRI o/ Ethernet PoC with an operator

Intel® Architecture = Flexible Network Deployments



Macro eNodeB:
- Traditional RAN market:
- Small chassis: 3 to ~50 Cells

Cloud RAN
- Alternative to Macro eNodeB
- 50-1000 Cells centralized using COTS

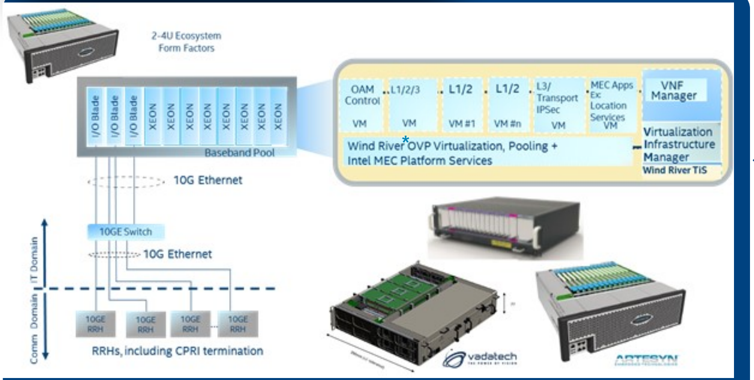
Ultra Dense Network
- Scalable 100+ Cells using COTS

Small Cell
- Network Capacity fillers
- 1-3 cells

Mobile Edge Computing:
- Decreasing RAN OpEx
- New Services = New Business Opportunities For SP's

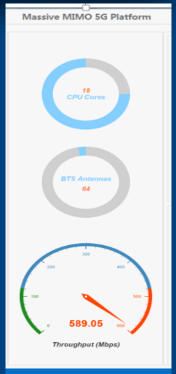
Demonstrated Technology Proof Points

FlexRAN, vRAN & MEC



Field Trial for outdoor traffic profile

Massive MIMO @ <6GHz

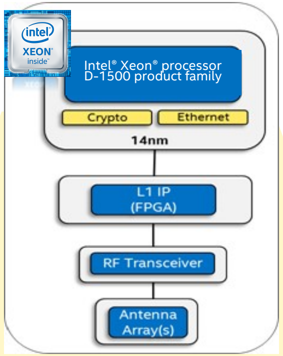


8 Streams @ MCS28, 20MHz, OTA, 64 Ant

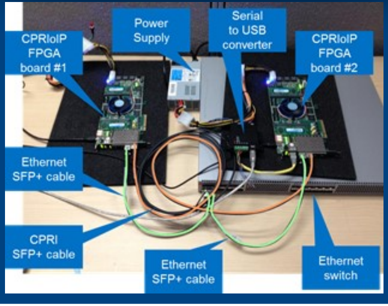
Joint demonstration with SK Telecom

Field Trial in China

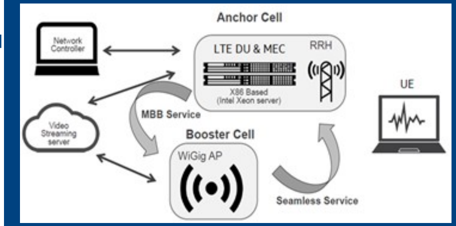
COTS platform with Wireless IP



CPRI over Ethernet



Anchor Booster

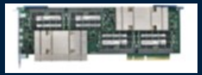


60GHz mmwave AP as booster

Joint demonstration with Korean Operator

Ultra dense COTS Platform

Ref: Artesyn* Chassis



Intel® Xeon® processor D product family-based card

Ethernet Switch Card

Altera* Arria* 10 FPGA Card

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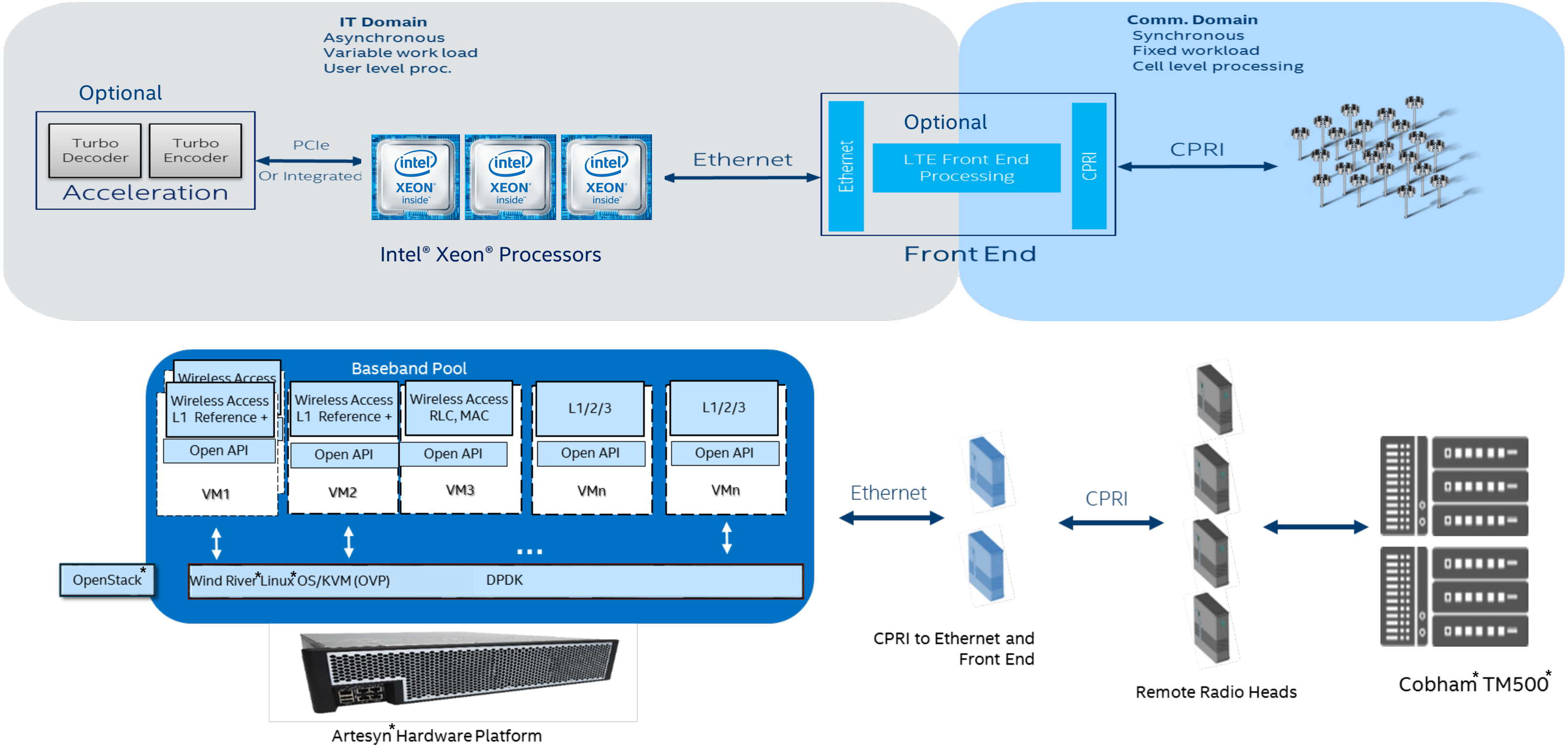
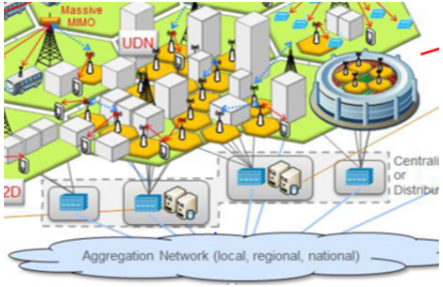
FlexRAN: Virtual RAN Architecture



Implemented operators call profiles and demo'd at MWC '2016.

FlexRAN & FlexCORE Platform For 5G

Ultra Dense Network

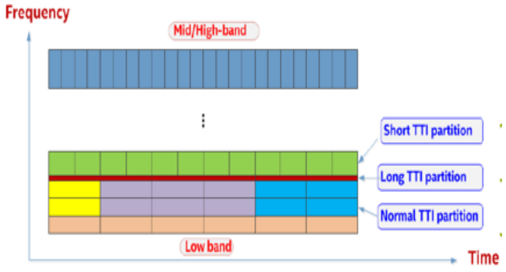


High Capacity With Shared Frequencies
Interference Cancellation
10x Performance Gain

Network Slicing

L1 To L3 Re-architecture
SDN/NFV As The Base Technology

New RAT



Low Latency
High Throughput eMBB
Massive Connections

Si Platform

5th-generation Intel® Xeon® processors

Intel® Xeon® processor D-1500 product family + separate FPGA as needed

Intel Xeon processor with integrated FPGA

NextGen

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5G Reference Design

Intel® Xeon® processor
D-1500 product family
(14nm)

2x Intel® Xeon® processor D-1500 product
family SoC devices/card

"n" SoC cards

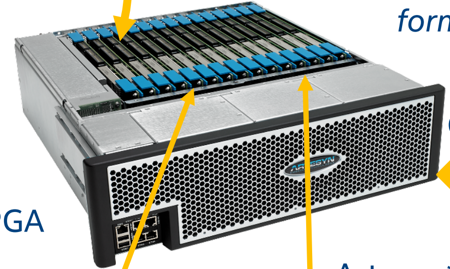
Ultra Dense Scalable and Flexible RAN
form factor design

+

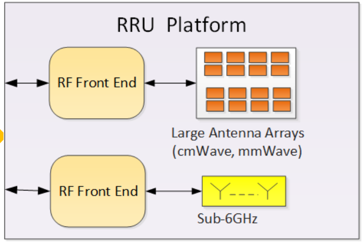
20nm

Intel 14nm

"m" FPGA
cards



CPRI/Ethernet



Artesyn* COTS
platform example

Customer defined or 3rd party vendor
- ➢ Sub 6GHz
- ➢ 28GHz

Ethernet Switch Card

IPs implemented in FPGA => Hardened IPs in
product for integration in SoC as needed

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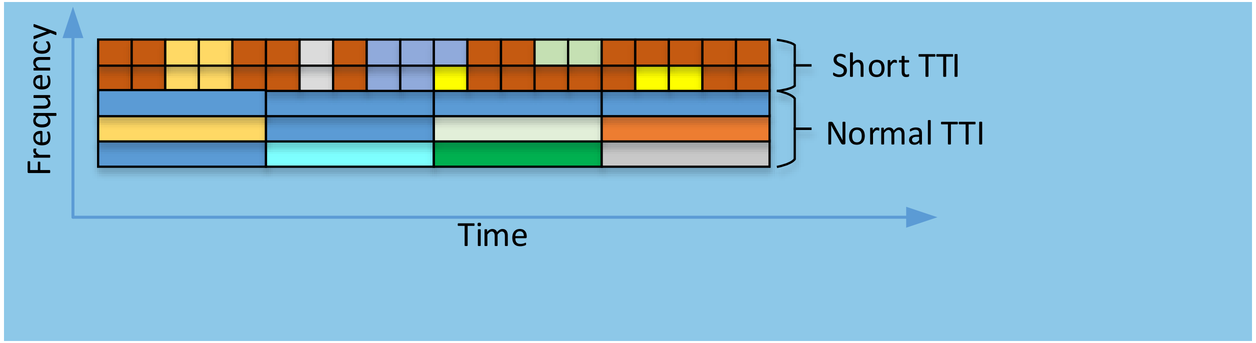
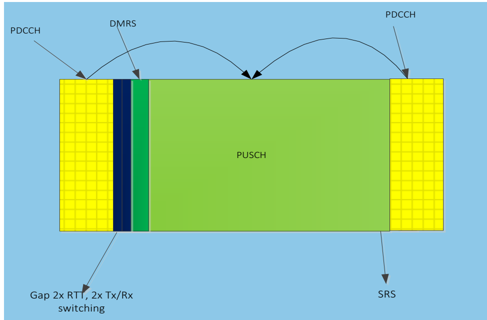
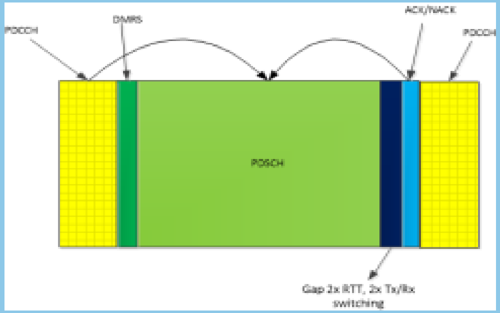
5G RAT Frame Structure: work in progress







TTI values for Slice Platform PoC: 0.2ms and 1ms
These values are driven by E2E latency requirement of 5G use cases

Frame format is based on TDD

Each frame has flexibility to carry all the control signals/channels as well as DL/UL data.

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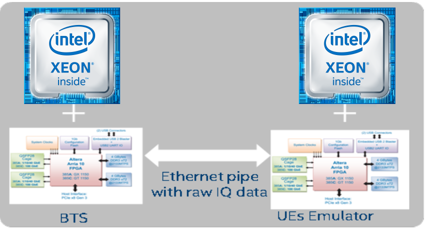
5G waveform – an example

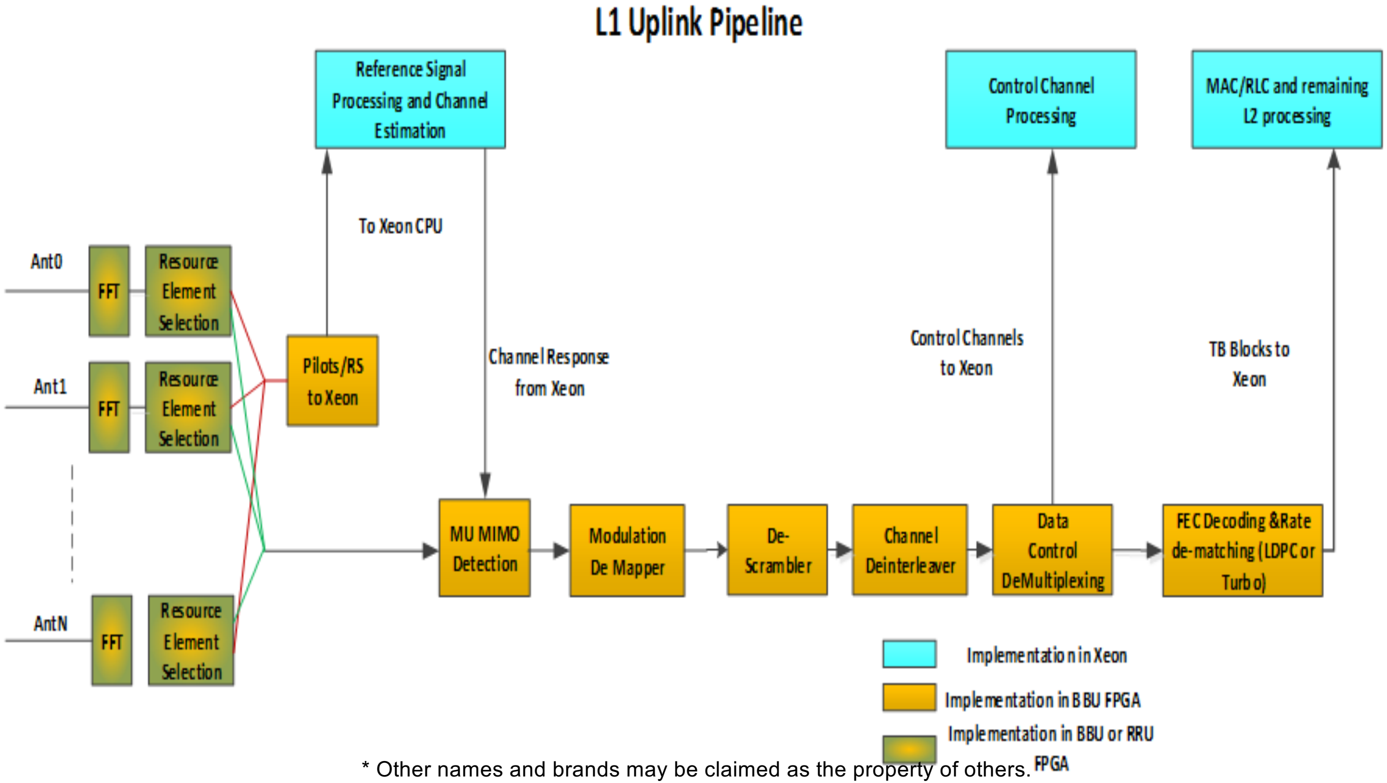
Numerology Parameter	Values for phase 1 (RF freq upto 40GHz)
TTI Duration	0.2ms, 1ms
Duplex scheme	TDD
Subcarrier Spacing	n*15KHz, n=5 for 100MHz per carrier (75KHz)
No. of subcarriers	1200
FFT size	2048
Bandwidth Scalability	m*100MHz
Basic waveform design	OFDM in both UL and DL
No. of OFDM symbols	14
Modulation	Upto 64 QAM
Coding	802.11n LDPC and Turbo (optional)
Flexible Frame Schedule	Support DL, UL Ctrl and data in the same subframe. Flexibility at symbol level
No. of Layers/streams	Upto 8 for both DL and UL
No. of Tx and Rx Antennas	8Tx/8Rx (traditional MIMO) 32-128 Tx & Rx each (massive MIMO)
Peak throughput per 100MHz carrier	2.9Gbps (64QAM, 5/6 coding rate for LDPC)

5G NETWORK SLICE (Phase 1 – Uplink)

Target Config using Intel® Xeon® processor + single Altera* Arria* 10 FPGA :
3x100MHz carriers :8 Streams & 8Tx/8Rx each at 0.2 ms TTI.
Phase 1 is focused on the datapath only; Control processing added in phase2



- Phase 1a uses Ethernet wired interface between UE and BTS
- Phase 1b: Integrate RF front end from 3rd party vendor or customer/partner provided



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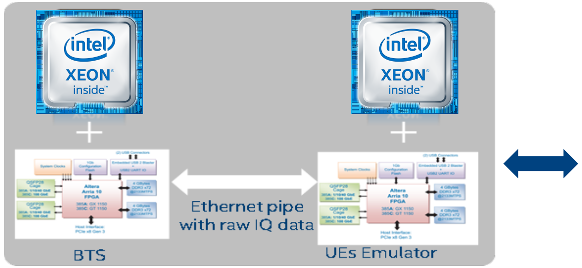
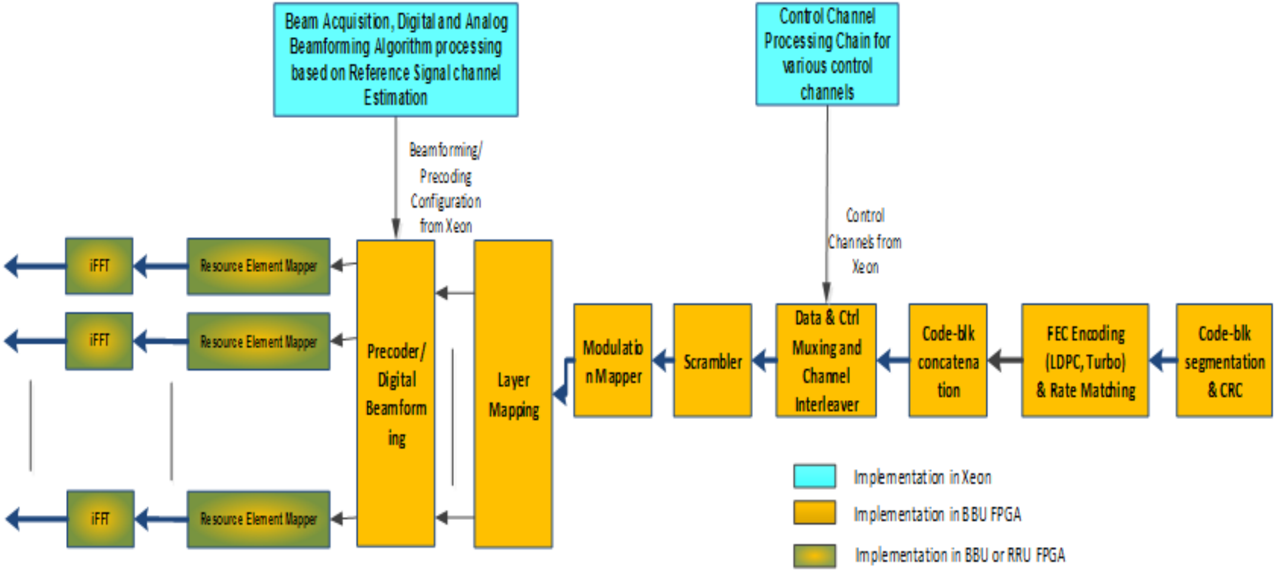
5G NETWORK SLICE (Phase 2 : Downlink + Uplink)

Includes Phase 1+ downlink and control channel processing



- Phase 2a uses Ethernet wired interface between UE and BTS.
- Phase 2b: Integrate RF front end from 3rd party vendor or customer provided.

L1 Downlink Pipeline



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Massive MIMO Phase 1
Joint Demonstration with SK Telecom*

UE RF (USRP*)

Video Client , Server (Intel® Xeon® Processor)

UE Emulators (Intel Xeon Processor)

BBU Server (Intel Xeon Processor)

BBU FPGA & Intel Xeon Processor-based Controller

Mega USRP* for BTS RF, Antennas 1-64

- 8 streams at MCS28 with total throughput of *590Mbps* tested over the air interface
- 1ms TTI, 20MHz

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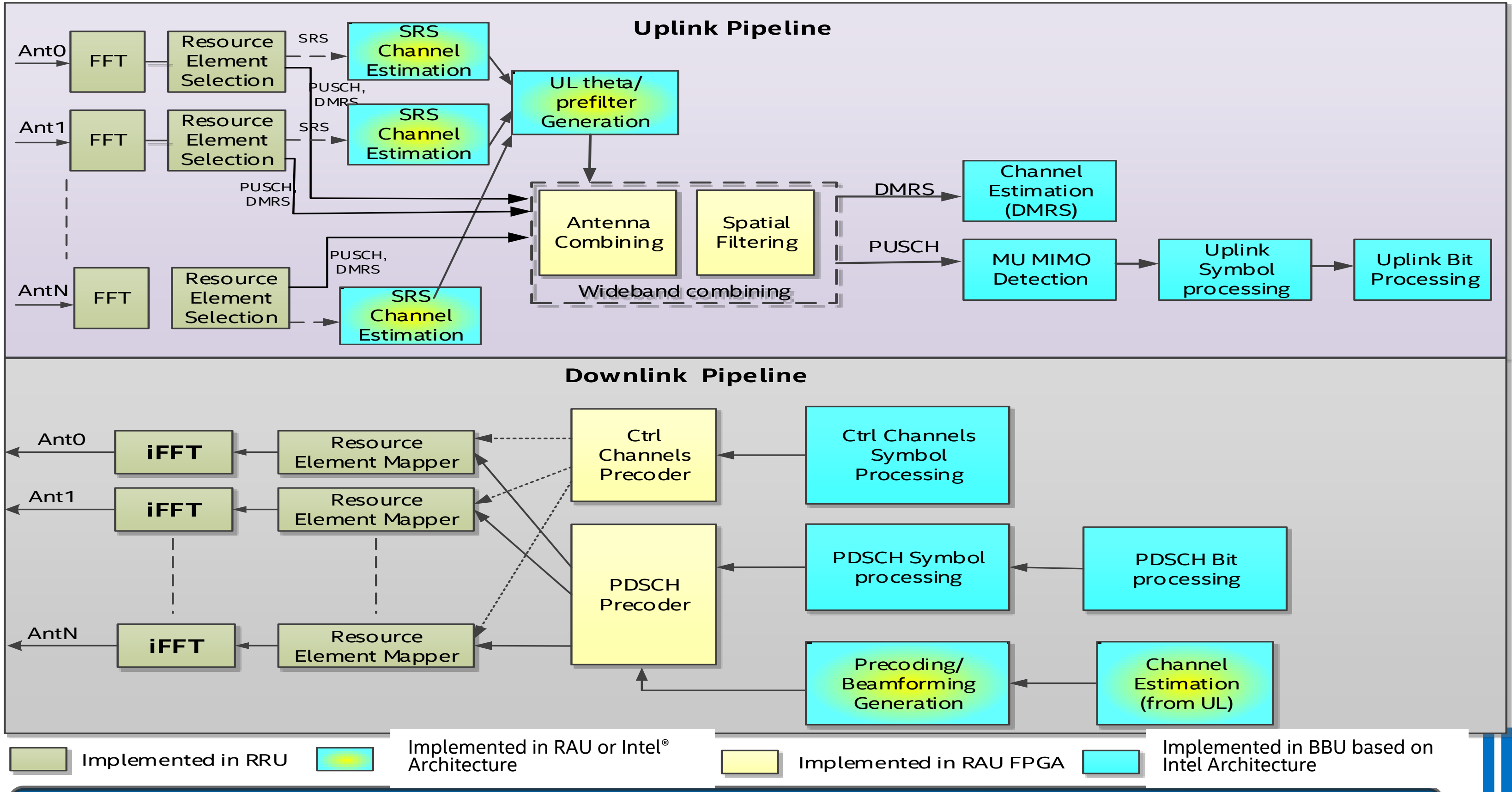
Massive MIMO L1Baseband Pipeline



Flexible L1 pipeline partitioning between RRU, RAU and BBU

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Summary & Call to action

- Static, “Purpose Built”, Vertical Network does not comprehend the use cases of next 10 years & beyond
- Intel making one of the largest investments in Silicon, reference SW and technology proof points for 5G network
- Lot of money will be made in developing next generation use cases that runs on 5G network platforms (like real time gaming, connected healthcare, massive/mission critical IOT)
- Developers can use Intel’s “off the shelf” servers and reference SW to develop next generation 5G uses cases

Technical Sessions in Road to 5G Track

Tuesday, August 16, 2016

1:15 PM – 2:15 PM *R5GBI01* — 5G: A Transformative Force Across Industries – Business Insights ***Level 2 Room 2016 Tech & Business Insight***

4:00 PM – 5:00 PM *R5GTS01* — 5G: Redefining Mobility ***Level 2 Room 2002***

Wednesday, August 17, 2016

11:00 AM – 12:00 PM *R5GTS02* — IoT Opportunities Enabled by 5G ***Level 2 Room 2003***

1:15 PM – 2:15 PM *R5GTS03* — Scalable 5G Massive MIMO Design with Intel® Xeon® Platforms ***Level 2 Room 2004***

2:30 PM – 3:30 PM *R5GTS04* — 5G Trials: Virtual RAN & Mobile Edge Computing ***Level 2 Room 2009***

4:00 PM – 5:00 PM R5GTS06 — CloudCell: Cell-less Network on IA ***Level 2 Room 2009***

Thursday, August 18, 2016

1:00 PM – 2:00 PM *R5GTS05* — Intel® Technology to Power the 5G Network: An Architecture Deep Dive ***Level 2 Room 2008***

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