Brian Pham

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Education

California State University, Long Beach | Long Beach, CA

Bachelor of Science in Electrical Engineering, DSP/Communications Emphasis, GPA: 3.94   August 2022 – December 2024

Golden West College | Huntington Beach, CA

Associate of Arts in Computer Science and Technology, Mathematics, and Science, GPA: 4.00   June 2020 – May 2022

Skills

Languages: MATLAB, VHDL, C++, Python, ARM Assembly

Software: Simulink, Xilinx Vivado, System Generator, Vitis Model Composer, Keil µVision, NI Multisim, AutoCAD, Microsoft Visual Studio/Code, Microsoft Office Suite

Certifications: Machine Learning Onramp, Learning FPGA Development

Organizations: CSULB Institute of Electrical and Electronics Engineers Student Chapter, Society of Asian Scientists and Engineers

Experience

CSULB Multi-disciplinary Neural Networks and DSP Lab | Long Beach, CA

Research Assistant   November 2023 – Present

- Conducted research on hall sensor characteristics and applications for speed and position capturing in a motor.
- Analyzed and worked on Simulink models for BLDC motor scope outputs and commutation logic.
- Attended weekly meetings for the research group to discuss and present progress reports.

CSULB Electrical Engineering Department – Electric Circuits Lab | Long Beach, CA

Instructional Student Assistant   February 2024 – May 2024

- Guided students through the design of electric circuits and the use of lab equipment such as DC power supplies, function generators, digital multimeters, and oscilloscopes.
- Explained theoretical concepts for the different techniques used for linear circuit and transient analysis.
- Proctored quizzes and did preparation for the lab experiments.

CSULB Electrical Engineering Department – Microprocessor Principles | Long Beach, CA

Teaching Assistant   August 2023 – December 2023

- Instructed students through the installation of Keil µVision software and resolved technical issues.
- Discussed assembly language code concepts and topics to students and aided students with debugging code.
- Graded lab assignments, quizzes, midterm, final, and held review sessions for the quizzes and midterm.

Projects

MAC-Based FIR Filter | DSP for Multimedia Communications   February 2024 – April 2024

- Realized a MAC based FIR filter using Simulink and System Generator to generate VHDL code used in Xilinx Vivado and implemented on a Basys 3 FPGA board which was tested through JTAG hardware co-simulation.
- Assembled and configured subsystems using the Xilinx block set for the control logic to control the storage of samples and coefficients and the memory to store the data using dual-port RAM.
- Created logic blocks for padding and unpadding data to force the conversion of data types, reinterpret unsigned or signed data, combine buses, and extract certain bits of data.

Digital Lock System | Digital System Design   April 2023

- Designed and implemented a digital lock module through Xilinx Vivado and VHDL code on a Nexys 4 DDR FPGA board, utilizing buttons and LED lights on the board to verify the inputs and outputs.
- Developed a Moore type state diagram to describe the behavior of the lock and analyzed simulation waveforms of test bench code to verify the results of the system.
- Incorporated a debouncing module to prevent mechanical debouncing input errors when the input buttons on the FPGA board are used.

Relevant Coursework

Completed: Digital Logic Design, Electric Circuits, Digital System Design, Analog Electronics I, Microprocessor Principles, Electromagnetic Fields, Control Systems, Probability and Statistics, Communication Systems I, Digital Signal Processing, DSP for Multimedia Communications

In Progress: Analog Electronics II, Communication Systems II, Digital Filter Design and Audio Processing, DSP Design, EE Design