Full-Custom Layout Techniques – Lab Number 5

Author	:	Brian Landy
Lab Instructor	:	Sayed Ashraf Mamun
TA	:	Andrew Fountain
TA	:	Sabrina Ly
Lab Section	:	Lab #2
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ABSTRACT

One-bit adder circuits are an extremely vital part of many digital designs. Another important concept in digital design is the layout. A layout allows a circuit to be transcribed from a transistor diagram to a physical circuit using materials. This allows for a circuit to be fabricated. Pyxis layout was used in the exercise. This process of design through layout is great for speed optimization. This exercise successfully demonstrated the benefits of custom layouts and the process of making a circuit layout. A 4-bit ripple carry adder was constructed and the outputs were timed and compared to the generated circuit from a higher-level schematic. The performance of the generated layout was a maximum input frequency of .288 GHz and a max throughput frequency of .534 GHz. The customized layout had a max input frequency of .285GHz and a max throughput frequency of .4632GHz. This successfully demonstrated that custom layout was done properly in this exercise.

DESIGN METHODOLOGY

A 4-bit ripple carry needed to be built in this exercise and to create a circuit like this, many 1-bit adders are strung together. Figure 1 shows the 4-bit ripple carry adder schematic.

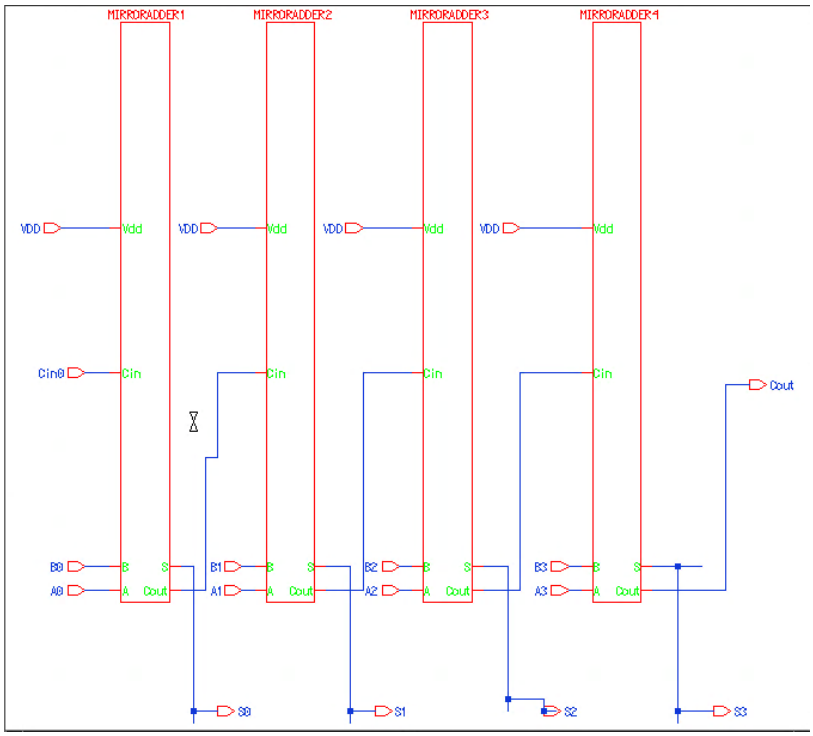

Fig. 1: Schematic for a 4 Bit Ripple Carry Adder Circuit

The circuit shown has 3 varying inputs, A and B which are 4-bit binary numbers and Cin, a 0 or a 1. The outputs Are a 4 bit sum out and a carry out. Each bar in the circuit schematic is a 1-bit adder circuit. This adder circuit (mirror adder) does a very important computation and the result bit is set and the carry is sent into the next layer of the circuit. To achieve N bit input, just keep adding 1-bit adders and input bits to the circuit. There will always

be 1 1-bit carry in and carry out. The 1-bit adder circuit is shown in transistor level detail below with appropriate transistor widths assigned.

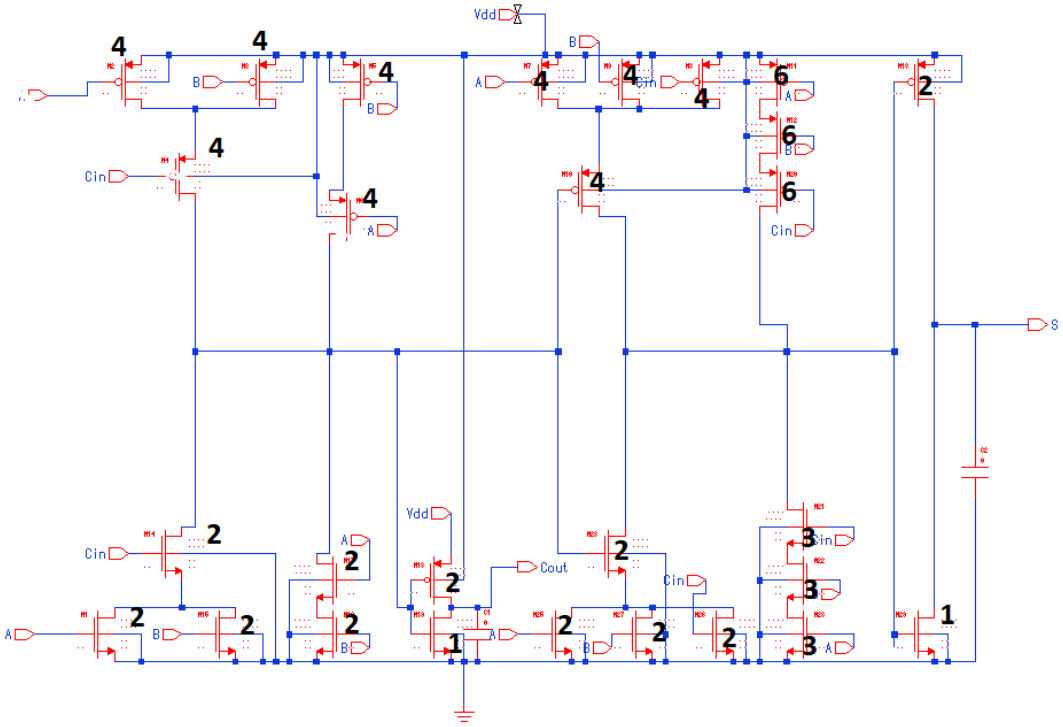

Fig. 2: Transistor Level Schematic for a 1 Bit Mirror Adder Circuit

This circuit is the vertical bar shown in figure 1. Through some simple digital logic, the Cin, an and B bits are combined in such a way that they are added and presented at the output terminal S as well as the carry out bit from the operation. In this exercise, this circuit will be laid out using Pyxis layout to make a circuit that can be fabricated. To do this, the circuit needs to be organized in a linear fashion. To do this, a Euler path is drawn through the entire circuit in one line. The bottom should mirror the top. The Euler path for this circuit is shown in figure 3.

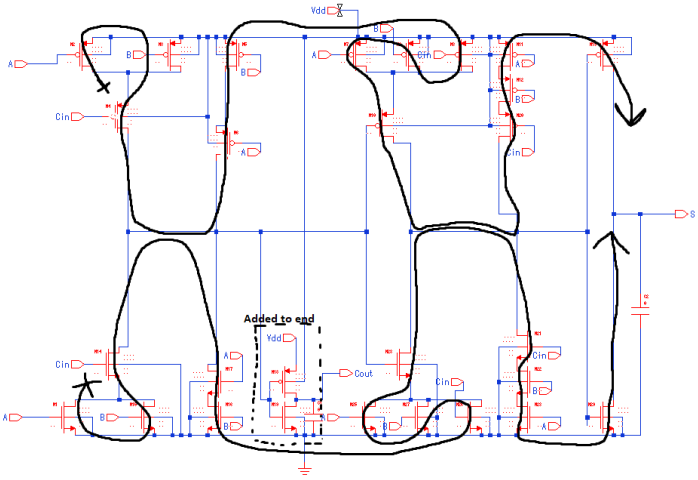

Fig. 3: 1 Bit Mirror Adder Euler Path

By using this Euler path, a linear listing of transistors can be created for the layout. This path is used to determine the order of polysilicon gate connections in the layout. The path starts with A then goes through B and so on. So, in the layout, the first gate will be A, then B and so on. This is illustrated in figure 4, the stick diagram for the entire 1-bit adder circuit.

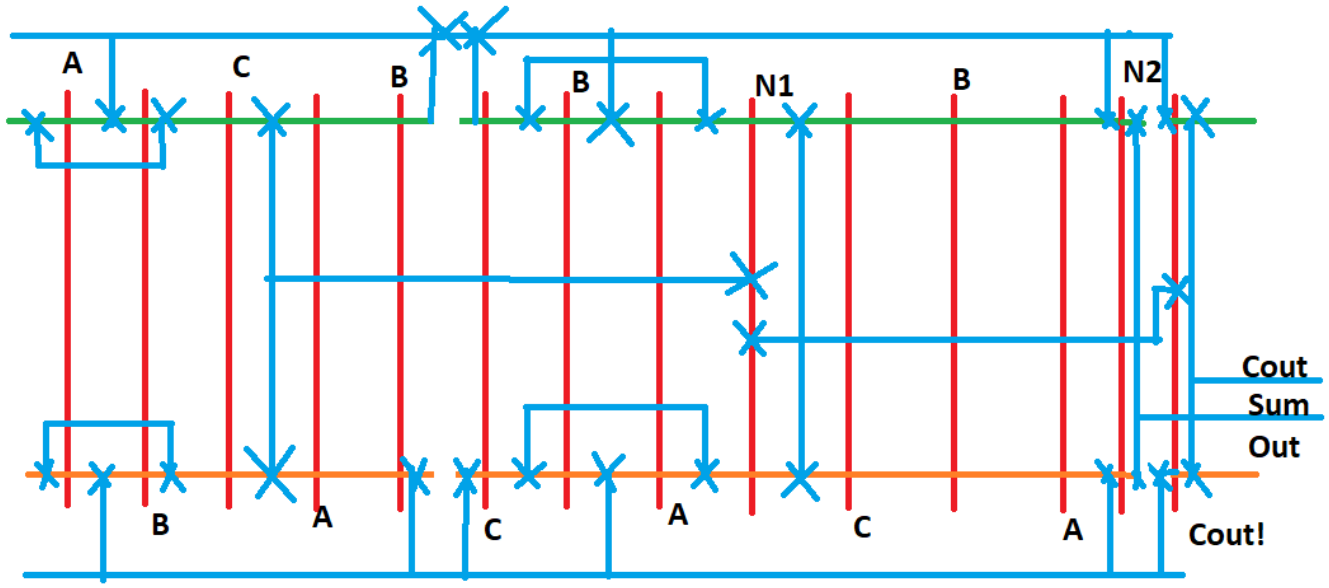

Fig. 4: 1 Bit Mirror Adder Euler Path

By using the stick diagram, a layout can be made quite simply. This stick diagram has an inverter at the end of each output line. Cout is passed from the fist half of the layout to the second to aid in the evaluation of the sum output. There is an inverter for sum and Cout at the end on the right in figure 4. The second from the top lines are the p substrate which has holes for the transistors. The second from the bottom is the NMOS substrate which has extra electrons for the transistors. The top and bottom are VDD and Ground terminals. The 14 vertical lines are the poly silicon gates. Each one represents on transistor gate connection. The letters show what input goes to each gate. The lines with X marks are the metal connections and contacts (X's) that bring the whole circuit together to achieve the desired operation. This diagram will aid greatly in determining the final layout circuit. It needs to be replicated in Pyxis.

To discuss the performance of a circuit, the maximum input and through put frequencies are calculated. By using equation 1 and 2, this can be done. These values will serve as the comparators for the pre layout and post layout circuits.

$$F\ In\ Max = \frac{1}{rise\ time + fall\ time}$$

Equation 1. F Input Max calculation

$$F\ \text{througput Max} = \frac{1}{Tp,HL + Tp,LH}$$

Equation 2. F throughput max calculation

The rest of the exercise involves constructing the layout of the 4-bit ripple carry adder and comparing it functionally to the generated schematic and comparing it with respect to time and frequency performance of the generated schematic.

RESULTS & ANALYSIS

The circuit was created using Pyxis Layout and simulated to verify the results were identical to the generated version from the schematic. The number of transistors in the circuit were 14 NMOS and 14 PMOS for the 1-bit adder. This means the overall design of the 4-bit adder had 112 transistors with 56 N and 56 P. The one-bit adder was built according to the stick diagram and is shown in figure 5.

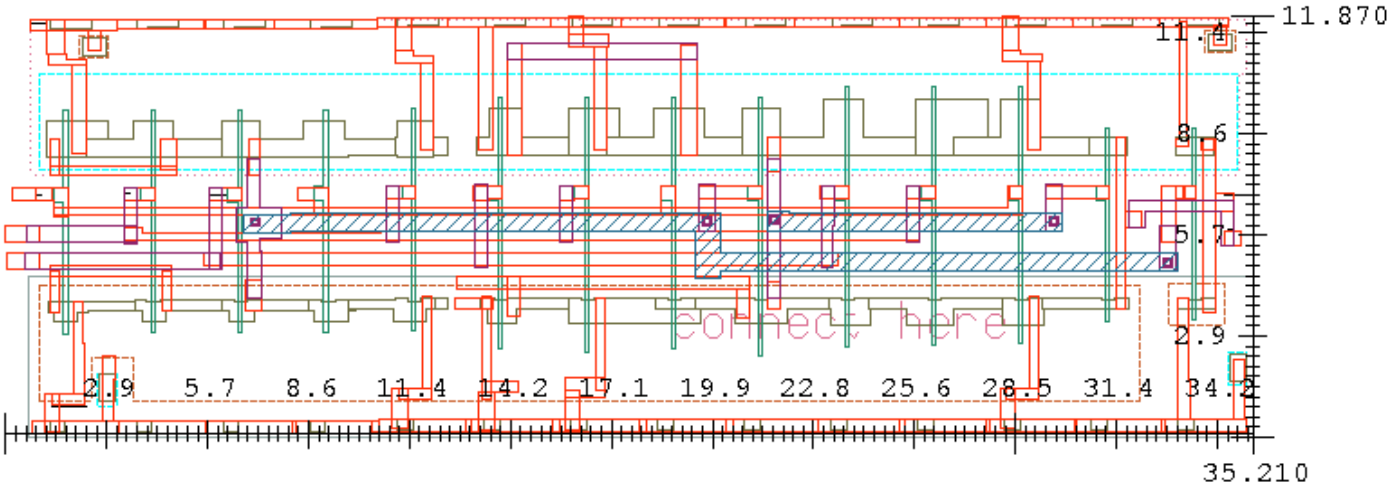

Fig. 5: 1 Bit Mirror Adder Layout

Upon closer inspection this layout looks very similar to the stick diagram. It has the separate parts for Cout and Sum out. The input gates are all the same and the only difference is the amount of path direction changes needed for the metal to not cross over itself. To cross metals over each other, via material was used to connect 2 metal layers. Then the metal could be laid on top or underneath and they would not interact. Then use via again to bring the metal back to the appropriate layer for correct operation. The transistor widths were adjusted accordingly per figure 2. The total area of this layout is 11.870um by 35.210um. Using this single bit adder, a larger 4-bit adder could be created using the Pyxis tool. This was done and is showman figure 6.

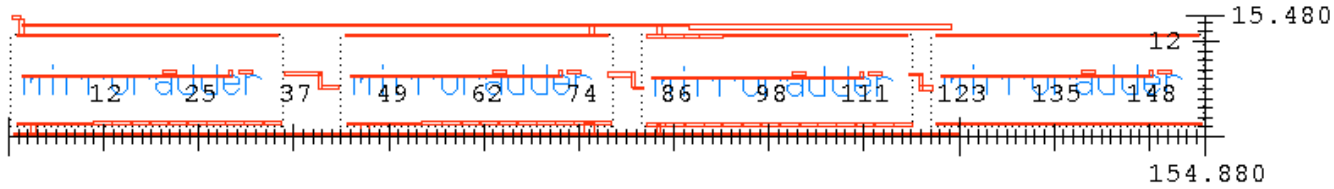

Fig. 6: 4 Bit Mirror Adder Layout

The four-bit ripple carry adder is strung together by metal paths in the same way that the circuit in figure 1 is connected. Each input bit for A and B is attached to the corresponding bit addition unit and the outputs of each

are connected to port outs. The carry in and out ports are also taken care of. The area of the whole layout is 15.480 um by 154.880 um. By using this circuit with the Eldo simulator, timing results can be achieved, and the 2 models of the same circuit can be compared. This circuit passed DRC and LVS and was fit to simulate. Using a simple circuit file with bit patterns the results were compared.

Before layout was done, the circuit was simulated. The functional results sum out MSB, Cout and Cin are shown in figure 7.

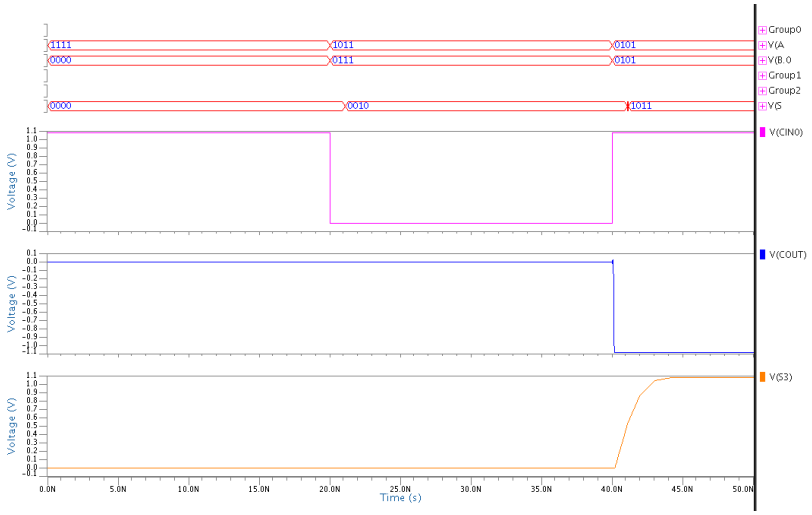

Fig. 7: Plotted Mirror Adder Pre-Layout Signal Voltages with Bit Pattern Transient Analysis with profile (T = 125 degrees C, 1.08V on VDD, C=120F)

The functionality is correct as shown in the 3 cases at the top of the waves. The additions of A+B =S and C are correct. The layout was also simulated for functional correctness. The 2 were compared. Figure 8 shows the functional correctness of the 4-bit ripple carry adder post layout.

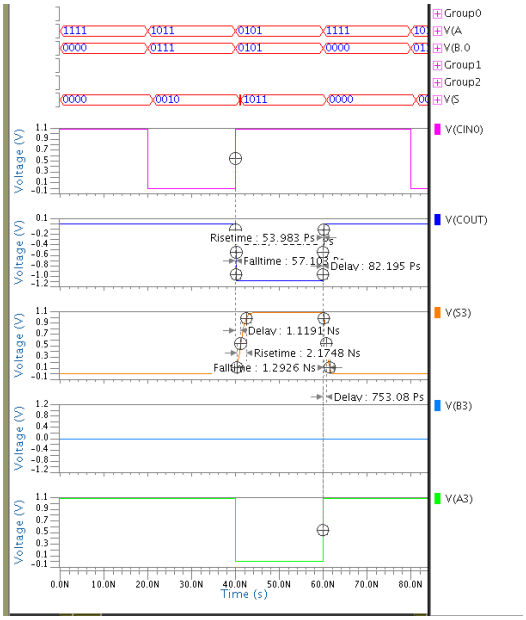

Fig. 8: Plotted Mirror Adder Post Layout Signal Voltages with Bit Pattern Transient Analysis with profile (T = 125 degrees C, 1.08V on VDD, C=120F)

These waves in figure 8 also illustrate functional correctness and the signals have the same behavior. The next step to verify that layout works as expected is to time both models and see what the results show. The timing of the waveform of the pre layout circuit is shown in figure 9.

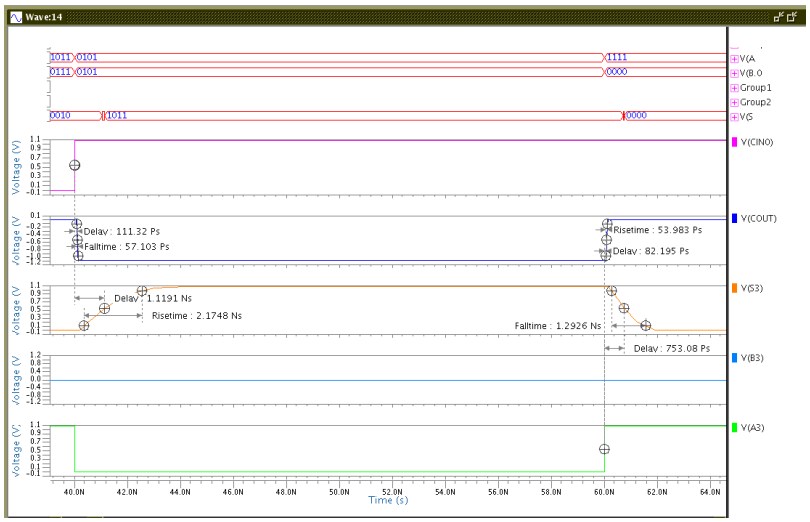

Fig. 9: Timed Plotted Mirror Adder Pre-Layout Signal Voltages with Bit Pattern Transient Analysis with profile (T = 125 degrees C, 1.08V on VDD, C=120F)

These times are recorded and are to be used in comparisons of the 2. The timing of the waveform of the post layout circuit is shown in figure 10.

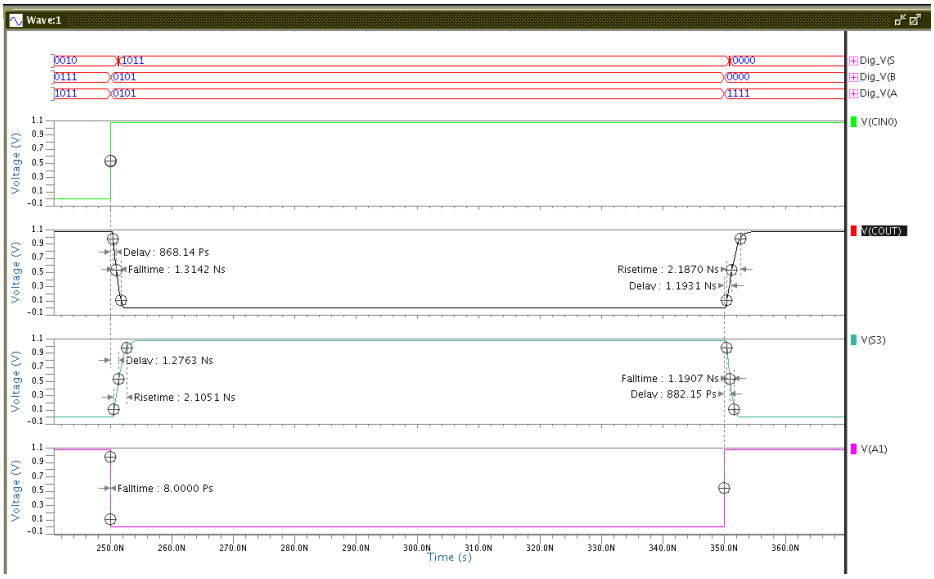

Fig. 10: Timed Plotted Mirror Adder Post Layout Signal Voltages with Bit Pattern Transient Analysis with profile (T = 125 degrees C, 1.08V on VDD, C=120F)

Tables 1 through 3 are the timing results of the circuits that are being analyzed.

Table 1: Sum MSB Output Results

	V_{DD} [V]	Temp [°C]	Load Capacitance [fF]	Rise Time [s]	Fall Time [s]	$T_{P,HL}$ [s]	$T_{P,LH}$ [s]	$F_{input, max}$ [Hz]	$F_{Throughput, Max}$ [Hz]
Pre-Layout	1.08	125	120.00	2.17E-09	1.29E-09	7.53E-10	1.12E-09	2.88401E+08	5.34137E+08
Post Layout	1.08	125	120.00	2.11E-09	1.19E-09	8.82E-10	1.28E-09	3.03416E+08	4.63295E+08

Table 2: Carry Output Results

	V_{DD} [V]	Temp [°C]	Load Capacitance [fF]	Rise Time [s]	Fall Time [s]	$T_{P,HL}$ [s]	$T_{P,LH}$ [s]	$F_{input, max}$ [Hz]	$F_{Throughput, Max}$ [Hz]
Pre-Layout	1.08	125.00	120.00	5.40E-11	5.71E-11	1.11E-10	8.22E-11	9.00203E+09	5.16756E+09
Post Layout	1.08	125.00	120.00	2.19E-09	1.31E-09	8.68E-10	1.19E-09	2.85616E+08	4.85145E+08

Table 3: Overall Worst-Case Output Results

	V_{DD} [V]	Temp [°C]	Load Capacitance [fF]	Rise Time [s]	Fall Time [s]	$T_{P,HL}$ [s]	$T_{P,LH}$ [s]	$F_{input, max}$ [Hz]	$F_{Throughput, Max}$ [Hz]
Pre-Layout	1.08	125.00	120.00	2.17E-09	1.29E-09	7.53E-10	1.12E-09	2.88401E+08	5.34137E+08
Post Layout	1.08	125.00	120.00	2.19E-09	1.31E-09	8.82E-10	1.28E-09	2.85616E+08	4.63295E+08

The timing results presented valuable information about the 2 circuits. IT turns out that the layout method was not always worse than the schematic generation method. This is surprising because the diffusion regions of the layout are larger than necessary. In some cases, the layout even performed better. When looking at the results overall, the performance of the generated layout was a maximum input frequency of .288 GHz and a max throughput frequency of .534 GHz. The customized layout had a max input frequency of .285GHz and a max throughput frequency of .4632GHz. This successfully demonstrated that custom layout was done properly in this exercise.

CONCLUSIONS

This exercise was a success in working with circuit layouts for fabrication in Pyxis. One-bit adder circuits are an extremely vital part of many digital designs. Another important concept in digital design is the layout. A layout allows a circuit to be transcribed from a transistor diagram to a physical circuit using materials. This allows for a circuit to be fabricated. Pyxis layout was used in the exercise. This process of design through layout is great for speed optimization. This exercise successfully demonstrated the benefits of custom layouts and the process of making a circuit layout. A 4-bit ripple carry adder was constructed and the outputs were timed and compared to the generated circuit from a higher-level schematic. The performance of the generated layout was a maximum input frequency of .288 GHz and a max throughput frequency of .534 GHz. The customized layout had a max input frequency of .285GHz and a max throughput frequency of .4632GHz. This successfully demonstrated that custom layout was done properly in this exercise.

CMPE 530/630 Digital IC Design
Lab 5. Full Custom Layout Techniques

Student's Name: Brian Lundy Section (circle one): Wednesday / Friday

In Lab Performance	Point Value	Points Earned	TA/Instructor Signature
4-bit ripple-carry adder schematic	5	5	
Stick diagram of mirror adder	10	10	
Good LVS report and good DRC for the 1-bit mirror adder layout	20	20	
Good LVS report and good DRC for the 4-bit mirror adder layout	10	10	
Post and pre-layout timing results for the 4-bit adder	5	5	

Report		Point Value	Points Earned	
Abstract		5		
Design Discussions		10		
Results and Analysis	Data table, waveforms	15		
	Analysis & explanation	15		
Conclusion		5		

Total for lab performance & report	100		

* **Bring a PRINTOUT of this sheet for In-Lab grading**
* **Student MUST ATTACH this sheet with the submitted lab-report**