Layout of CMOS Logic Gates – Lab Number 4

Author   :   Brian Landy
Lab Instructor   :   Sayed Ashraf Mamun
TA   :   Andrew Fountain
TA   :   Sabrina Ly
Lab Section   :   Lab #4
Submission Date :   10/11/2019

Table of Contents

ABSTRACT

Complementary metal-oxide semiconductor (CMOS) devices are extremely valuable circuit components as they allow for small digital logic circuits to be placed in an extremely small amount of area on a chip. These circuits are fast and complex tools can synthesize designs, but the way to get the fastest and most highly customized circuits are to design these circuits with layout tools. In this lab exercise, layout tools were used to design a CMOS inverter circuit. The results of timing and simulation were compared to the generated version of the circuit. This lab successfully showed the importance of custom layouts and that a speed benefit can come from custom layouts. Pyxis layout was used. Various design rule checks were adhered to in this procedure as the layout needs to be able to be fabricated. That is what design rules are for. The timing results were also recorded so important metrics could be calculated like through put maximum and input maximum frequencies. When looking at the worst-case results of the schematic method and the layout method, the maximum throughput and input frequencies were 16.4GHz and 8.3GHz for the layout. For the schematic the results were 27.7GHz and 10.3GHz for throughput and input frequencies respectively. The schematic method was faster, and this is probably due to intense optimizations for the tool and the fact that this is a trivial circuit. Nontrivial circuits will likely show a better performance increase with a custom design.

DESIGN METHODOLOGY

A CMOS layout consists of a few materials organized in a specific way to get the proper results. The design for the circuit in this exercise was generated using the cross section of an inverter provided in the exercise handout. Figure 1 shows the cross section of the inverter (RIT CMPE Lab4 1).
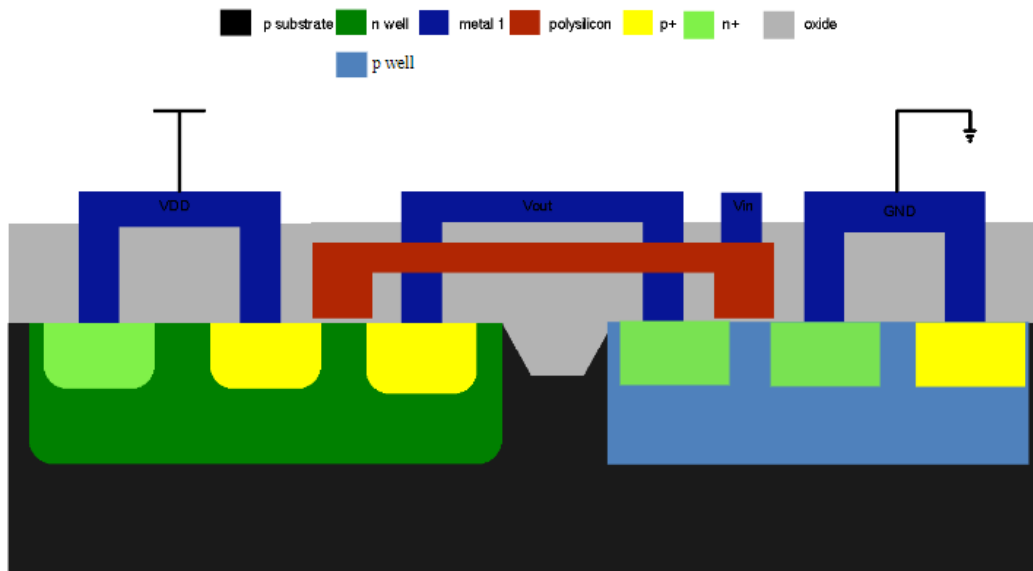
Fig. 1: CMOS Inverter Cross Section (RIT CMPE Lab 4)

This cross section contains all the important parts of the design that needed to be considered. The purpose of the design using the layout tool is to maximize speed. The layout tool has many different material types. The NMOS portion had a p well to on it, and the NMOS portion had an n well in it. These 2 bodies were connected through metal links and a polysilicon gate. And at the connector points between the metal and the well, there was either a

P+ region or an n+ region. And lastly, there was a diffusion region over all the areas with connections. The nwell creates negative charge and the pwell creates positive charge. The current then flows through the regions with specific voltages applied to the terminals. There is a design rule set to follow. A design rule is one which needs to be followed for the actual circuit to function properly and to be able to be created in the fabrication process. This includes material sizing, placement and widths and lengths as well as other things. By following these rules, the layout in figure 2 was created for the exercise. It is a CMOS inverter.
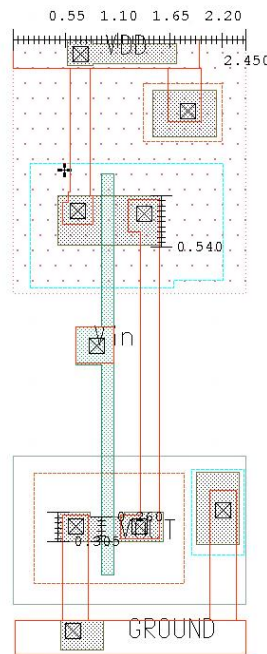
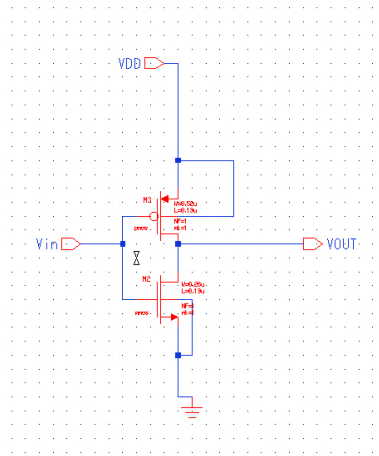**Fig. 2:** CMOS Inverter Layout

The figure contains all materials. The orange rectangles are metal lines. The red polka dots are the nwell region. The light blue dotted lines are p+ regions. The half shaded grey areas are diffusion regions. The little black squares are contact points where the layers can connect. The orange dotted section is an n+ area and the greyish area surrounding it is the pwell. Lastly, the greenish long portion in the middle of the layout is the polysilicon gate. The input voltage passes through the gate and the output is connected to a piece of metal that touches the PMOS and NMOS. The ground is connected to the NMOS side and the PMOS side is connected to VDD. The body connections are also set up and if they were not, the circuit would not properly function at all. The portion where the polysilicon touches diffusion is the transistor width metric. The length of the gate strip is the transistor length. The PMOS width is double the NMOS width as per a unit inverter. Metal is used because it is good at carrying charge. The polysilicon is used because it is good at carrying charge when under the correct operating conditions. The n and p wells are good for providing electrons or charge and receiving charge or providing holes. The doped regions, n+ and p+ are used to make the substance act more like a conductor than it would normally be. Lastly, the diffusion region is good for providing a path for the flow.

It is necessary to follow design rules when setting up a CMOS inverter. The design rules are there to force a circuit to be built properly. Some of the things the DRC check take care of are transistor layering and boundary area, connections, minimum width and lengths and layer area. If the rules do not get satisfied, the circuit can not

be considered valid. These rules are determined by the fabrication process. There are another set of rules and comparisons for the circuit but they exist to verify the transistor matches a provided schematic. This will help determine the connections are setup right, ports match, transistor sizing matches a schematic and other thing specific to the circuit. Both checks were used in the exercise.

RESULTS & ANALYSIS

The purpose of the results section in this exercise was to compare the layout CMOS inverter with the schematic CMOS inverter. The schematic of the CMOS inverter that was used in the exercise is shown in figure 3.


Fig. 3: CMOS Inverter Schematic

This is the circuit that was used for the circuit verification step which is LVS. LVS stands for layout vs schematic and it does exactly what the name implies. This is the final check before waveform simulation takes place. The behavior of a CMOS inverter is simple. A capacitive load is applied from the output terminal to ground. This will further delay the output and increase the time it takes for the circuit to operate. It is to understand the effect of a load on the timing results. The transistor widths and lengths are also important. The NMOS width and length are .13uM and .26uM. These numbers are determined by the process being used. The PMOS needs double the width to be as powerful as the NMOS. The width is .52uM and the length is .13uM.

To simulate, first all rule checks were run and passed. Then PEX timing was done. After this had finished, a spice netlist was generated. This spice netlist was used by the Eldo simulator in conjunction with a circuit file. The circuit simulation profile file is shown in the appendix. The circuit file was just a text-based way of setting up the circuit simulation profiles. The circuit simulations were run with and without a 120fF capacitor and under nominal and worst-case conditions. The fist simulations run were the voltage characteristics of the schematic. Figure 4 shows the plot of input and output voltage for the inverter schematic. This is used as a baseline for the expectations of the simulated CMOS layout inverter.
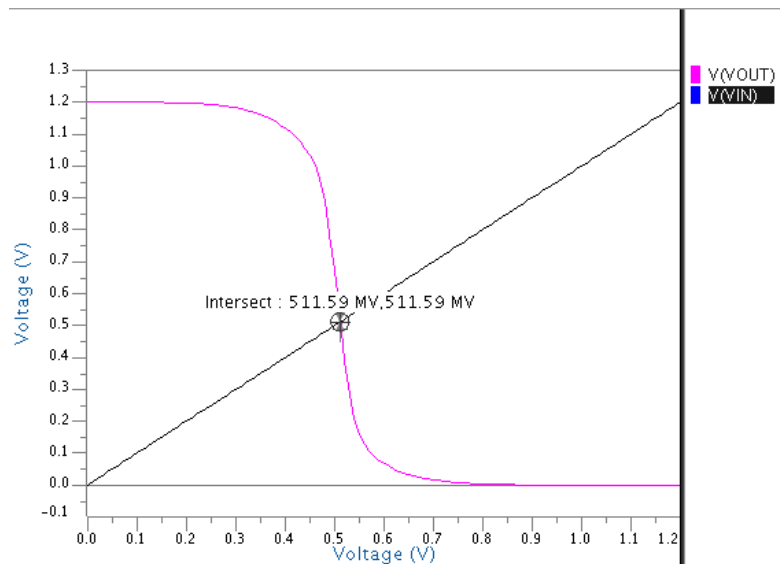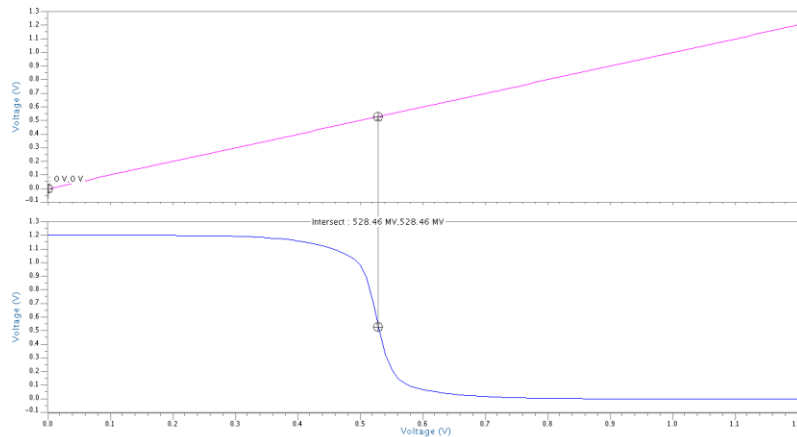
Fig. 4: Plotted CMOS Inverter characteristics using schematic with profile (T = 25 degrees C, DC signal on Vin swept from 0V to 1.2V and Vdd held constant at 1.2V)

The intersection point on the graph of Vout and Vin in figure 4 is the midpoint voltage. This is where Vout is the same as vin. Ideally, it should be right in the middle of 0 and 1 for best operation. In this case, the midpoint voltage is 511.59. The next plot is shown in figure 5 and it is a transient plot of input pulses and the inverter response. This is also from the schematic of the inverter.
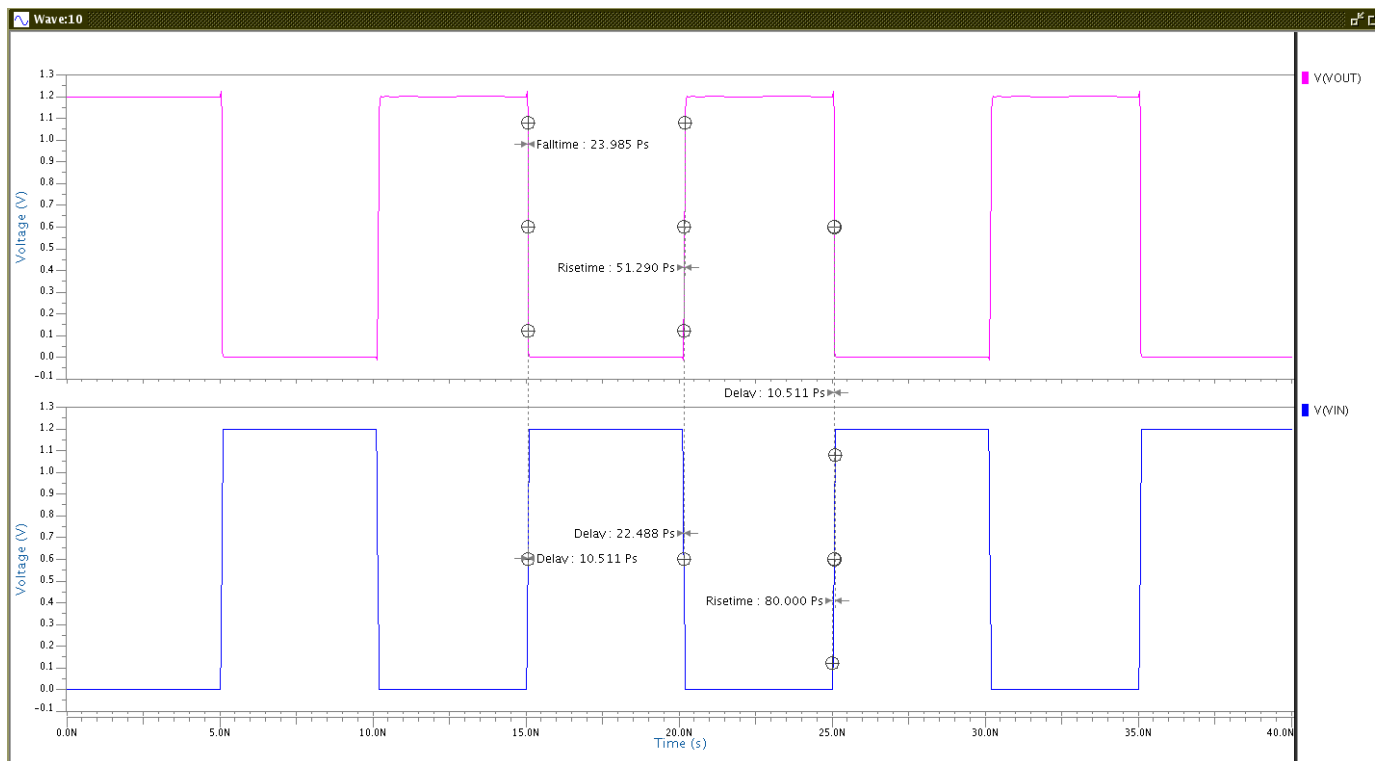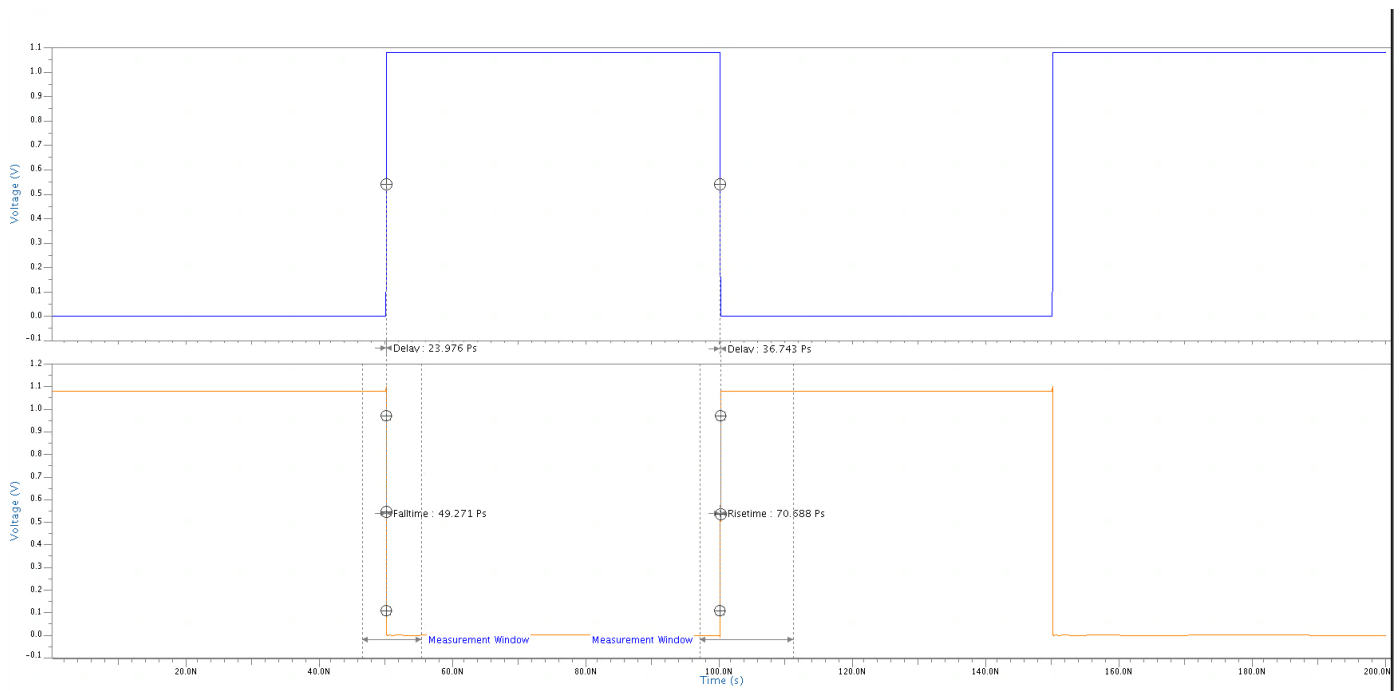

Fig. 5: Plotted CMOS Inverter Vin and Vout with 40ns transient analysis with profile (T = 25 degrees C, 1.2V Pulse on Vin swept)

The delay, rise and fall times were measured and they are shown on the plot in figure 5. These metrics will operate as a baseline for the expectations of the layout developed during this exercise. Figure 6 is the DC voltage characteristic plot of the layout.

Fig. 6: Plotted CMOS Inverter characteristics using layout with profile (T = 25 degrees C, DC signal on Vin swept from 0V to 1.2V and Vdd held constant at 1.2V)

This plot is almost the same as the inverter from the schematic but there is a slight variance in the behavior. The midpoint voltage is now at 528.46mv. This increase means the circuit is technically less receptive to noise because the midpoint voltage is closer to the theoretical midpoint of 1.2V which is .6V. The plot of the layout pulse simulation is shown in figure 7.

Fig. 7: Plotted CMOS Inverter from Layout Vin and Vout with 40ns transient analysis with profile (T = 25 degrees C, 1.2V Pulse on Vin swept)

These measurements were used to gather timing information about the inverter circuit made by the layout. The timing information from the inverter circuit with the schematic is shown in figure 1.

Table 1: Schematic Inverter Results

	V_{DD} [V]	Temp [°C]	Load Capacitance [fF]	Rise Time [S]	Fall Time [S]	$T_{P,HL}$ [S]	$T_{P,LH}$ [S]
Nominal	1.2	25	0	5.13E-11	2.40E-11	2.25E-11	1.05E-11
Nominal	1.2	25	120	1.74E-09	9.08E-10	4.65E-10	8.15E-10
Worst Case	1.08	125	0	5.39E-11	4.26E-11	2.33E-11	1.28E-11
Worst Case	1.08	125	120	2.04E-09	1.32E-09	9.58E-10	6.03E-10

The timing information extracted from these plots are shown in table 2.

Table 2: Layout Inverter Results

	V_{DD} [V]	Temp [°C]	Load Capacitance [fF]	Rise Time [S]	Fall Time [S]	$T_{P,HL}$ [S]	$T_{P,LH}$ [S]
Nominal	1.2	25	4.42E-11	5.63E-11	1.86E-11	3.37E-11	4.42E-11
Nominal	1.2	25	1.80E-09	9.22E-10	4.88E-10	8.23E-10	1.80E-09
Worst Case	1.08	125	7.07E-11	4.93E-11	2.40E-11	3.67E-11	7.07E-11
Worst Case	1.08	125	2.05E-09	1.29E-09	6.08E-10	9.67E-10	2.05E-09

The values of these tables are very similar and the best way to compare is to compare the input and throughput frequencies of the circuits. Equations 1 and 2 are the method of solving for these critical frequencies.

$$F \; In \; Max = \frac{1}{rise \; time + fall \; time}$$
Equation 1. F Input Max calculation

$$F \; througput \; MAx = \frac{1}{Tp, HL + Tp, LH}$$
Equation 2. F throughput max calculation

These equations were used to generate the worst case frequency information in table 3.

Table 3: Inverter Frequencies

Type	V_{DD} [V]	Temp [°C]	Load Capacitance [fF]	$F_{input, max}$ [Hz]	$F_{Throughput, Max}$ [Hz]
Schematic	1.08	125	0	1.037E+10	2.771E+10
Schematic	1.08	125	120	2.976E+08	6.404E+08
Layout	1.08	125	0	8.331E+09	1.647E+10
Layout	1.08	125	120	2.994E+08	6.349E+08

From the table, it is easy to see that the custom layout performed worse in almost all cases except for worst case input frequency. This is most likely since the synthesized layout is already tuned because this is a trivial circuit. More complex circuits could possibly be made to be faster through design improvements that are specific to that circuit in the layout editor. It should be noted that the effect temperature and capacitance slow circuit operation. Temperature changes the rate of transistor current flow and the added capacitance further slow delay by requiring that they be fully saturated before anything hits the output line.

The area of the layout is 15.516 uM^2 as the length is 6.465uM and the width is 2.4uM. There is one PMOS and one NMOS in the design.

CONCLUSIONS

The way to get the fastest and most highly customized circuits are to design these circuits with layout tools. In this lab exercise, layout tools were used to design a CMOS inverter circuit. The results of timing and simulation were compared to the generated version of the circuit. This lab successfully showed the importance of custom layouts and that a potential speed benefit can come from custom layouts. When looking at the worst-case results of the schematic method and the layout method, the maximum throughput and input frequencies were 16.4GHz and 8.3GHz for the layout. For the schematic the results were 27.7GHz and 10.3GHz for throughput and input frequencies respectively. Since the design is trivial, the synthesis tool is probably tuned for this sort of layout generation and so the non-custom layout was better. This is probably not always the case though.

QUESTIONS

1. From your extracted SPICE netlist, draw a picture of your inverter with the extracted parasitic capacitances and resistances. You will need the files that are included in your .sp file (.include). Briefly discuss what each RC network represents.
    a. The model is shown at the end of this explanation. Each RC network shown is a sub circuit that represents the parasitic resistances and capacitances that are associated with each node of the circuit. These passive components include all parts of the circuit, which means the transistors are shown in the RC delay model form in here. They are in this list somewhere in some combination of resistors and capacitors.
    b. Here is the drawn circuit:
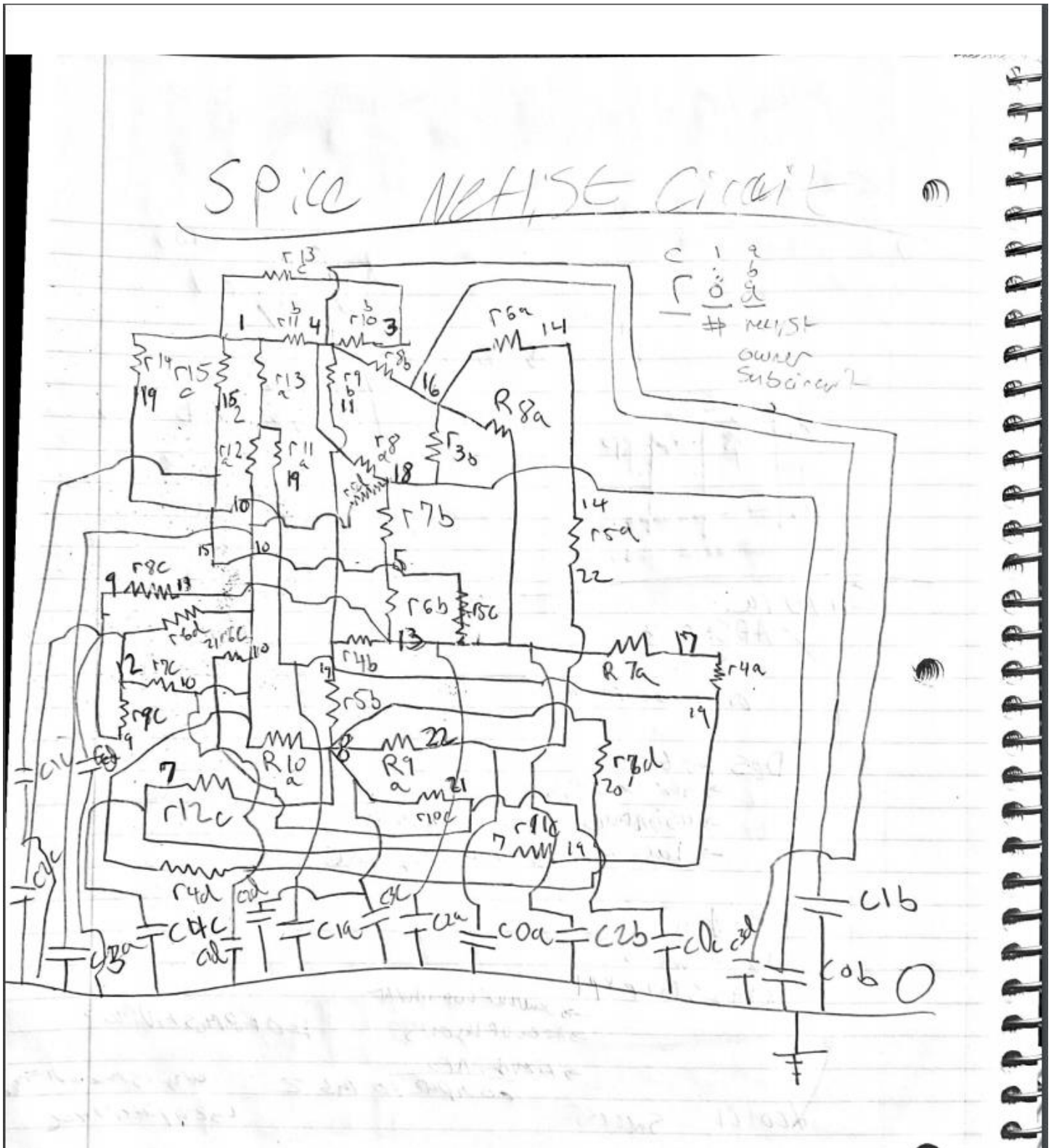
APPENDIX

Simulation Profile Circuit File:

```
* Example circuit file for simulating PEX

.INCLUDE "/home/bxl1703/Pyxis_SPT_HEP/ic_projects/Pyxis_SPT/digicdesign/inv2/inv2.cal/inv2.pex.netlist"

.LIB /home/bxl1703/Pyxis_SPT_HEP/ic_reflibs/tech_libs/generic13/models/lib.eldo TT
.LIB /home/bxl1703/Pyxis_SPT_HEP/ic_reflibs/tech_libs/generic13/models/lib.eldo TT_33
.LIB /home/bxl1703/Pyxis_SPT_HEP/ic_reflibs/tech_libs/generic13/models/lib.eldo TT_lwt
.LIB /home/bxl1703/Pyxis_SPT_HEP/ic_reflibs/tech_libs/generic13/models/lib.eldo TT_hvt
.LIB /home/bxl1703/Pyxis_SPT_HEP/ic_reflibs/tech_libs/generic13/models/lib.eldo TT_BIP
.LIB /home/bxl1703/Pyxis_SPT_HEP/ic_reflibs/tech_libs/generic13/models/lib.eldo TT_BIP_NPN
.LIB /home/bxl1703/Pyxis_SPT_HEP/ic_reflibs/tech_libs/generic13/models/lib.eldo DIO
.LIB /home/bxl1703/Pyxis_SPT_HEP/ic_reflibs/tech_libs/generic13/models/lib.eldo DIO_33
.LIB /home/bxl1703/Pyxis_SPT_HEP/ic_reflibs/tech_libs/generic13/models/lib.eldo TT_RES
.LIB /home/bxl1703/Pyxis_SPT_HEP/ic_reflibs/tech_libs/generic13/models/lib.eldo MOS_CAP
.LIB /home/bxl1703/Pyxis_SPT_HEP/ic_reflibs/tech_libs/generic13/models/res.spi res_t

* - Instantiate your parasitic netlist and add the load capacitor
** FORMAT :
* XLAYOUT [all inputs as listed by the ".subckt" line in the included netlist, in the order that they appear there] [name of the subcircuit as listed in the included netlist]
XLAYOUT GROUND VOUT VIN INV2
COUT VOUT 0 120f

* - Analysis Setup - DC sweep
* FORMAT : .DC [name] [low] [high] [step]
.DC VFORCE__VIN 0 1.08 0.01

* - Analysis Setup - Trans
* FORMAT : .TRAN [start time] [end time] [time step]
.TRAN 0 200n 0.001n

* --- Forces
* FORMAT -- PULSE : [name] [port] [reference (0 means ground)] PULSE [low] [high] [delay] [fall time] [rise time] [pulse width] [period]
*
* FORMAT -- DC    : [name] [port] [reference (0 means ground)] DC [voltage]
*
VFORCE__Vin VIN 0 PULSE (0 1.08 50n 0.1n 0.1n 50n 100n)
VFORCE__Vdd VDD 0 DC 1.08
*VFORCE__VSS VSS 0 DC 0

VFORCE__GROUND GROUND 0 DC 0

* --- Waveform Outputs
.PLOT DC V(VIN)
.PLOT DC V(VOUT)
.PLOT TRAN V(VIN)
.PLOT TRAN V(VOUT)

* --- Params
.TEMP 125
```

Extracted HSPICE netlist:

```
* File: inv2.pex.netlist.pex
* Created: Fri Oct  4 15:57:17 2019
* Program "Calibre xRC"
* Version "v2013.4_26.18"
* Nominal Temperature: 27C
* Circuit Temperature: 27C
*
.subckt PM_INV2_GROUND 1 2 16
c0 22 0 0.15714f
c1 19 0 0.281799f
c2 13 0 0.329739f
c3 10 0 0.228983f
r4 17 19 0.327298
r5 14 22 0.026824
r6 14 16 0.100282
r7 13 17 0.0453973
r8 13 16 0.188169
r9 8 22 0.0153724
r10 8 10 0.29363
r11 2 19 15.53
r12 2 10 15.61
r13 1 2 6.27522
.ends

.subckt PM_INV2_VOUT 1 3 8
c0 18 0 0.537529f
c1 16 0 0.10202f
c2 13 0 0.09945f
r3 16 18 0.0577135
r4 11 13 0.03584
r5 8 11 0.0624
r6 5 13 0.0126293
r7 5 18 1.16293
r8 4 16 15.53
r9 4 11 15.61
r10 3 4 3.51923
r11 1 4 6.01622
.ends
```

```
.subckt PM_INV2_VDD 1 3 12
c0 21 0 0.16146f
c1 15 0 0.103081f
c2 9 0 0.251373f
c3 8 0 0.23468f
c4 7 0 0.0985f
r5 13 15 0.0615211
r6 10 21 0.0254635
r7 10 12 0.044
r8 9 13 0.0351279
r9 9 12 0.173333
r10 8 21 0.0168226
r11 7 19 0.0611843
r12 7 8 0.48186
r13 1 3 3.44885
r14 1 19 15.53
r15 1 15 15.61
.ends

.subckt PM_INV2_VIN 4 8 12
c0 12 0 0.1256f
c1 10 0 0.166f
c2 8 0 0.376634f
c3 4 0 0.513364f
r4 10 20 10.0225
r5 10 18 9.82252
r6 10 12 11.07
r7 8 20 86.1538
r8 4 18 133.077
.ends
```

SOURCES

Rit CMPE Digital IC design lab 4 manual, RIT

Lab 4 Sign Off Sheet

CMPE 530/630 Digital IC Design
Lab 4. Layout of CMOS Logic Gates

Student's Name: _Brian Landy_   Section (circle one): __Wednesday / Fri__

In Lab Performance	Point Value	Points Earned	TA/Instructor Sign
Stick diagram of CMOS inverter	10	10	Amb
Good LVS report (smiley face) and good DRC	20	20	andrew
PEX timing results (tables 3 and 4 in lab writeup)	10	10	andrew

Report		Point Value	Points Earned	
Abstract		5		
Design Discussions		10		
Results and Analysis	Data table, waveforms	15		
	Analysis & explanation	15		
Conclusion		5		