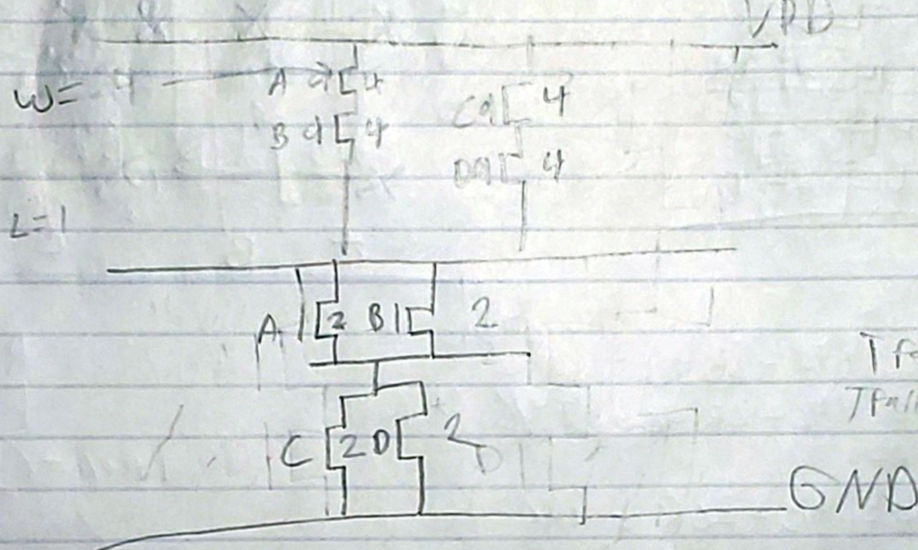
Brian Landy Digital IC design HW4

1) Rising and falling propogation delay of ... gate that implements $((A+B)\cap(C+D))'$ 1 iF

Do with RC delay + Elmore delay

0 iF



fall

$T_{fall1} = R/2 \cdot 10C + R\,10C$

$T_{fall2} = R/2\,10C + R\,10C$
$= 5RC + 10RC$

$\overline{(A+B)\cap(C+D)} \rightarrow 1$ 0 iF $(A+B)\cap(C+D) \rightarrow 0$

~~$(A\cap B)+(C\cap D)$~~

↳ So $(A+B)\cap(C+D)$ s pull down

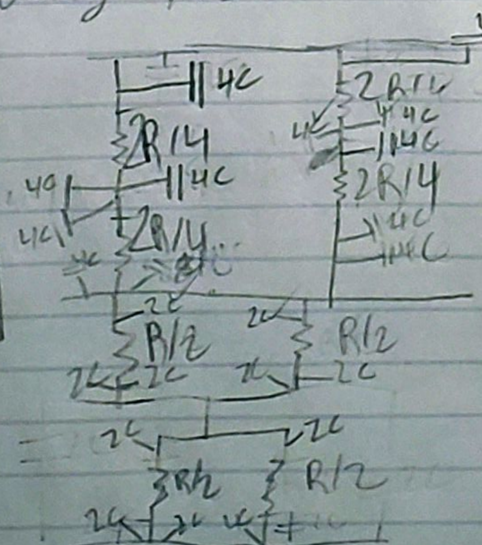
R+C delay rise + Fall

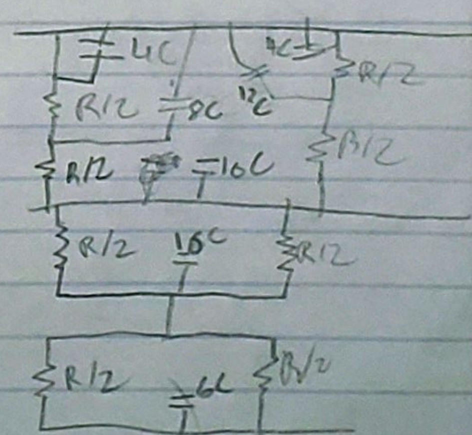
Electrically isolated trans...

ACD

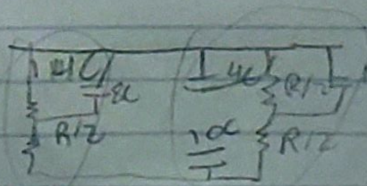
Worst case Rise: 16RC

worst case Fall: 15RC





Rise



Trise chain 1 → $R/2 \cdot 8C + R \cdot 10C = 14RC$ (4RC)

Trise chain 2 → $R/2 \cdot 12C + R \cdot 10C = 16RC$

$6RC + 10RC$