Mirror Adder – Lab Number 3

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Submission Date	:	9/27/2019

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ABSTRACT

CMOS devices are crucial in small circuits and the exercise performed included building a Mirror Adder circuit. The objectives were to see how sizing of the transistor widths affects output. This is with respect to timing and proper operation. Pyxis was sued for layout and Eldo was used to simulate the devices. Changing channel width changes the time that the signal is delayed through the circuit. Another important observation from the exercise is that the PMOS and NMOS transistors must have their Width to length ratios balanced according to the circuit layout or else it will not operate as desired. The output of the circuit is a 3-input adder with carryout and sum. At 125 degrees Celsius, the overall max input frequency for no output capacitance is 10.3Ghz, and the max throughput with no capacitance is 27.7Ghz. The overall max input frequency for 120fF output capacitance is 297Mhz, and the max throughput with 120fF capacitance is 640Mhz. With a 120fF load added, percent change is -97.22% for throughput frequency and -87.83% for input frequency. And when considering delays, the best sized transistor in this exercise was a PMOS with a W/L ratio of 8 and the NMOS structure associated with this PMOS structure had a ratio of 4W/L.

DESIGN METHODOLOGY

The exercise started with creating the circuit for the mirror adder in Pyxis. The transistor lengths were left at .13u but the widths had to be filled in accordingly. The circuit is shown in figure 1.

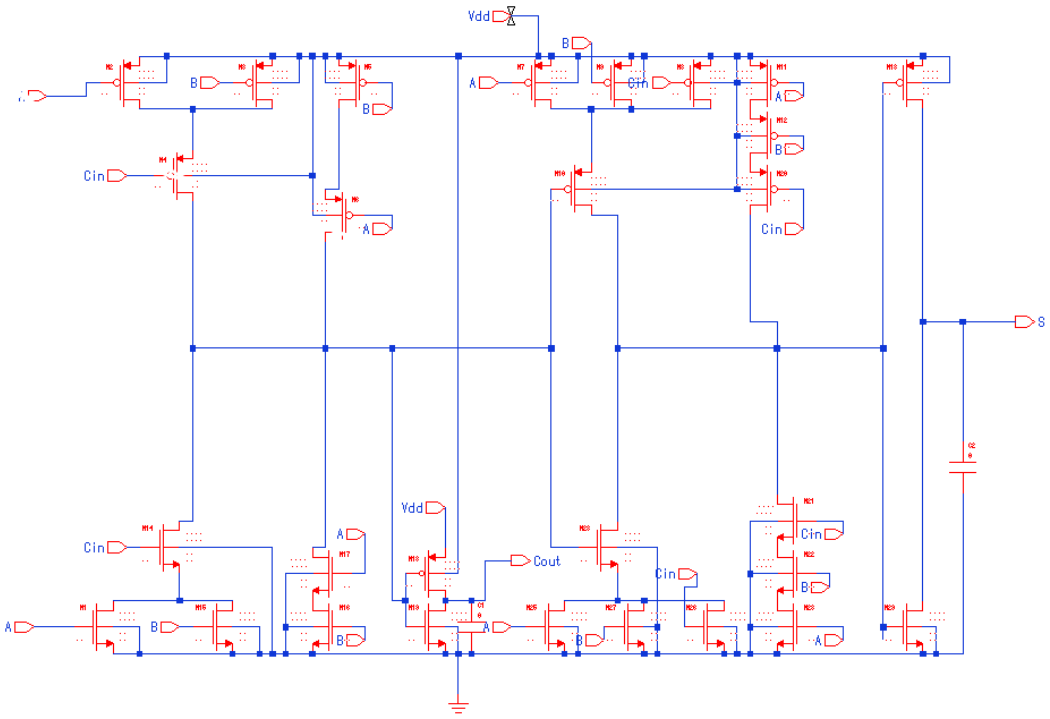

Fig. 1: Mirror Adder Transistor circuit made with Pyxis

The circuit is relatively simple and operates like a full adder. There are 3 inputs and 2 outputs. In this circuit the transistor widths had to be filled in. The rules for doing so are such that PMOS transistors have double the width of the NMOS. And transistors in series need to have their widths incremented to be able to drive through the series. Parallel transistors are unaffected, but they still need to balance out the opposite branch. In general, smaller is better and this is shown in the results. Figure 2 contains the labelled transistor widths where the number next to the transistor is the width divided by lambda which is .13uM.

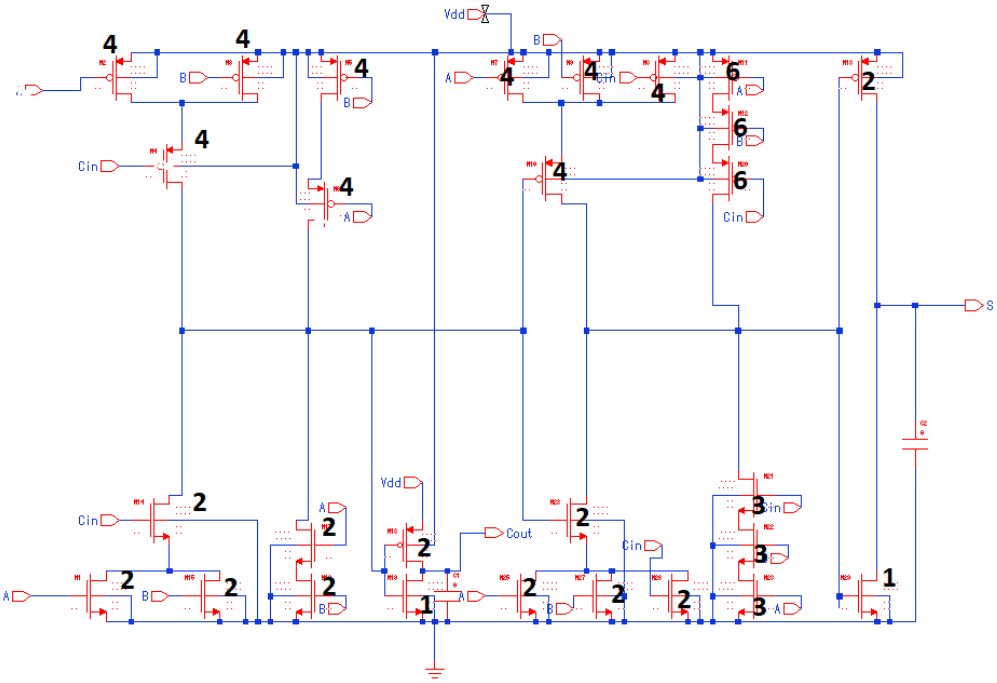

Fig. 2: Mirror Adder Transistor circuit made with Pyxis Containing Labeled Width Ratios

There are load capacitors that are used in this circuit as well. It is a 120fF capacitor tied to each output. The evaluation of critical path is important, and it is done by looking at the Elmore model delay. This formula is one that will come up with a time constant for any branch of the circuit. It is used to determine the longest time path after inspection fails to be useful. To calculate Elmore delay use equation 1 which is sourced from lectures. The largest RC multiple is the critical path, or path that will take the most time. This is the method used to identify the critical path.

$$t_{delay} = \sum_{i=0}^{Num\ Nodes} R_{i-to-source} C_i$$

Eq. 1: Elmore Delay of a Circuit

Figure 3 shows the evaluated paths and the time constants associated with them using the Elmore delay model. The values are overlaid on each path. Some paths can be immediately discounted because they will be fast. A PMOS and NMOS pair with ratio 2 to 1 will be faster than the same components with 2 PMOS in parallel. The sum of capacitances will slow down operation, especially as the width grows.

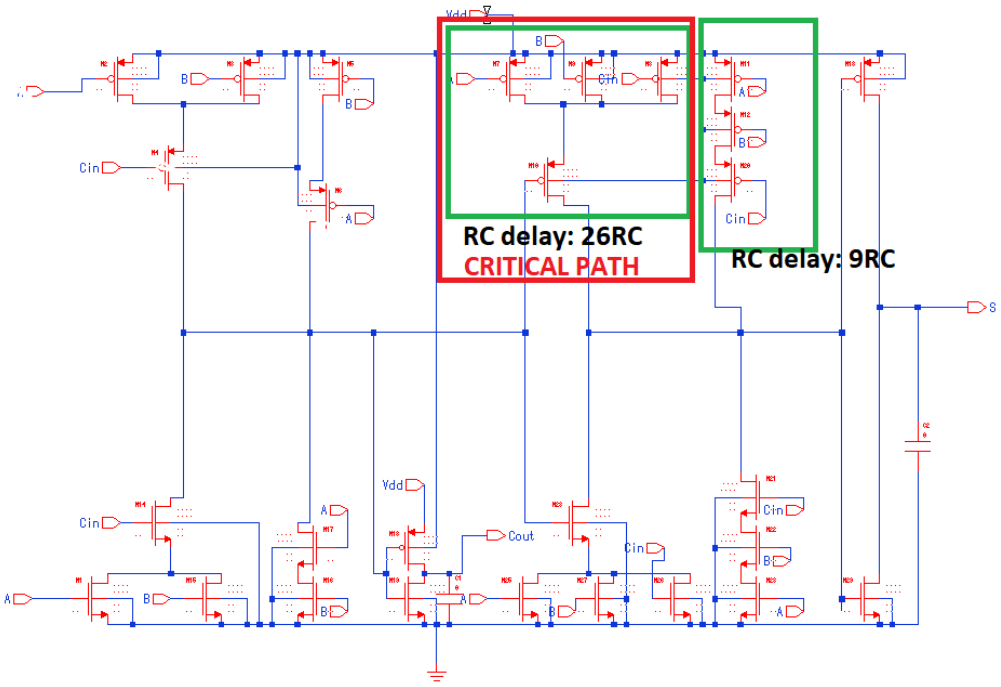

Fig. 3: Mirror Adder Timing Delay Calculations with Elmore Model

The critical path is the 3 parallel PMOS in series with another PMOS. The combined capacitances blow the 3 series PMOS out of the water with more than double the delay. To summarize, minimize delays by picking transistors that provide the smallest Elmore delay at the critical paths. This is the approach that was used to determine the best transistor sizes for fastest operation.

Additionally, to calculate input and throughput frequencies equation 2 and 3 are used.

$$F\ In\ Max = \frac{1}{rise\ time + fall\ time}$$

Equation 2. F Input Max calculation

$$F\ \text{througput MAx} = \frac{1}{Tp,HL + Tp,LH}$$

Equation 3. F throughput max calculation

These will be important metrics for digital circuits that are part of a larger system. These will be calculated for various trials of this circuit under different conditions.

RESULTS & ANALYSIS

This procedure consisted of several steps. The metric portions of the circuit that were examined are the rise, fall and delay times. This was used to calculated throughput and input frequencies. The conditions for these were similar as well. The circuit was analyzed under worse case parameters and with and without a 120fF load at each

output terminal. The VDD voltage was 1.08V and the temperature was 125 degrees Celsius for each trial. The simulation profile for this circuit was pretty standard. The input waves were pulse waves that had rise times of .1ns. For A, B and C the periods were 20ns, 40ns, and 80ns respectively. This is all that was needed to capture simulated output on S and Cout terminals for the circuit. Figure 4 shows the simulated circuit results with no load at 1.08V VDD and 125 degrees Celsius.

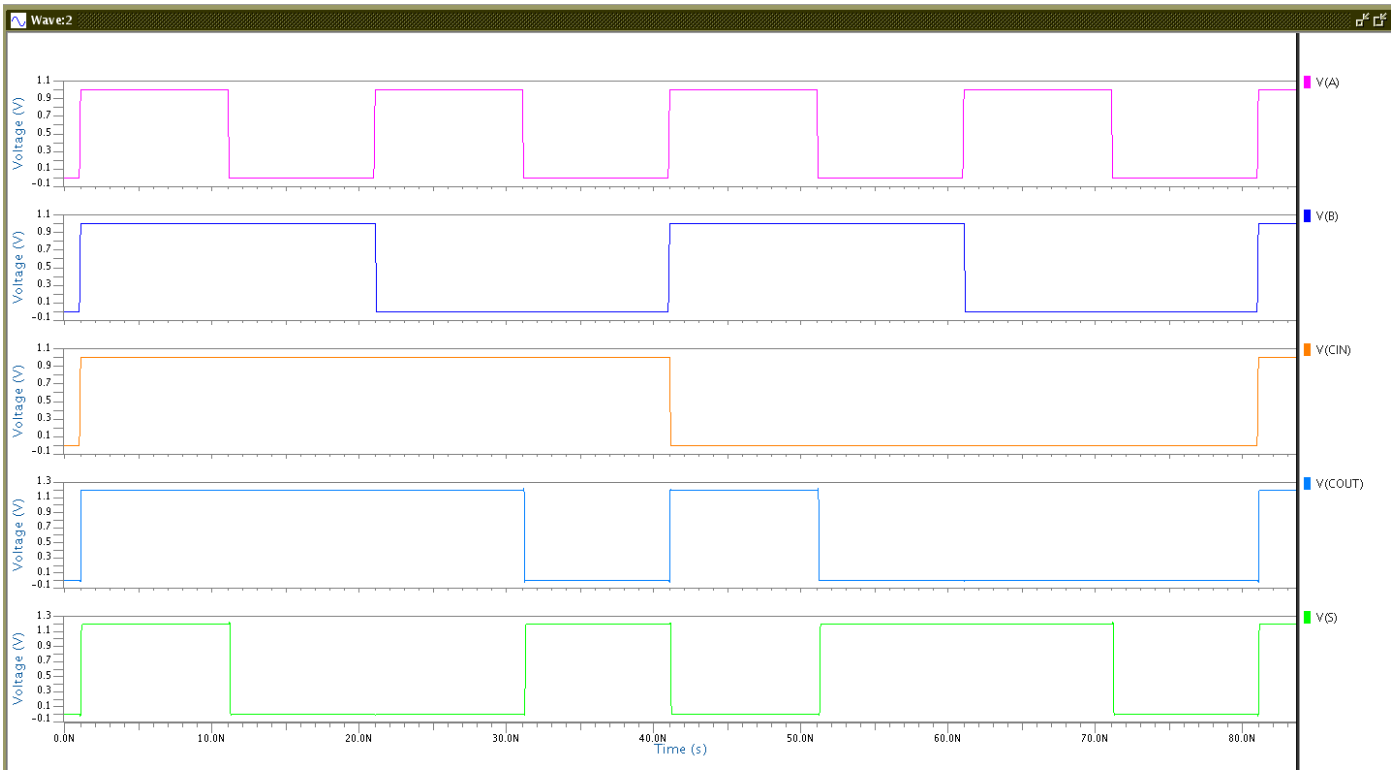

Fig. 4: Plotted Mirror Adder Signal Voltages with Pulsed Transient Analysis with profile (T = 125 degrees C, 1.08V on VDD, C=0F)

Upon inspecting the figure, the adder behavior works. When no signals are high, no output is high. When all signals are high, all output is high. And for every combination of inputs the corresponding carry out and sum are appropriate. Another way to verify operation is to treat this circuit as a digital one. Since the adder circuit is meant to operate as a digital circuit, busses can be created for input and output. This is shown in figure 5.

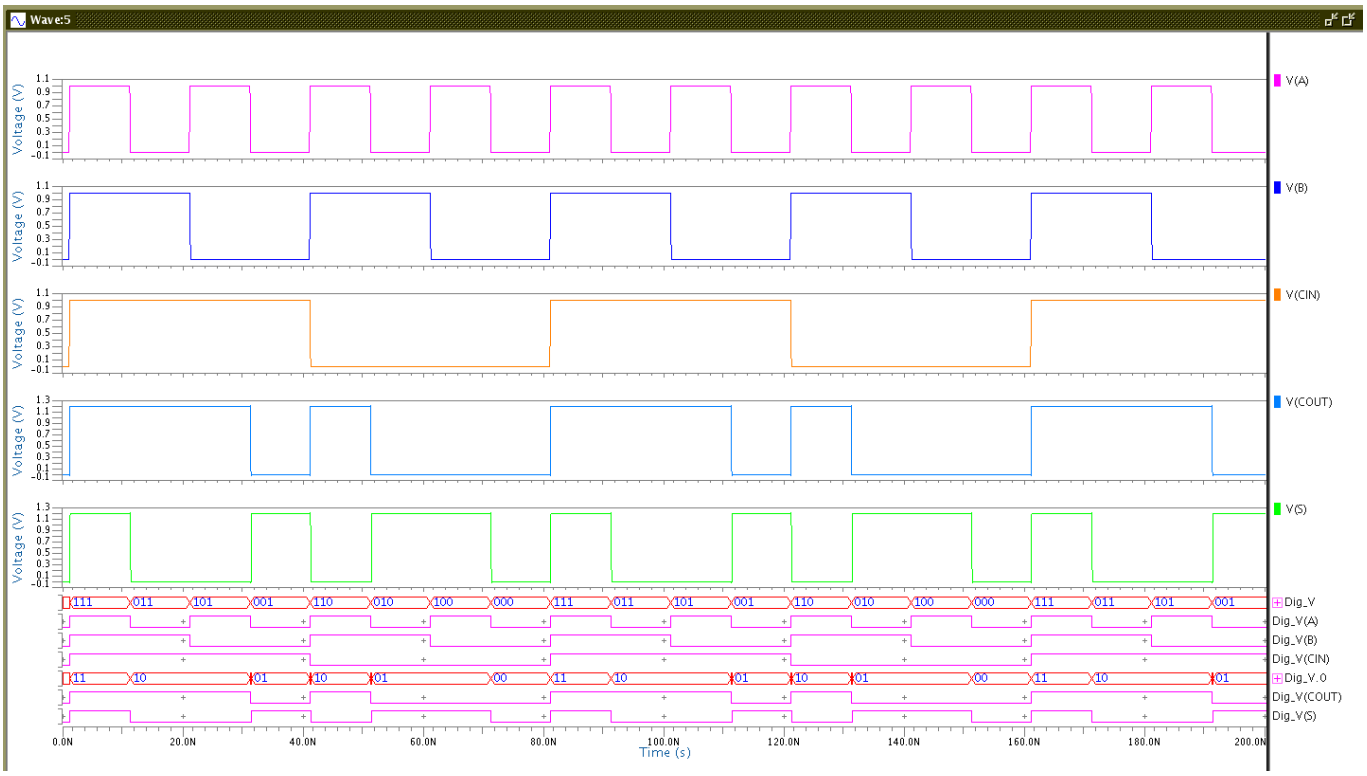

Fig. 5: Plotted Mirror Adder Signal Voltages with Pulsed Transient Analysis with Binary Buses and Digital Signals with profile (T = 125 degrees C, 1.08V on VDD, C=0F)

In figure 5 the binary representation of the input and output signals is clearly shown. This is a great way to analyze the behavior of digital circuits. The circuit was also simulated with 120fF capacitors at the output terminals and this simulation wave form is shown in figure 6.

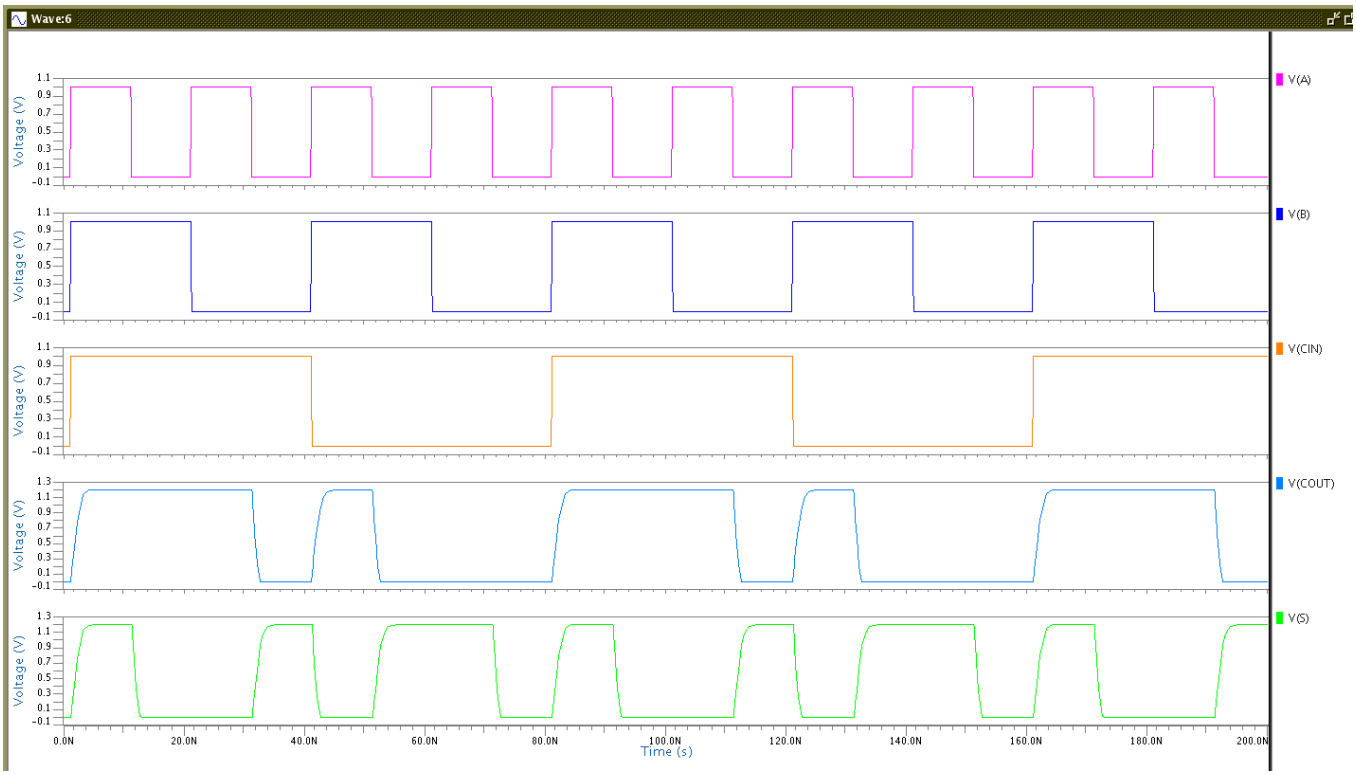

Fig. 6: Plotted Mirror Adder Signal Voltages with Pulsed Transient Analysis with Binary Buses and Digital Signals with profile (T = 125 degrees C, 1.08V on VDD, C=120F)

It is apparent that the added output capacitance affects rise fall and delay times in the circuit.

The next important set of results is the timing analysis of the mirror adder. The circuit is timed at the carry out and sum out portions and with and without loads. Figure 7 shows the labeled rise fall and delay times for outputs of the mirror adder.

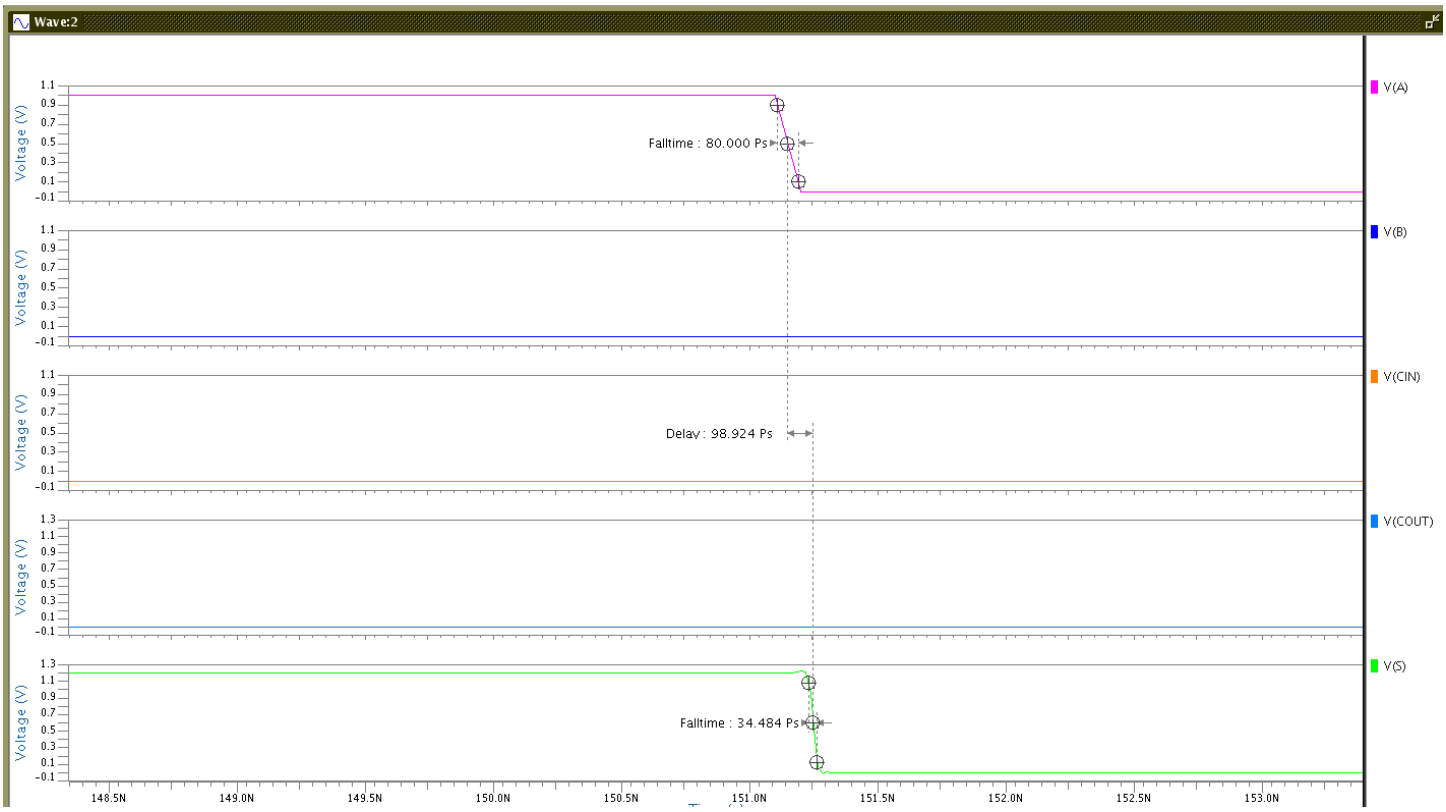

Fig. 7: Plotted Mirror Adder Signal Voltages with Measure Fall and Delay with profile (T = 125 degrees C, 1.08V on VDD, C=0F)

This form of measurement can be used to fill out result tables. Table 1 shows the timing results for the sum portion of the circuit after this process is repeated for all rise times, fall times, delays and profiles.

Table 1: Sum Output Results

	V_{DD} [V]	Temp [°C]	Load Capacitance [fF]	Rise Time [S]	Fall Time [S]	$T_{P,HL}$ [S]	$T_{P,LH}$ [S]	$F_{input,\ max}$ [Hz]	$F_{Throughput,\ Max}$ [Hz]
Worst Case	1.08	125	4.27E-11	3.45E-11	9.89E-11	8.25E-11	1.29514E+10	1.29514E+10	5.51213E+09
Worst Case	1.08	125	1.76E-09	1.02E-09	5.97E-10	8.93E-10	3.59415E+08	3.59415E+08	6.70988E+08

The results here are straightforward. The output of the sum is more delayed when there is output capacitance and the throughput and input frequencies are lowered due to this capacitance.

Table 2 shows the timing results for the carry portion of the circuit.

Table 2: Carry Output Results

	V_{DD} [V]	Temp [°C]	Load Capacitance [fF]	Rise Time [S]	Fall Time [S]	$T_{P,HL}$ [S]	$T_{P,LH}$ [S]	$F_{input,\ max}$ [Hz]	$F_{Throughput,\ Max}$ [Hz]
Worst Case	1.08	125.00	0.00	2.56E-11	2.76E-11	8.42E-11	6.21E-11	1.87977E+10	6.83466E+09
Worst Case	1.08	125.00	120.00	1.77E-09	9.87E-10	5.80E-10	8.52E-10	3.62911E+08	6.98027E+08

The results here are also straightforward. The output of the carry is more delayed when there is output capacitance and the throughput and input frequencies are lowered due to this capacitance. It is also clear that the path that contributes to Carry contains the critical path because when not obscured by the extra capacitor, this output performs much slower than the sum in rise and fall times. This idea leads to the completion of table 3, the circuits overall results for input and throughput frequencies.

Table 3: Overall Results

V_{DD} [V]	Temp [°C]	Load Capacitance [fF]	$F_{input, max}$ [Hz]	$F_{Throughput, Max}$ [Hz]
1.08	125	0	1.037E+10	2.771E+10
1.08	125	120	2.976E+08	6.404E+08

For this overall input and throughput frequency, the lowest ones had to be selected. This is to ensure no inputs move to fast for the slowest branch of the circuit to process and get output out in time. The overall max input frequency for no output capacitance is 10.3Ghz, and the max throughput with no capacitance is 27.7Ghz. The overall max input frequency for 120fF output capacitance is 297Mhz, and the max throughput with 120fF capacitance is 640Mhz.

An important metric to consider is the percent change in throughput and input from loaded to unloaded output signals. This uses a formula like percent error. This is shown in equation 4.

$$Percent\ Change = \frac{Old - New}{Old}$$

Equation 4. Percent Change Formula

Equation 4 was used to determine the percent change for Max throughput and input frequencies when a load is added of 120fF. With a 120fF load added, percent change is -97.22% for throughput frequency and -87.83% for input frequency.

The next portion of the exercise dealt with transistor sizing and circuit response. The widths were changed, and the delays were recorded for the new circuits. The purpose was to analyze how transistor width affects delay and choose the best size for the fastest circuit. Several trials were done with various widths to get an idea of how width affects delay. Table 4 shows the delays associated with different widths of transistors in the critical path highlighted in figure 3 for the Sum.

Table 4: Sum Width-Delay Output Results

PMOS W/L ratio	VDD (V)	TEMP (C)	LOAD (fF)	RiseTime	Fall Time s	TP,HLs S	TP,LHs S
8	1.08	125	0	4.27E-11	3.45E-11	9.89E-11	8.25E-11
10	1.08	125	0	1.59E-09	1.02E-09	5.97E-10	8.93E-10
12	1.08	125	0	1.76E-09	1.02E-09	1.37E-10	8.93E-10

From table 4, wider transistors negatively affect time results. This is likely because more capacitance is added. Table 5 shows the delays associated with different widths of transistors in the critical path highlighted in figure 3 for the Carry.

Table 5: Carry Width-Delay Output Results

PMOS W/L ratio	VDD (V)	TEMP (C)	LOAD (fF)	RiseTime	Fall Time s	TP,HLs S	TP,LHs S
8	1.08	125	0	2.56E-11	2.76E-11	8.42E-11	6.21E-11
10	1.08	125	0	1.77E-09	1.01E-09	5.80E-10	8.52E-10
12	1.08	125	0	1.77E-09	1.01E-09	5.80E-10	8.52E-10

Table 5 shows that the delay is also negatively affected by larger transistors. This relationship is plotted in figure 8 for the sum. On the plot are the high to low and low to high delays.

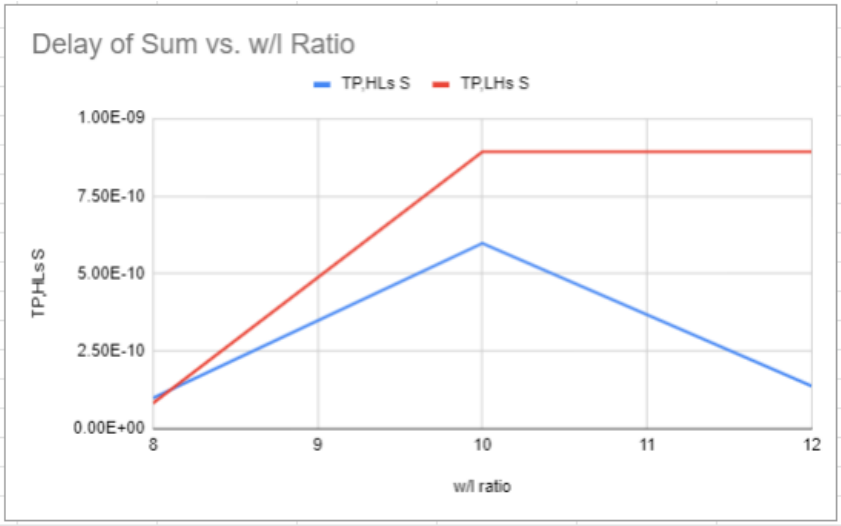

Fig. 8: Delay vs W/L Ratio for Sum

The delay increases for the most part with larger transistors. Figure 9 shows the delays HL and LH for carry.

Fig. 9: Delay vs W/L Ratio for Carry

The delay increases for the most part with larger transistors. The delay tends to get worse and worse for each as the transistors get larger and larger. That is why the best delay is obtained by using the smallest circuits with the smallest widths. The capacitances really add up. So, the best sized transistor in this exercise was a PMOS with a W/L ratio of 8 and the NMOS structure associated with this PMOS structure had a ratio of 4W/L.

CONCLUSIONS

This exercise was a success. CMOS devices are crucial in small circuits and the exercise performed included building a Mirror Adder circuit. The objectives were to see how sizing of the transistor widths affects output. This is with respect to timing and proper operation. Another important observation from the exercise is that the PMOS and NMOS transistors must have their Width to length ratios balanced according to the circuit layout or else it will not operate as desired. At 125 degrees Celsius, the overall max input frequency for no output capacitance is 10.3Ghz, and the max throughput with no capacitance is 27.7Ghz. The overall max input frequency for 120fF output capacitance is 297Mhz, and the max throughput with 120fF capacitance is 640Mhz. With a 120fF load added, percent change is -97.22% for throughput frequency and -87.83% for input frequency. And when considering delays, the best sized transistor in this exercise was a PMOS with a W/L ratio of 8 and the NMOS structure associated with this PMOS structure had a ratio of 4W/L.