Lab 4 Sign Off Sheet

CMPE 530/630 Digital IC Design
Lab 4. Layout of CMOS Logic Gates

Student's Name: Brin Landy Section (circle one): Wednesday / Fri

In Lab Performance	Point Value	Points Earned	TA/Instructor Sign
Stick diagram of CMOS inverter	10	10	
Good LVS report (smiley face) and good DRC	20	20	
PEX timing results (tables 3 and 4 in lab writeup)	10	10	

Report		Point Value	Points Earned	
Abstract		5		
Design Discussions		10		
Results and Analysis	Data table, waveforms	15		
	Analysis & explanation	15		
Conclusion		5		