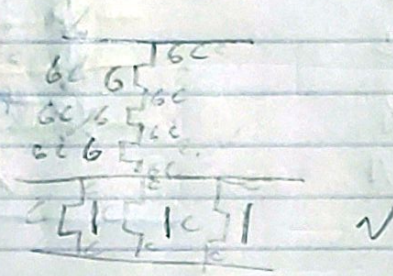
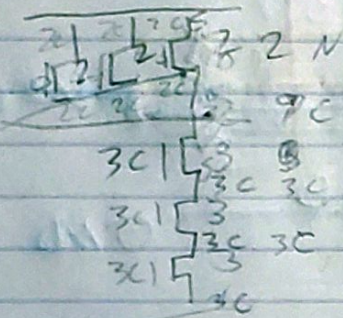
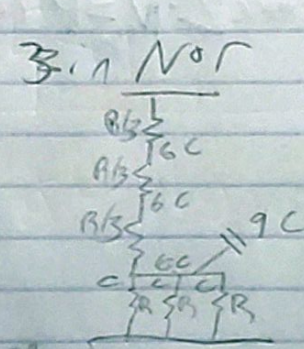
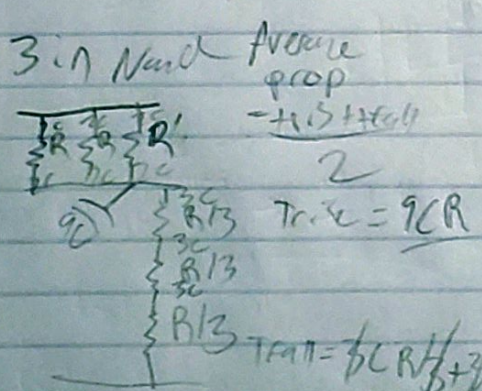


$\frac{S}{L_0}$   $\frac{L_1}{L_0}$

2) which has worse parasitic capacitance N-in NAND or N-NOR?  
 Evaluate delays and compare. Assume diff. capacitance for  
 N-input NAND N-input NOR



Diffusion sharing happens when S + d touches



$N=3$

$$T_{rise} = \frac{R}{3} C_{in} + \frac{2R}{3} C_{out} + R C_{out}$$

$$= 2RC + 4RC + 6RC$$

$$= 12RC$$

$$T_{pd} = \frac{(9+6)RC}{2} = 7.5RC$$

NAND

$$T_{pd} = \frac{9CR + 12RC}{2} = \frac{21RC}{2}$$

NOR

Worse N-input parasitic delays come from NOR