Design of CMOS Logic Gates – Lab Number 2

Author	:	Brian Landy
Lab Instructor	:	Abhishek Vashist
TA	:	Andrew Fountain
TA	:	Sabrina Ly
Lab Section	:	Lab #2
Submission Date	:	9/12/19

Table of Contents

ABSTRACT

CMOS device simulation is a valuable tool in digital design. Pyxis Layout, by Mentor Graphics, is a tool that allows for the creation of circuits to a level as specific as transistors. The procedure of exercise 2 was to use this tool to construct a transistor circuit and an inverter circuit with transistors and then use an analog simulation tool called Eldo to simulate the voltage and current characteristics of each. These tools accurately model CMOS devices and allowed for the estimation of the maximum input and throughput frequencies at different voltages, temperatures and capacitive loads. A CMOS modeled with Eldo had a Maximum input frequency of 10.37 Gigahertz and a maximum throughput frequency of 27.71 Gigahertz with no capacitive load. When accounting for a 120 femtofarad load, the inverters maximum input frequency was 297 Megahertz and its maximum throughput was 640.40 Megahertz.

DESIGN METHODOLOGY

The exercise started with creating a Pyxis schematic with a simple NMOS circuit in it. There is no capacitor attached. Figure 1 shows the circuit that was built for simulation.

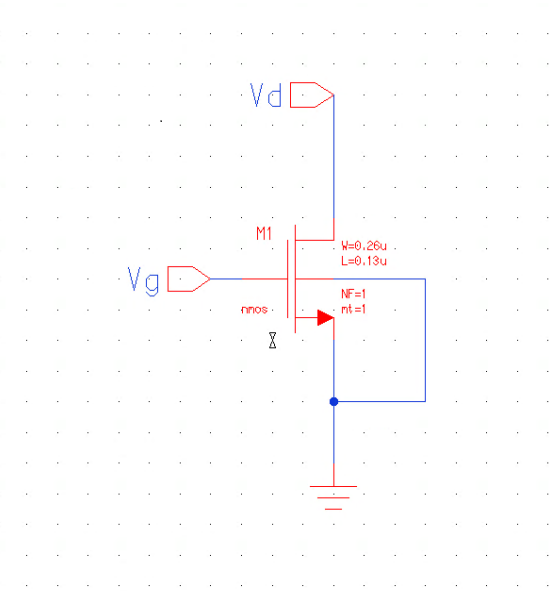


Fig. 1: Transistor circuit made with Pyxis

The circuit has a gate input voltage and a drain input voltage. The source and bias terminals are both tied to ground. The transistor is an NMOS and the desired width is .26u meters and the length is .13u meters. This circuit was simulated with voltage sweeps across Vg and Vd. The expected NMOS characteristics are shown in equation 1.

$$ID = \begin{cases} 0, & Cutoff \\ \frac{\mu_n \varepsilon_{ox} * W}{T_{ox} * L}\left(Vgs - Vt - \frac{Vds}{2}\right)Vds, & Linear \\ \frac{\mu_n \varepsilon_{ox} * W}{2 * T_{ox} * L}(Vgs - Vt)^2, & Saturation \end{cases}$$

Equation 1. NMOS Transistor IV characteristics

CMOS transistor devices have 3 modes of operation. They can be in cutoff where no current flows, the linear region where current flowing is directly related to a voltage difference or they can be in saturation mode. These modes depend on voltage differentials between the drain and the gate. Saturation mode is when the device has maximum current flow. This is a desired state in digital design because it represents a logical 1. The results of simulation are shown in the Results and Analysis section of this exercise.

The next circuit used in the exercise was a CMOS inverter. This circuit consists of an NMOS and a PMOS. There is an input and an output node in this circuit. Figure 2 shows the inverter circuit.

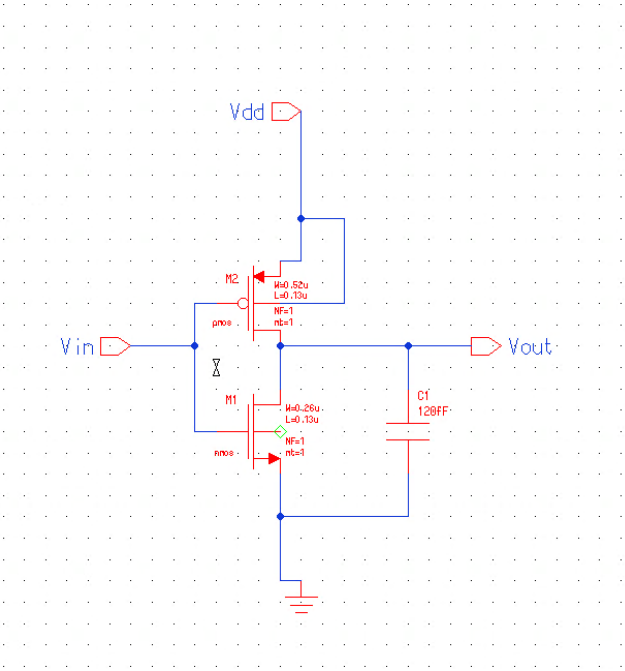


Fig. 2: CMOS Transistor Inverter Circuit

The circuit has a capacitive load of 0 or 120 femtofarads depending on the simulation profile. This capacitance is from the output to the source of the NMOS. The NMOS specifications include a width of .26u meters and a length of .13u meters. To have an equivalently powerful PMOS, the width and length must be different. The ratio must be a double of the NMOS. So, the width is 52u meters and the length is 13u meters. Different simulation profiles were applied to this circuit to measure its response. These results are shown in the results and analysis section as well.

RESULTS & ANALYSIS

The procedure consisted of simulating 2 circuits. The first was a simple NMOS transistor with a .26u meter width and a .13u meter length. Simulation took place with the Eldo tool. The simulation setup included setting the maximum magnitude for the gate voltage and drain voltage to 1.2 volts. The simulation was a sweep through these values with a Vd step of .01V and a Vg step of .3V. The temperature of the simulation was 25 degrees Celsius. The IV curve for the NMOS transistor is shown in figure 3.

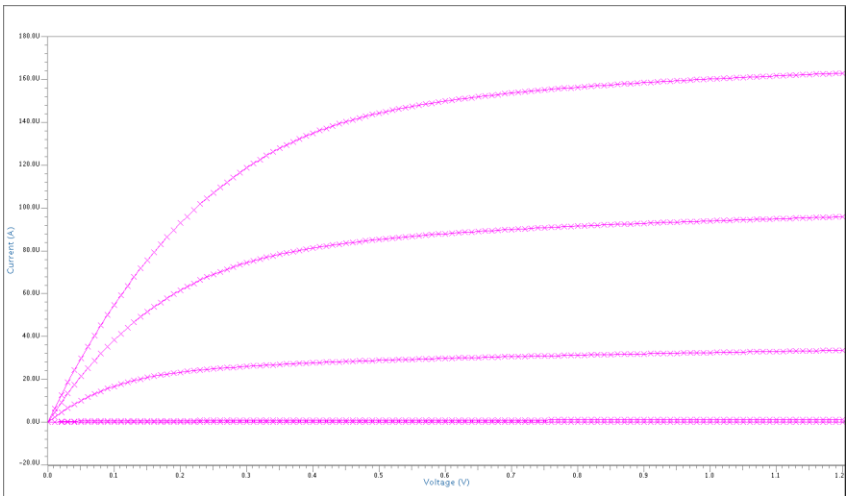


Fig. 3: Plotted NMOS transistor IV characteristics with profile(T = 25 degrees C, VD and VG swept from 0V to 1.2V)

The resulting simulation plot was as expected. It ended up being an extremely obvious characteristic curve associated with NMOS IV properties. The 3 regions are visible, cut off(I=0), linear(I=linear scale), and saturation (I=maximum, levels off). The next portion of the exercise was to take the NMOS circuit and add in a PMOS transistor to create a CMOS Inverter and simulate it.

The CMOS inverter to simulate is shown in figure 2. The circuit was simulated under the same conditions (25 degrees Celsius, 0 to1.2V input sweep). The length and width of the NMOS are still the same but the PMOS length is .13u meters and the width is .52 u meters. The width needs to be double for PMOS to equate to an NMOS of a certain size. Eldo was used again to simulate this. The plot of Vin is also on there. It is a single straight line with voltage swept from 0 to 1.2V. The voltage characteristic curve for this device is shown in figure 4.

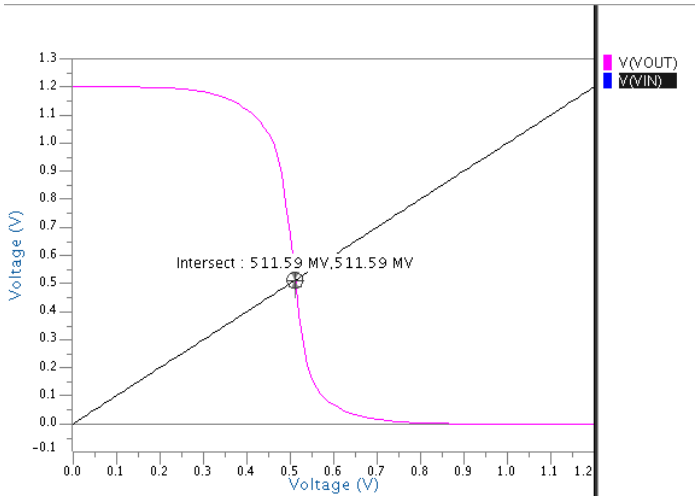


Fig. 4: Plotted CMOS Inverter characteristics with profile (T = 25 degrees C, DC signal on Vin swept from 0V to 1.2V and Vdd held constant at 1.2V)

There is an intersection point on the graph of Vout and Vin in figure 4. This is the interchange point where the CMOS device input and output voltages are identical. This is called the midpoint voltage and it should be in the middle of the logical 0 and 1 or the device will not be as resistant to noisy signals. This is an extremely important concept in digital design. A bad midpoint voltage could be due to poor channel length and width coordination. Figure 5 shows the midpoint voltage plot for a circuit with an unbalanced NMOS and PMOS. The PMOS width is .6uM, then length is .13uM. The NMOS width is .2uM and the length is .13uM.

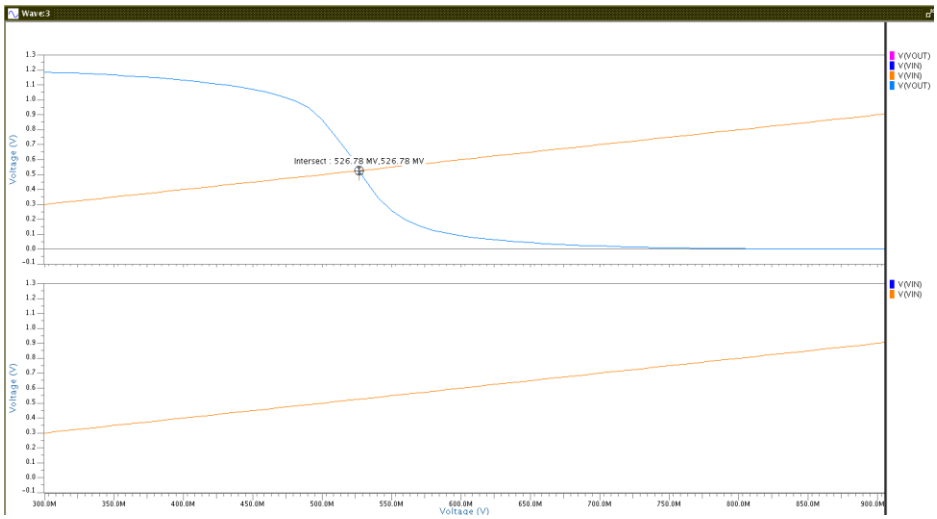


Fig. 5: Plotted unbalanced CMOS Inverter in/out voltage characteristics with profile (T = 25 degrees C, DC signal on Vin swept from 0V to 1.2V and Vdd held constant at 1.2V)

If the NMOS is not balanced properly with the PMOS, the point where input and output voltage will shift. If it shifts too much in either direction, behavior will be incorrect, and the device will not work. Signal noise will completely ruin device operation.

The next portion of CMOS inverter simulation focused on transient analysis of the device. A 40ns transient analysis was performed where Vin was a pulsing input in the Eldo simulation. It was run at 25 degrees Celsius still. Figure 6 shows the output of this simulation.

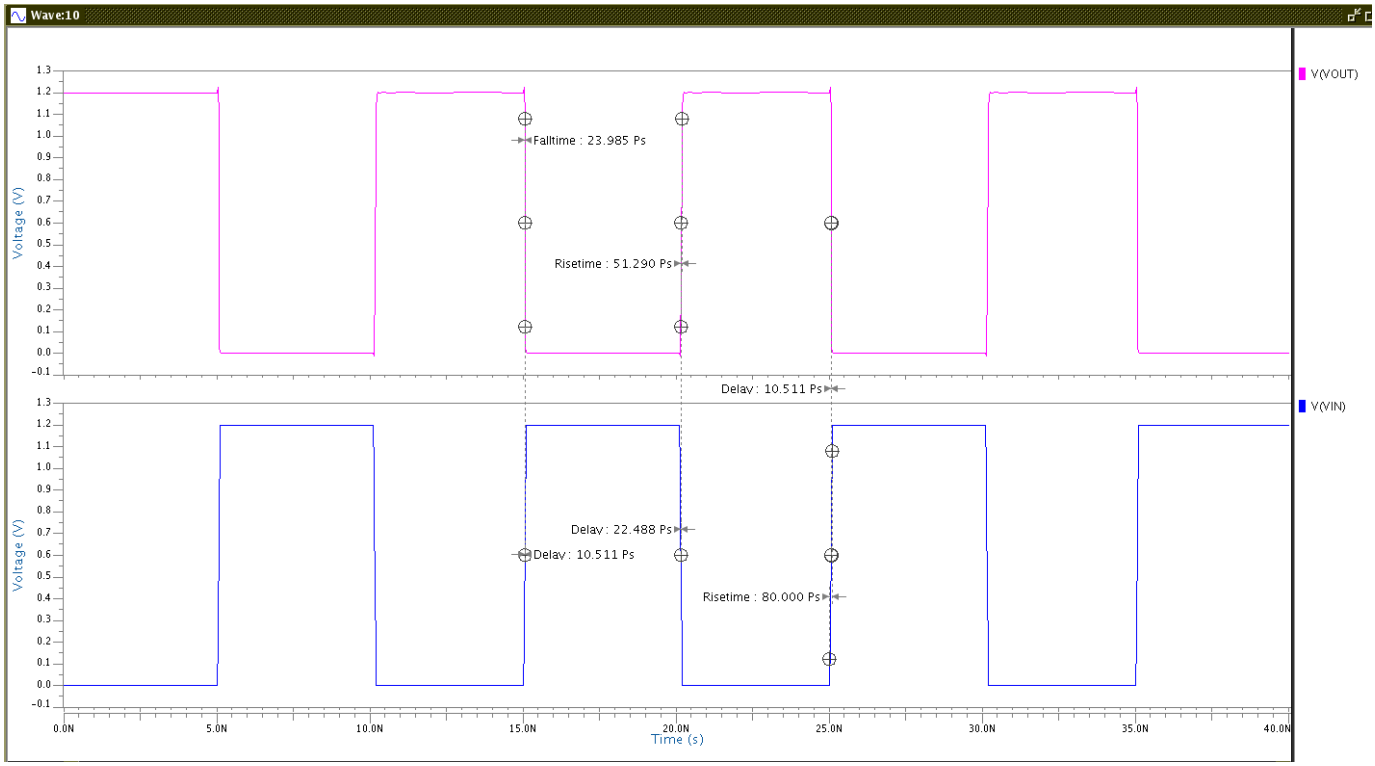


Fig. 6: Plotted CMOS Inverter Vin and Vout with 40ns transient analysis with profile (T = 25 degrees C, 1.2V Pulse on Vin swept)

Figure 6 contains 2 plots. They are the input voltage and the output voltage of the CMOS inverter. There are measurements on the plot that are required for 2 important characteristics. The 2 important device characteristics are device input frequency and device throughput frequency. To calculate input frequency, measure the fall and rise times of the input wave. To calculate throughput frequency, measure the delay of the wave input to output. A closeup of the rise and fall time can be seen in figure 7.

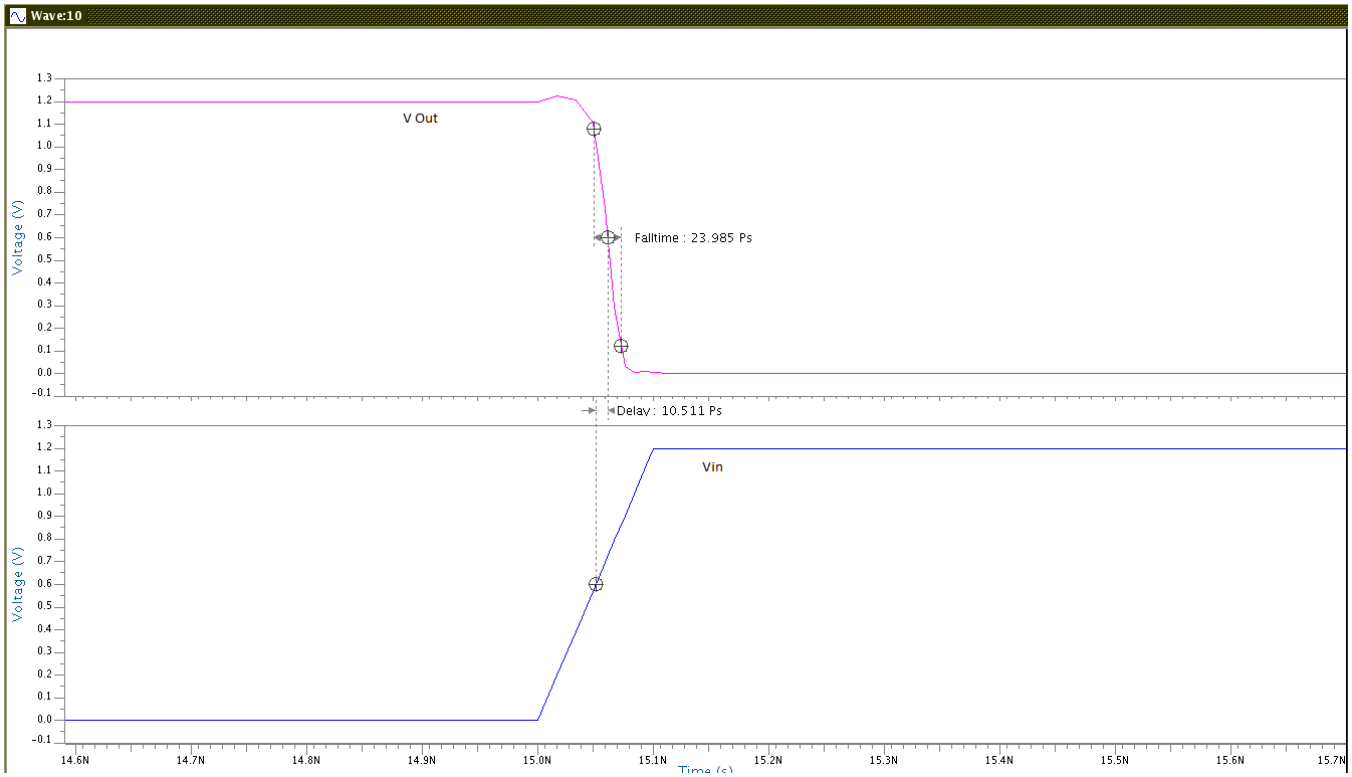


Fig. 7: Close up of Plotted CMOS Inverter Vin and Vout with 40ns transient analysis with profile (T = 25 degrees C, 1.2V Pulse on Vin swept)

From the figure input and output are not exactly one to one in terms of response. This is due to transistor characteristics and capacitances. To further show the impact of capacitance on input and throughput frequencies, a capacitor that exists in figure 2 had its value altered. It was either 0 farads or 120fF. Several simulations were run with varying profiles for different values. The temperature was also changed between 25 degrees C and 125 degrees C to achieve a worst case. In addition, the value of VDD was changed from 1.2 to 1.08V for worst case. Also, the capacities load was changed to 120fF. Table 1 holds the profile and measured results of each simulation. They consist of best case no capacitance, best case with capacitance, worst case no capacitance and worst case with capacitance.

Table 1: Inverter Results

	V_{DD} [V]	Temp [°C]	Load Capacitance [fF]	Rise Time [S]	Fall Time [S]	$T_{P,HL}$ [S]	$T_{P,LH}$ [S]
Nominal	1.2	25	0	5.13E-11	2.40E-11	2.25E-11	1.05E-11
Nominal	1.2	25	120	1.74E-09	9.08E-10	4.65E-10	8.15E-10
Worst Case	1.08	125	0	5.39E-11	4.26E-11	2.33E-11	1.28E-11
Worst Case	1.08	125	120	2.04E-09	1.32E-09	9.58E-10	6.03E-10

From the table values it is possible to calculate input frequency and throughput frequency. This is done with equation 2 and 3.

$$F\ In\ Max = \frac{1}{rise\ time + fall\ time}$$

Equation 2. F Input Max calculation

$$F \text{ througput MAx} = \frac{1}{Tp,HL + Tp,LH}$$

Equation 3. F throughput max calculation

Equation 2 and 3 were used to calculate the frequencies. The resulting frequency values for these calculations with the worst-case scenario profiles are shown in table 2.

Table 2: Inverter Results

V_{DD} [V]	Temp [°C]	Load Capacitance [fF]	$F_{input, max}$ [Hz]	$F_{Throughput, Max}$ [Hz]
1.08	125	0	1.037E+10	2.771E+10
1.08	125	120	2.976E+08	6.404E+08

A CMOS Inverter modeled with Eldo had a Maximum input frequency of 10.37 Gigahertz and a maximum throughput frequency of 27.71 Gigahertz with no capacitive load. When accounting for a 120 femtofarad load, the inverters maximum input frequency was 297 Megahertz and its maximum throughput was 640.40 Megahertz.

CONCLUSIONS

The procedure successfully demonstrated CMOS logic gate concepts. The procedure of exercise 2 was to use Pyxis simulation tools to construct a transistor-based circuits and use an analog simulation tool called Eldo to simulate the voltage and current characteristics of each. These tools both successfully were used to create the circuits and plot their characteristics. It revealed the IV characteristics as expected for the NMOS transistor and was useful in determining the rise and fall times of the circuits. It was also great for finding the time from High to Low in the circuits. With these values, the max input frequency and max throughput frequency were able to be determined. A CMOS Inverter modeled with Eldo had a Maximum input frequency of 10.37 Gigahertz and a maximum throughput frequency of 27.71 Gigahertz with no capacitive load. When accounting for a 120 femtofarad load, the inverters maximum input frequency was 297 Megahertz and its maximum throughput was 640.40 Megahertz. The lower frequency is due to the capacitor slowing down the operation of the device. It requires a certain amount of charge, so the device is slowed down as the capacitor charges first.

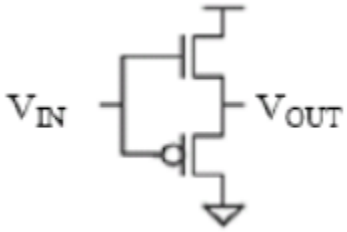
QUESTIONS

1. What are the regions of operation for an inverter? Describe the mode of operation for each transistor for the regions. Use the VTC curve that you created as part the exercise.

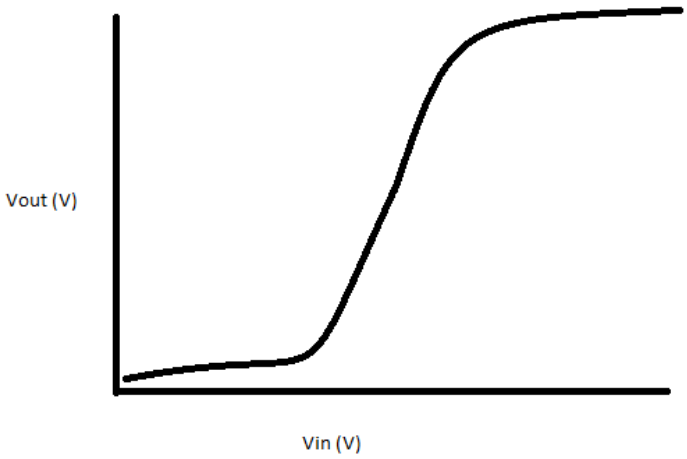
   There are many modes of operation for a transistor. A transistor is a CMOS device with an NMOS and a PMOS. Each MOS device has 3 modes (Cutoff, linear, and saturation). The plot in figure 3 (VTC curve) can be shown to overlay a corresponding IV chart for PMOS transistors and the resulting plot will look exactly like figure 4. In there, there are 5 modes for the transistor. The modes are as follows: NMOS

cutoff and PMOS linear, NMOS saturated and PMOS linear, NMOS saturated and PMOS saturated, NMOS linear and PMOS saturated, NMOS linear and PMOS cutoff.

2. Draw the waveform that would result from a DC sweep of the input of the following circuit. Explain the behavior.



The behavior of this circuit would look like this:



When Vin is low, the output voltage would be low as well because the device is not in saturation mode when there is a logic 1 now and then when Vin is high, the output voltage would be high. It would not invert anymore.

3. What are the theoretical rise/fall times for the inverter with a 120 fF load? How do these compare with your results? If there is a discrepancy, what would cause it?
   The theoretical rise and fall times that were calculated for this circuit are done so with the idea that the circuit has a time constant of 6*R*C. And so, to calculate rise/fall it is T=ln(2)*6*R*C. The ln(2) comes from the reduction

   Assume internal resistance is at .1 ohm for 25 degrees Celsius (Keim plot 2)

   Rise: So the rise time is 4.99*10^-11
   Fall: And the fall time is also 4.99*10^-11

   The rise time is similar, but the fall time is off from the expected fall time. Discrepancies occur from too many calculation assumption made.

4. Estimate channel length modulation parameter for the NMOS devices based on the NMOS IV characteristics.
   To estimate CLM, find the Voltage VA where a line extrapolated from the saturation region meets the X axis. Then the CLM param is 1/VA. I calculated that the line fit by the saturation curve decreases by .000017Amps per 1.2 volts. So with some simple math, the point where this line will meet the X axis is at -9.8235. So the CLM param **lambda is.10119**

EXTERNAL SOURCES CITED

Keim, Robert. "Understanding MOSFET On-State Drain-to-Source Resistance." *All About Circuits*, 2 Sept. 2016, https://www.allaboutcircuits.com/technical-articles/understanding-mosfet-on-state-drain-to-source-resistance/.