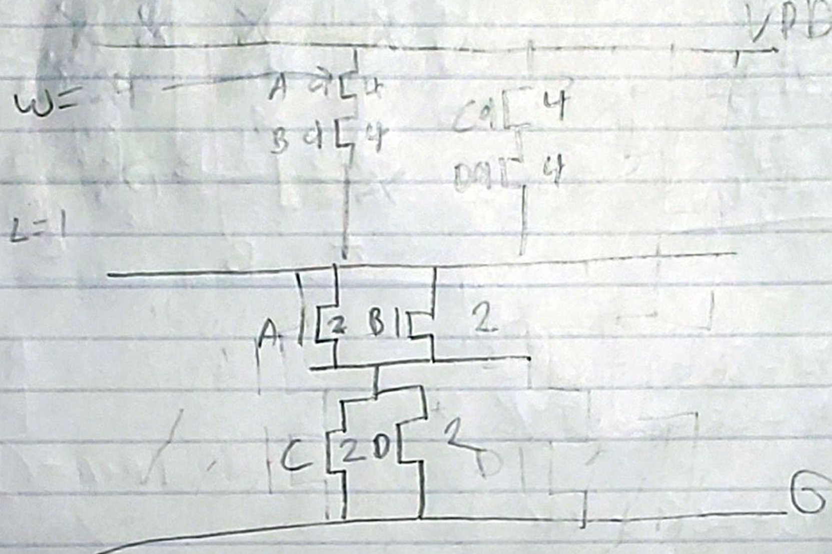
Brian Landy Digital IC design HW4

1) Rising and falling propogation delay of wrogard gate that implements ((A+B) ∩ (C+D)) 1iF

Do with RC delay + Elmore delay

0 iF



fall

Tfall1 = R/2·10C + R 10C

Tfall2 = R/2·10C + R 10C

5RC + 10RC

(A+B) ∩ (C+D) → 1   0 iF (A+B) ∩ (C+D) → 0

~~(A∩B)+(C∩D)~~

↳ So (A+B) ∩ (C+D) spulldown

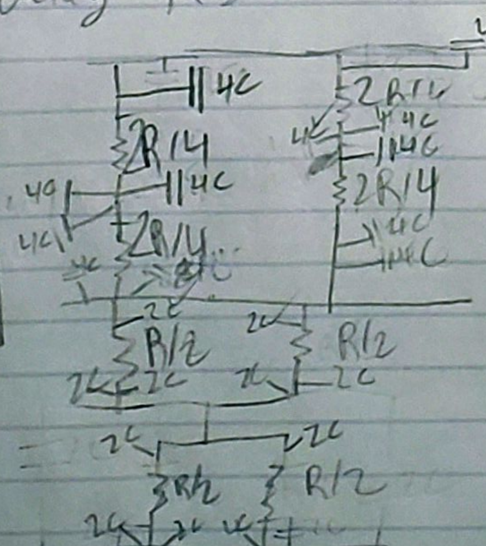
RCD

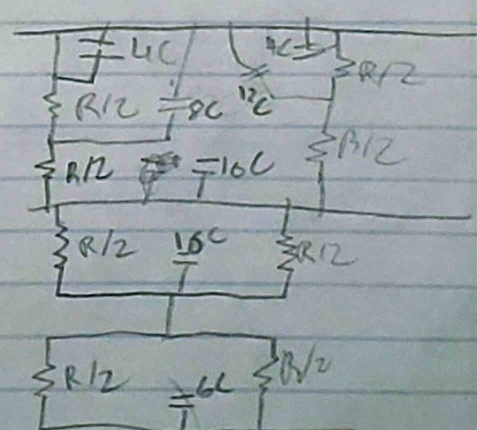
R+C delay rise + Fall

Electricallyisolatedtransgs

Worst case Rise: 16RC

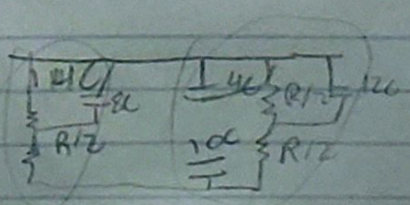
worst case fall: 15RC





Rise

Trise

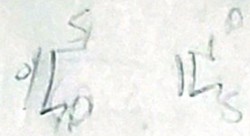


Rise

Trisechain 1 → R/2·8C + R·10C = 14RC (4RC)

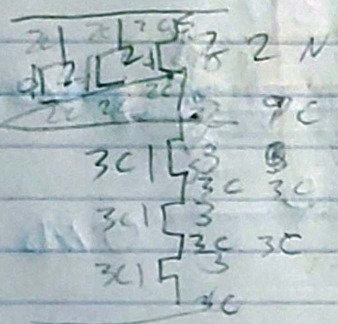
Trisechain 2 → R/2·12C + R·10C = 16RC

6RC + 10RC

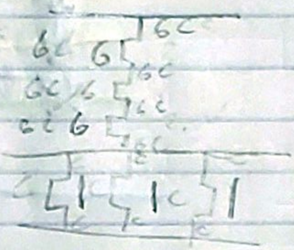


2) Which has worse parasitic capacitance N-in Nand or N-in NOR?
Evaluate 2 delays and compare. Assume diffusion sharing

N input Nand

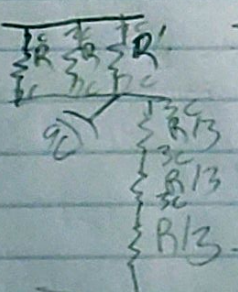


N input Nor



Diffusion sharing happens when S + d touch

3 in Nand



Average prop $= \frac{t_{rise} + t_{fall}}{2}$

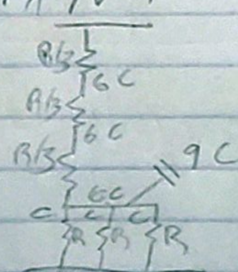
$T_{rise} = 9CR$

$T_{fall} = 3C\frac{R}{3} + 3C\frac{2R}{3} + 3CR$

$= RC + 2RC + 3RC = 6RC$

$T_{pd} = \frac{(9+6)RC}{2} = \frac{15RC}{2}$ Nand

3 in Nor



N=3

$T_{rise} = \frac{R}{3}6C + \frac{2R}{3}6C + R6C$

$= 2RC + 4RC + 6RC$

$= 12RC$

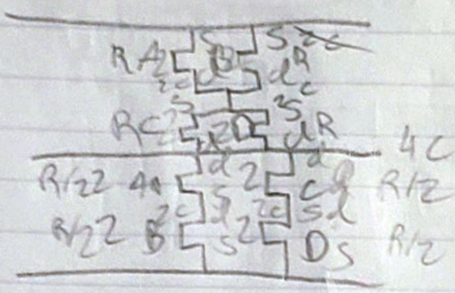
$T_{fall} = 9CR$

$T_{pd} = \frac{9CR + 12RC}{2} = \frac{21RC}{2}$ NOR

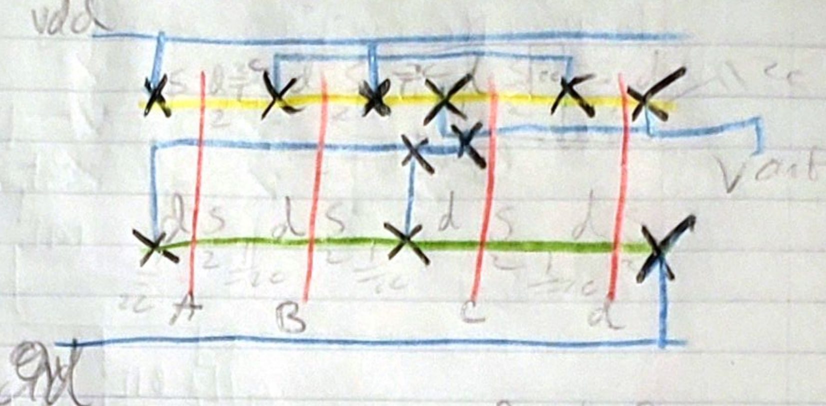
Worse N-input parasitic delay comes from NOR

Metal P
Poly N

3) Draw stick diagram of $\overline{(AB+CD)}$, size trans so rise + fall are same as inverter. Eval logic effort, assume diffusion sharing



diff share → flip S+D



$T_{rise1} = R4C + 2R4C = 12RC$
$T_{rise2} = R4C + 2R4C = 12RC$

$T_{fall1} = 4CR/2 + 2CR = 4RC$
$T_{fall2} = 4CR/2 + 2CR = 4RC$

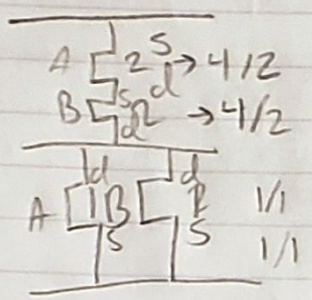
$R = 12RC$
$F = 4RC$

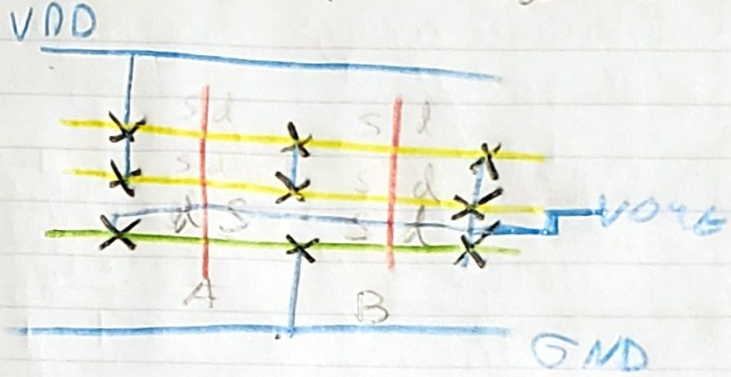
$T_{prop} = \frac{(R+F)}{2}$

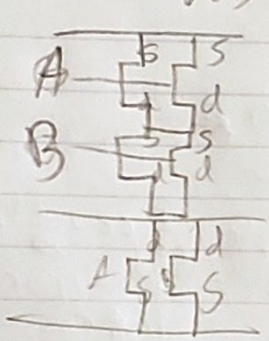
$\boxed{T_{prop} = 8RC}$

$\overline{(A+B)}$

4) stick diagram 2 input NOR, PW = 2 NW







↙ folded

can type one $2 \cdot N_{on} = P_{on}$