Design of CMOS Logic Gates – Lab Number 2

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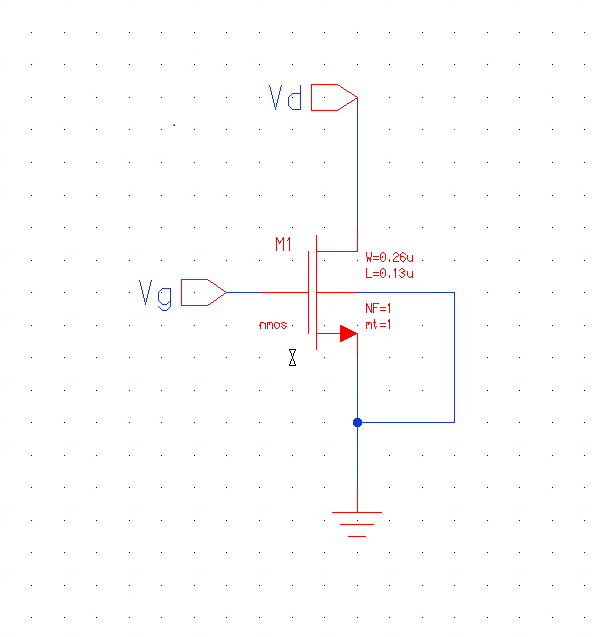
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# ABSTRACT

CMOS Logic Gate simulation is a valuable tool in digital design. Pyxis Layout, by Mentor Graphics, is a tool that allows for the creation of circuits to a level as specific as transistors. The procedure of exercise 2 was to use this tool to construct a transistor circuit and an inverter circuit with transistors and then use an analog simulation tool called Eldo to simulate the voltage and current characteristics of each. These tools accurately model CMOS devices and allowed for the estimation of the maximum input and throughput frequencies at different voltages, temperatures and capacitive loads. A CMOS modeled with Eldo had a Maximum input frequency of 10.37 Gigahertz and a maximum throughput frequency of 27.71 Gigahertz with no capacitive load. When accounting for a 120 femtofarad load, the inverters maximum input frequency was 297 Megahertz and its maximum throughput was 640.40 Megahertz.

# DESIGN METHODOLOGY

The exercise started with creating a Pyxis schematic with a simple NMOS circuit in it. There is no capacitor attached. Figure 1 shows the circuit that was built for simulation.



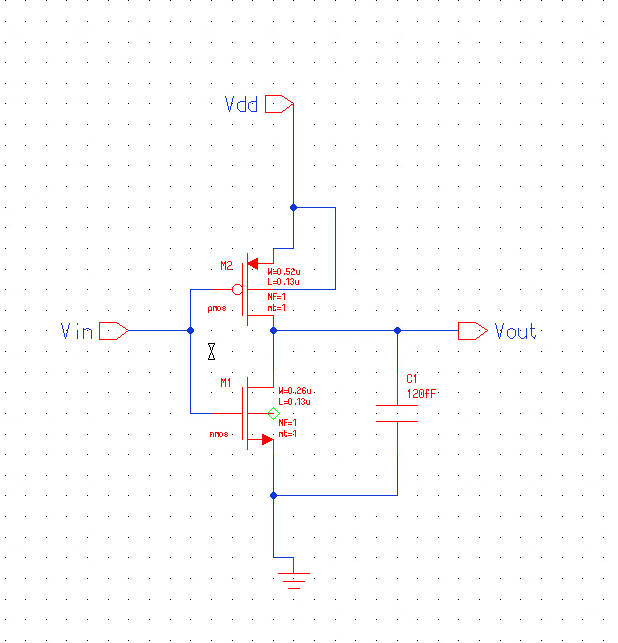
**Fig. 1:** Transistor circuit made with Pyxis

The circuit has a gate input voltage and a drain input voltage. The source and bias terminals are both tied to ground. The transistor is an NMOS and the desired width is 26u meters and the length is 13u meters. This circuit was simulated with voltage sweeps across Vg and Vd. The expected NMOS characteristics are shown in equation 1.

**Equation 1.** NMOS Transistor IV characteristics

CMOS transistor devices have 3 modes of operation. They can be in cutoff where no current flows, the linear region where current flowing is directly related to a voltage difference or they can be in saturation mode. These modes depend on voltage differentials between the drain and the gate. Saturation mode is when the device has maximum current flow. This is a desired state in digital design because it represents a logical 1. The results of simulation are shown in the Results and Analysis section of this exercise.

The next circuit used in the exercise was a CMOS inverter. This circuit consists of an NMOS and a PMOS. There is an input and an output node in this circuit. Figure 2 shows the inverter circuit.



**Fig. 2:** CMOS Transistor Inverter Circuit

The circuit has a capacitive load of 0 or 120 femtofarads depending on the simulation profile. This capacitance is from the output to the source of the NMOS. The NMOS specifications include a width of 26u meters and a length of 13u meters. To have an equivalently powerful PMOS, the width and length must be different. The ratio must be a double of the NMOS. So, the width is 52u meters and the length is 13u meters. Different simulation profiles were applied to this circuit to measure its response. These results are shown in the results and analysis section as well.

# RESULTS & ANALYSIS

This section should be the meat of your report. Here you need to describe in vivid detail exactly what was done. If you simulated something, explain what you simulated and how you simulated it. All of the supporting waveforms, schematics, tables, derivations, etc… should be included in this section (unless directed otherwise by the lab handout). This section should flow very well.

As an example, take a look at the content at the end of this section. The following is shown:

* How to properly include and reference an image
* How the image should look like (properly labeled!!) – Ideally everything including the axes should be readable. For this course, some of the images get to be difficult to render, so that will be excused; however, **if it is not obvious what is happening in your figure then you will lose points**. The TAs should be able to look at the figure and have it immediately support what you are stating.
  + Center figures. If caption exceeds one line, justify the text.
  + Size your figures appropriately (make them readable and no larger)
  + All figures should be properly colored, i.e. white background with black lines. For printing purposes use grayscale.
* How tables should be inserted and formatted
  + Center tables. If caption exceeds one line, justify the text.
* What captions for figures and tables should be like (include lots of details!)

Before continuing, you should note the academic policy. Cheating or plagiarizing of any sort will not be tolerated. You may use this document as a template; however, that is all it may be used for. If you try to pass this example content off as your own, serious consequences will ensue – You have been warned.

The inverter was also tested via transient analysis. A load capacitor, *CL*, was added to the netlist. The rise and fall times (*Tr* and *Tf*), as well as the propagation delay from a high to low signal, *TP,HL*, and a low to high signal, *TP,LH*, were measured for various cases. Fig. 1 shows the worst-case simulation (***make sure you include all of your simulations, not just one – remember that this is just an example***) and Table 1 shows the tabulated results. From Table 1 it is apparent that the worst timings occur when (***make sure to explain your results in good detail, i.e. the worst timings occurred at \_\_ because of \_\_***)….

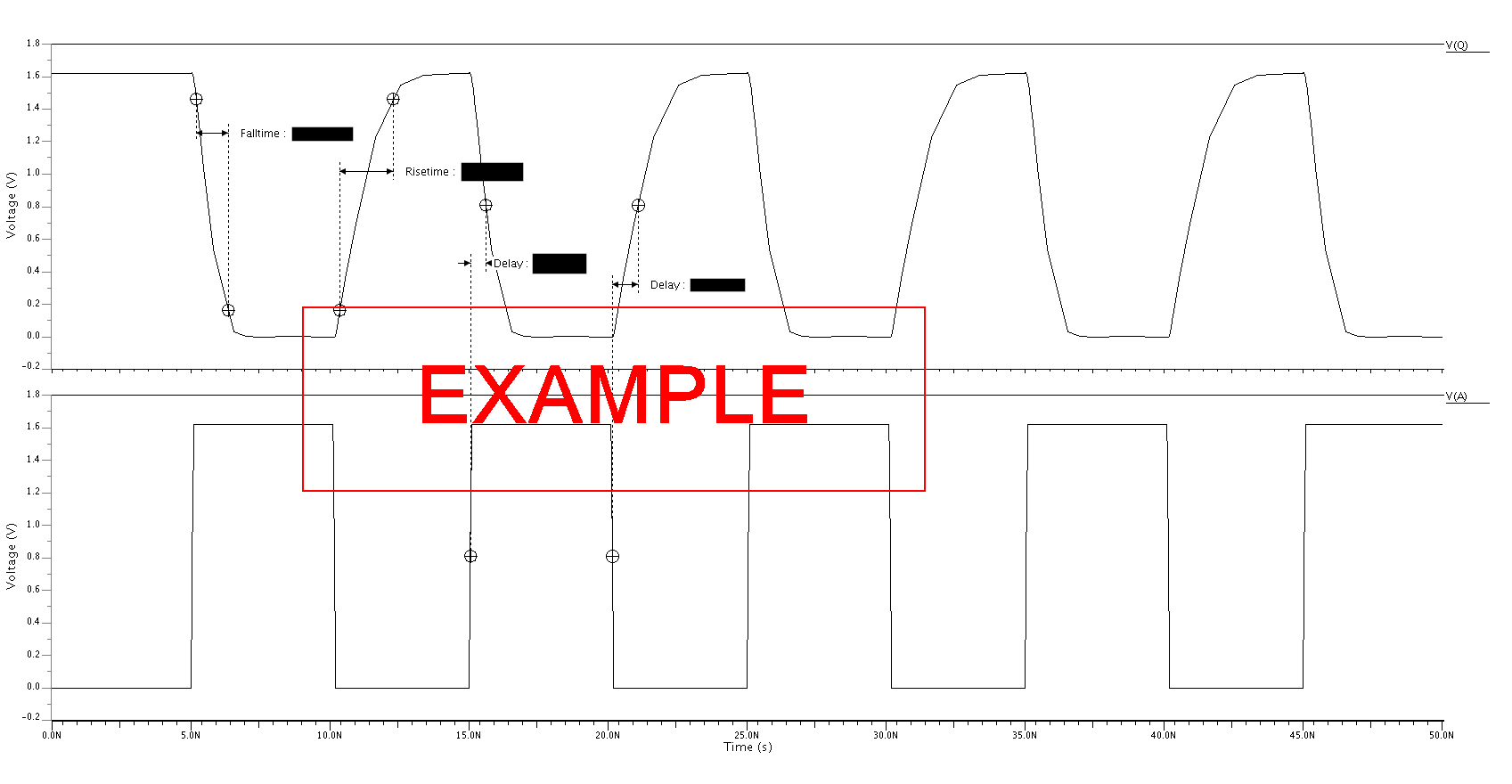


Fig. : Transient analysis of the inverter for the “worst” case (*T* = 125°C, *VDD* = 1.62 V) with *CL* = 120 fF. The measured values are *Tr* = X ns, *Tf* = X ns, *TP,HL* = X ps, and *TP,LH* = X ps.

Table : Timing results for the inverter

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **VDD [V]** | **T [°C]** | **CL [fF]** | **Tr [ps]** | **Tf [ps]** | **TP,HL [ps]** | **TP,LH [ps]** |
| 1.8 | 70 | 0 | X | X | X | X |
| 1.8 | 70 | 120 | X | X | X | X |
| 1.62 | 125 | 0 | X | X | X | X |
| 1.62 | 125 | 120 | X | X | X | X |

# CONCLUSIONS

The conclusion should repeat what you did and what your results were. You should additionally add in any statements about why things happened and possible future work. The conclusion should be between one and two paragraphs.

# QUESTIONS

1. Each question should be numbered and the text repeated, i.e. what you are reading right now should be the question that was in the lab.

And this text should be your answer.

# APPENDICES

In this section, include any items that were requested. Make sure that each item is properly labeled with a useful caption. Additionally, make sure that each item is referenced by your report’s body. Simply having something in the appendix without referencing it is useless. Also, the appendix should always start on a new page.

Some additional note – Make sure to update the references in the table of contents (right click on it, update field, update entire table, ok). If you do that while the entire document is highlighted (ctrl+a) you will update all of the references in your entire document.