Design of CMOS Logic Gates – Lab Number 2

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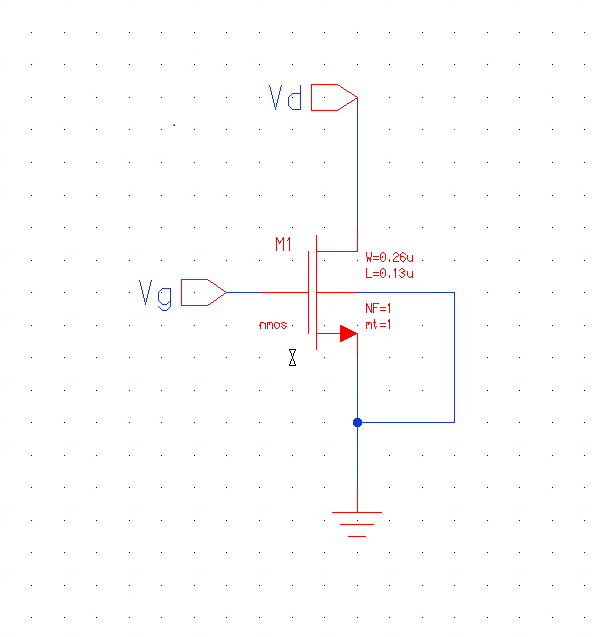
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# ABSTRACT

CMOS device simulation is a valuable tool in digital design. Pyxis Layout, by Mentor Graphics, is a tool that allows for the creation of circuits to a level as specific as transistors. The procedure of exercise 2 was to use this tool to construct a transistor circuit and an inverter circuit with transistors and then use an analog simulation tool called Eldo to simulate the voltage and current characteristics of each. These tools accurately model CMOS devices and allowed for the estimation of the maximum input and throughput frequencies at different voltages, temperatures and capacitive loads. A CMOS modeled with Eldo had a Maximum input frequency of 10.37 Gigahertz and a maximum throughput frequency of 27.71 Gigahertz with no capacitive load. When accounting for a 120 femtofarad load, the inverters maximum input frequency was 297 Megahertz and its maximum throughput was 640.40 Megahertz.

# DESIGN METHODOLOGY

The exercise started with creating a Pyxis schematic with a simple NMOS circuit in it. There is no capacitor attached. Figure 1 shows the circuit that was built for simulation.



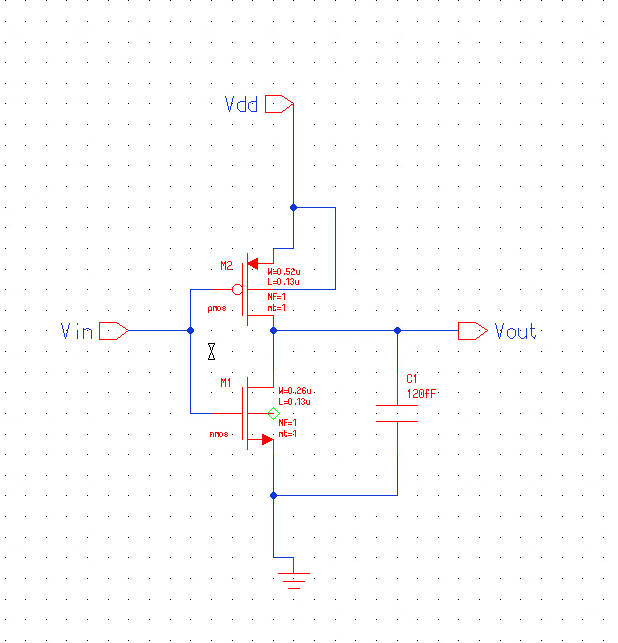
**Fig. 1:** Transistor circuit made with Pyxis

The circuit has a gate input voltage and a drain input voltage. The source and bias terminals are both tied to ground. The transistor is an NMOS and the desired width is 26u meters and the length is 13u meters. This circuit was simulated with voltage sweeps across Vg and Vd. The expected NMOS characteristics are shown in equation 1.

**Equation 1.** NMOS Transistor IV characteristics

CMOS transistor devices have 3 modes of operation. They can be in cutoff where no current flows, the linear region where current flowing is directly related to a voltage difference or they can be in saturation mode. These modes depend on voltage differentials between the drain and the gate. Saturation mode is when the device has maximum current flow. This is a desired state in digital design because it represents a logical 1. The results of simulation are shown in the Results and Analysis section of this exercise.

The next circuit used in the exercise was a CMOS inverter. This circuit consists of an NMOS and a PMOS. There is an input and an output node in this circuit. Figure 2 shows the inverter circuit.



**Fig. 2:** CMOS Transistor Inverter Circuit

The circuit has a capacitive load of 0 or 120 femtofarads depending on the simulation profile. This capacitance is from the output to the source of the NMOS. The NMOS specifications include a width of 26u meters and a length of 13u meters. To have an equivalently powerful PMOS, the width and length must be different. The ratio must be a double of the NMOS. So, the width is 52u meters and the length is 13u meters. Different simulation profiles were applied to this circuit to measure its response. These results are shown in the results and analysis section as well.

# RESULTS & ANALYSIS

**exactly what was done.**

**how you simulated it.**

waveforms, schematics, tables, derivations,

Blank simulations were run on 2 circuits. They were : ………

The first was run with this. It looked like this,. Lookj at this portio here to see this.

Etc.

Fig. 1: Transient analysis of the inverter for the “worst” case (*T* = 125°C, *VDD* = 1.62 V) with *CL* = 120 fF. The measured values are *Tr* = X ns, *Tf* = X ns, *TP,HL* = X ps, and *TP,LH* = X ps.

Table 1: Inverter Results

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **VDD [V]** | **Temp [°C]** | **Load**  **Capacitance [fF]** | **Rise Time[S]** | **Fall Time[S]** | **TP,HL [S]** | **TP,LH [S]** |
| Nominal | 1.2 | 25 | 0 | 5.13E-11 | 2.40E-11 | 2.25E-11 | 1.05E-11 |
| Nominal | 1.8 | 25 | 120 | 1.74E-09 | 9.08E-10 | 4.65E-10 | 8.15E-10 |
| Worst Case | 1.08 | 125 | 0 | 5.39E-11 | 4.26E-11 | 2.33E-11 | 1.28E-11 |
| Worst Case | 1.08 | 125 | 120 | 2.04E-09 | 1.32E-09 | 9.58E-10 | 6.03E-10 |

Table 2: Inverter Results

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **VDD [V]** | **Temp [°C]** | **Load**  **Capacitance [fF]** | **Finput, max [Hz]** | **FThroughput, Max [Hz]** |
| 1.08 | 125 | 0 | 1.037E+10 | 2.771E+10 |
| 1.08 | 125 | 120 | 2.976E+08 | 6.404E+08 |

# CONCLUSIONS

The procedure of exercise 2 was to use Pyxis simulation tools to construct a transistor-based circuits and use an analog simulation tool called Eldo to simulate the voltage and current characteristics of each. These tools both successfully were used to create the circuits and plot their characteristics. It revealed the IV characteristics as expected for the NMOS transistor and was useful in determining the rise and fall times of the circuits. It was also great for finding the time from High to Low in the circuits. With these values, the max input frequency and max throughput frequency were able to be determined. A CMOS modeled with Eldo had a Maximum input frequency of 10.37 Gigahertz and a maximum throughput frequency of 27.71 Gigahertz with no capacitive load. When accounting for a 120 femtofarad load, the inverters maximum input frequency was 297 Megahertz and its maximum throughput was 640.40 Megahertz. The lower frequency is due to the capacitor slowing down the operation of the device. It requires a certain amount of charge, so the device is slowed down as the capacitor charges first.

# QUESTIONS

1. Each question should be numbered and the text repeated, i.e. what you are reading right now should be the question that was in the lab.

And this text should be your answer.