Autolayout Design Techniques (HDL-Layout) – Lab Number 7

**<INSERT SIGNOFF SHEET>**

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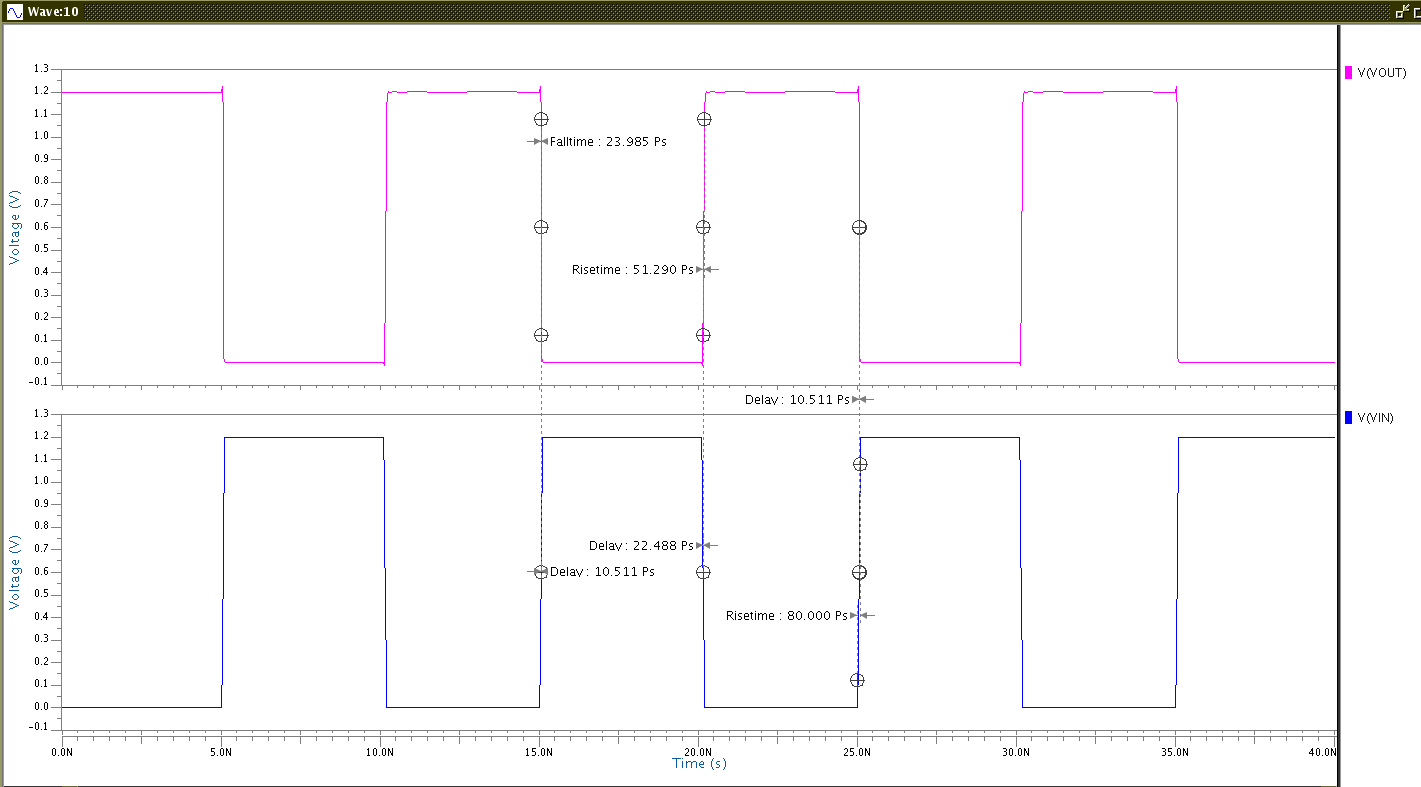
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# ABSTRACT

This exercise involved using VHDL code and Pyxis Layout to generate a physical design of the circuit described in the hardware description language. The procedure involved writing VHDL for a 1 bit and 16 bit ALU with 4 opcodes. The VHDL was functionally tested and the code was then used in Pyxis to create a layout that was then tested in eldo. There were many cases used to determine the performance of the 11 and 16 bit ALU’s. Overall the 1 bit ALU had a **MAX INPUT FREQ AND MAX THRUPUT FREQ and the 16 bit had a MAXINPUT AND THRUPUT of . This exercise was based in the process of generating circuits based on VHDL. Static and dynamic powewre was also measured for the auto routed circuits. The static power and dynamic power of a 1 bit alu are INSERT S^TAT AND DYN. The ostatic and dynamic power for the 16 bit ALU ARE STAT AND DYN. It ended up a success as the process to go from a HDL file to an auto generated layout now routine and repeatable.**

# DESIGN METHODOLOGY

# RESULTS & ANALYSIS



**Fig. 5:** Plotted CMOS Inverter Vin and Vout with 40ns transient analysis with profile (T = 25 degrees C, 1.2V Pulse on Vin swept)

Table 1: Schematic Inverter Results

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **VDD [V]** | **Temp [°C]** | **Load**  **Capacitance [fF]** | **Rise Time[S]** | **Fall Time[S]** | **TP,HL [S]** | **TP,LH [S]** |
| Nominal | 1.2 | 25 | 0 | 5.13E-11 | 2.40E-11 | 2.25E-11 | 1.05E-11 |
| Nominal | 1.2 | 25 | 120 | 1.74E-09 | 9.08E-10 | 4.65E-10 | 8.15E-10 |
| Worst Case | 1.08 | 125 | 0 | 5.39E-11 | 4.26E-11 | 2.33E-11 | 1.28E-11 |
| Worst Case | 1.08 | 125 | 120 | 2.04E-09 | 1.32E-09 | 9.58E-10 | 6.03E-10 |

Equations 1 and 2 are the method of solving for these critical frequencies.

**Equation 1.** F Input Max calculation

**Equation 2.** F throughput max calculation

These equations were used to generate the worst case frequency information in table 3.

Table 3: Inverter Frequencies

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Type** | **VDD [V]** | **Temp [°C]** | **Load**  **Capacitance [fF]** | **Finput, max [Hz]** | **FThroughput, Max [Hz]** |
| Schematic | 1.08 | 125 | 0 | 1.037E+10 | 2.771E+10 |
| Schematic | 1.08 | 125 | 120 | 2.976E+08 | 6.404E+08 |
| Layout | 1.08 | 125 | 0 | 8.331E+09 | 1.647E+10 |
| Layout | 1.08 | 125 | 120 | 2.994E+08 | 6.349E+08 |

# CONCLUSIONS

# QUESTIONS

# APPENDIX

# SOURCES

Rit CMPE Digital IC design lab 7 manual, RIT