Autolayout Design Techniques (HDL-Layout) – Lab Number 7

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Submission Date : 11/14/2019

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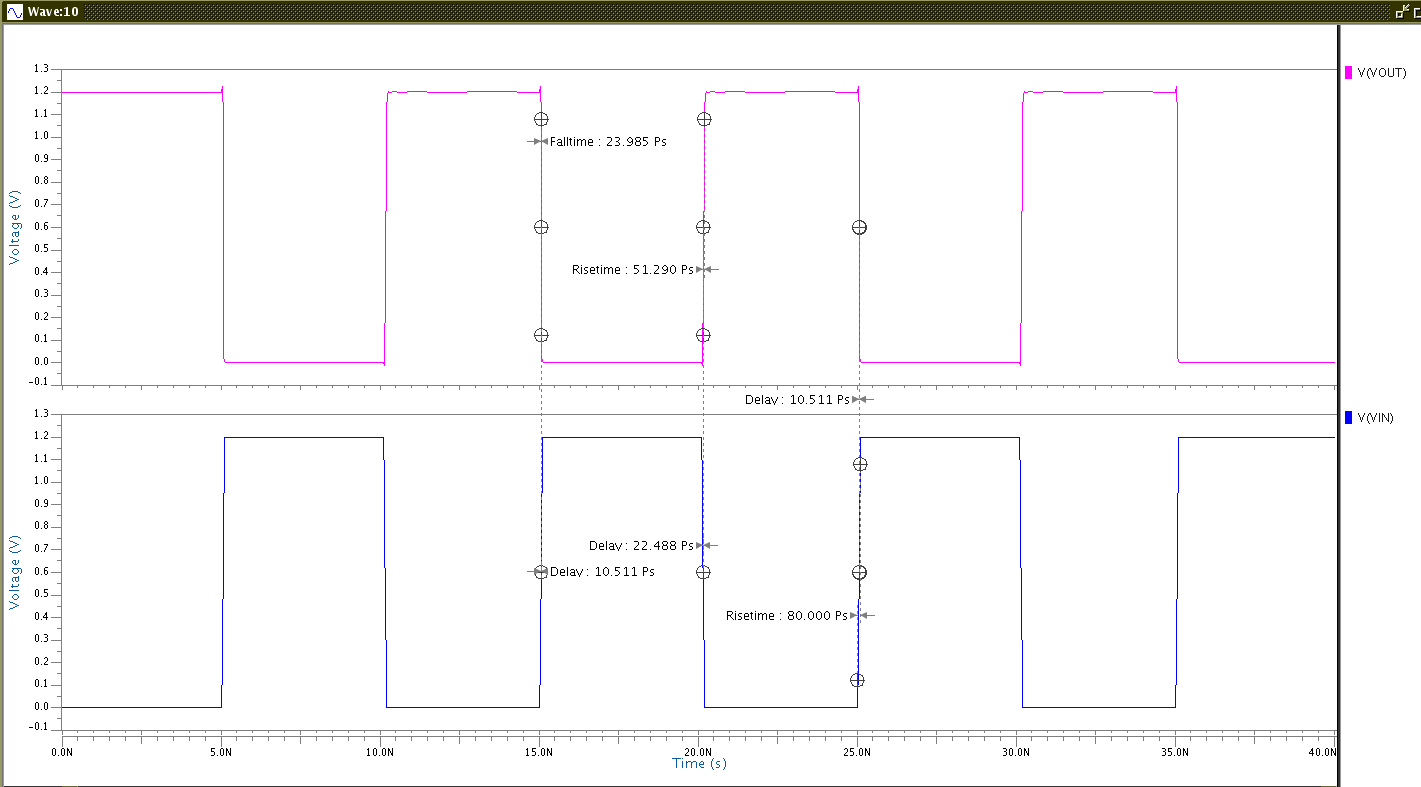
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# ABSTRACT

# DESIGN METHODOLOGY

# RESULTS & ANALYSIS



**Fig. 5:** Plotted CMOS Inverter Vin and Vout with 40ns transient analysis with profile (T = 25 degrees C, 1.2V Pulse on Vin swept)

Table 1: Schematic Inverter Results

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **VDD [V]** | **Temp [°C]** | **Load**  **Capacitance [fF]** | **Rise Time[S]** | **Fall Time[S]** | **TP,HL [S]** | **TP,LH [S]** |
| Nominal | 1.2 | 25 | 0 | 5.13E-11 | 2.40E-11 | 2.25E-11 | 1.05E-11 |
| Nominal | 1.2 | 25 | 120 | 1.74E-09 | 9.08E-10 | 4.65E-10 | 8.15E-10 |
| Worst Case | 1.08 | 125 | 0 | 5.39E-11 | 4.26E-11 | 2.33E-11 | 1.28E-11 |
| Worst Case | 1.08 | 125 | 120 | 2.04E-09 | 1.32E-09 | 9.58E-10 | 6.03E-10 |

Equations 1 and 2 are the method of solving for these critical frequencies.

**Equation 1.** F Input Max calculation

**Equation 2.** F throughput max calculation

These equations were used to generate the worst case frequency information in table 3.

Table 3: Inverter Frequencies

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Type** | **VDD [V]** | **Temp [°C]** | **Load**  **Capacitance [fF]** | **Finput, max [Hz]** | **FThroughput, Max [Hz]** |
| Schematic | 1.08 | 125 | 0 | 1.037E+10 | 2.771E+10 |
| Schematic | 1.08 | 125 | 120 | 2.976E+08 | 6.404E+08 |
| Layout | 1.08 | 125 | 0 | 8.331E+09 | 1.647E+10 |
| Layout | 1.08 | 125 | 120 | 2.994E+08 | 6.349E+08 |

# CONCLUSIONS

# QUESTIONS

# APPENDIX

# SOURCES

Rit CMPE Digital IC design lab 7 manual, RIT