Advanced Digital Integrated Circuits

Design Project: A Wide Operating Range Injection Locking PLL

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1. Abstract

The target of the project is to design a wide operating range phase locked loop (PLL) with minimum power consumption. With Voltage Controlled Oscillator (VCO) having the same resolution, achieving a wide range characteristic has a trade-off with low jitter clock outputs. But by utilizing the **injection locking mechanism**, we mitigated this trade-off relation and successfully implemented the wide range, low output clock jitter, low power analog PLL.

The output clock of our design successfully locks at **2.8Ghz-to-9Ghz range**, and the overall power consumption is about **3.17mW at 2.8Ghz clock output** and **4.31mW at 9Ghz clock output**. The proposed PLL **successfully locks within 10ns** above all operation frequencies. In terms of jitter in 9Ghz clock output, we observed the eye diagram within 11ns range (about 100 samples) after when the PLL has locked, and 12.5ps peak-to-peak jitter is observed. This means our PLL achieves 2**.68ps (2.42%) rms jitter at 9Ghz** clock output when gaussian noise distribution is assumed. But the jitter performance is mainly contributed by the spur generation from injection locking. The phase noise floor is greatly reduced at the cost of spur generations.

2. Overall Design Approach

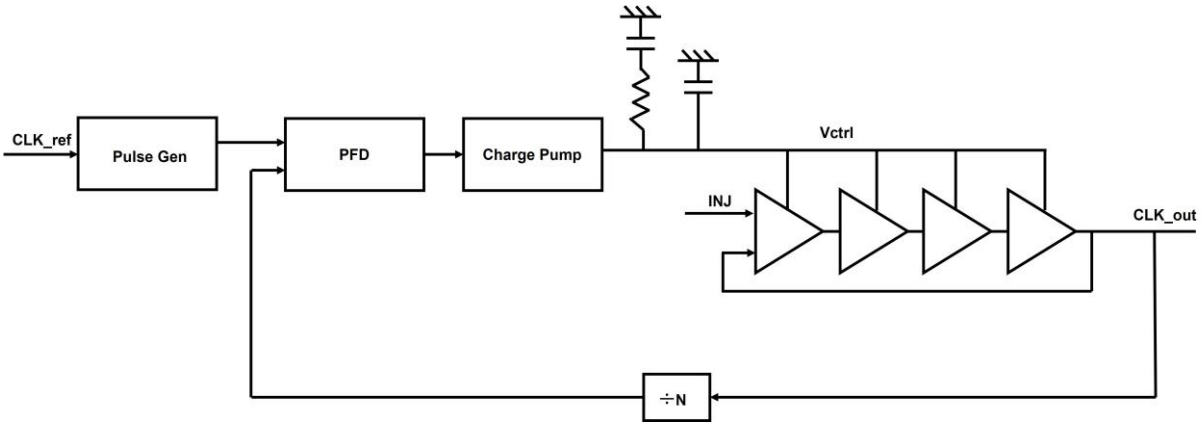


Figure 1. Overall Design Schematic

It is widely known that a maximum achievable PLL bandwidth is 1/10 of the reference frequency. But for low power / low spur operation, low charge pump current is highly preferred, which leads to the limitation of the bandwidth. Therefore, we doubled the frequency of the reference clock by implementing a **XOR based pulse generation circuit** to achieve the same PLL bandwidth with lowered charge pump current. Since the phase-frequency detector only detects the rising edge of the inputs, duty cycle correction is not implemented.

A VCO is also indeed a critical block in the design of a PLL. As it directly produces the output clock signals, its gain (Kvco [rad/V]) plays a significant role in the PLL operation. If Kvco is large, output phase noise and reference spur magnitude increase as noise signals from charge pump and loop filter are amplified through Kvco gain. On the other hand, if Kvco is small, overall operation range of PLL

decreases. Therefore, a differential ring-type **VCO with high gain** is used for wide range operation. In addition, **injection-locking mechanism** is utilized to compensate the poor output clock jitter performance due to high VCO gain.

Since we doubled the reference frequency, **the divider with N=4 is implemented** to make the output clock frequency 8 times the frequency of the reference clock, and the PLL bandwidth is doubled. Also, since one D-Flipflop is saved compared to the divider with N=8, the loop latency is reduced which also contributes to the reduced phase noise.

3. Schematic of the Blocks

A. Pulse Generator

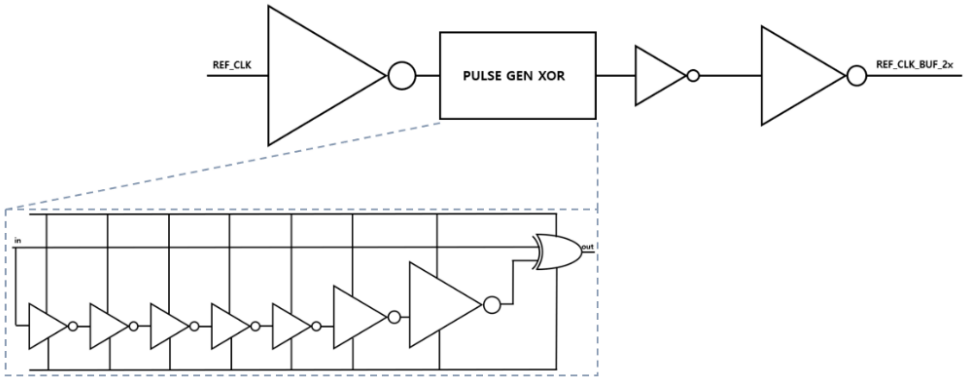
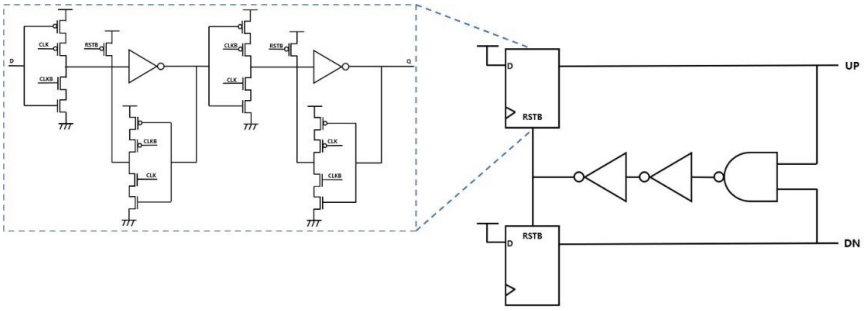


Figure 2. Pulse Generator Schematic

A pulse generator is used to generate the input *pulse* signal from reference clock with doubled frequency [1]. A simple XOR gate is implemented with multiple delay cells to set the delay sufficient for pulse generation. Buffers are also implemented regarding the fanouts.

B. Phase Frequency Detector (PFD)

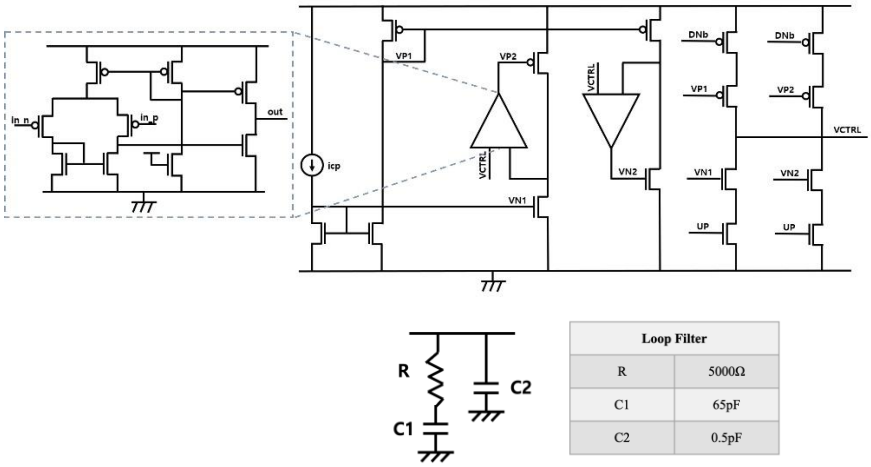


D_Flip_Flop	
PMOS	1um / 45nm
NMOS	500nm / 45nm

Figure 3. PFD Schematic

Conventional PFD structure, which contains two resettable d-flip-flops and a nand gate, is used to generate the UP/DN signals. 2 additional PMOS are used to reset the PFD when both UP/DN is on.

C. Charge Pump and Loop Filter



Charge Pump	
PMOS	1um / 45nm
NMOS	500nm / 45nm
Op-Amp	
PMOS	1um / 45nm
NMOS	500nm / 45nm

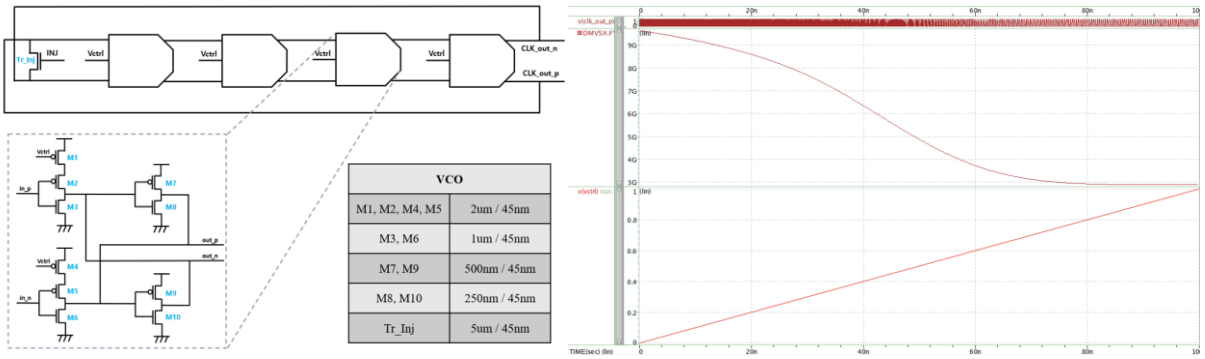
Loop Filter	
R	5000Ω
C1	65pF
C2	0.5pF

Figure 4. Charge Pump and Loop Filter Schematic

Two op-amps [2] are implemented to stabilize the Vctrl signal, and this leads to the minimization of UP/DN signal mismatch [3]. To be specific, not only the VN1/VP1 signals made by the current mirror structure are used to produce the control voltage. Additional signals VN2/VP2, which are generated by the op-amp, are used to stabilize the Vctrl.

Also, the value of Icp is halved (200uA) since input pulse has doubled frequency compared to the reference clock signal; such result clearly minimizes power consumption in the charge pump. The charge pump current could be optimized by tuning the parameters including the loop filter components. Resistor value in the loop filter is currently 5k ohm, and the capacitances are 63pF and 0.5pF.

D. Voltage-Controlled Oscillator (VCO) with injection locking mechanism



VCO	
M1, M2, M4, M5	2um / 45nm
M3, M6	1um / 45nm
M7, M9	500nm / 45nm
M8, M10	250nm / 45nm
Tr_Inj	5um / 45nm

Figure 5. VCO Schematic and VCO Characteristic

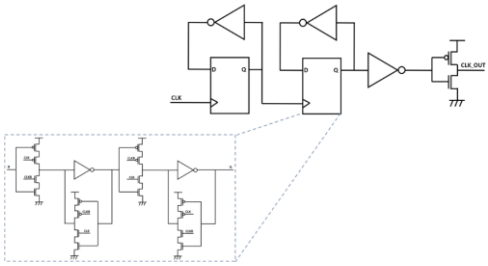
To minimize the overall power consumption of the PLL, differential four-stage ring type VCO is used to generate the output clock signal. Each stage is designed with a symmetrical structure with a controllable PMOS switch. For better linearity of the VCO, current mirror structure could be used to control the output clock frequency. But since it has a static current, this leads to the increase of power consumption. In our case, we omitted the current mirror inside the VCO, and this structure is possible since Vctrl is strongly stabilized by the op-amps used in the charge pump.

In addition, a NMOS transistor switch is added to the feedback loop to align the edge of the output clock signal to the rising edge of the input pulse signal. This injection mechanism helps improve the jitter performance of the VCO.

In terms of VCO characteristics as shown in figure 5, linear operation is observed for frequency range between 4GHz to 9GHz, and down to 2.8GHz is achievable. There is an inevitable trade-off between

power consumption and operation range; above VCO design aims for low power operation with reasonable frequency range.

E. Frequency Divider



D_Flip_Flop	
PMOS	1um / 45nm
NMOS	500nm / 45nm

Figure 6. Divider Schematic

As the frequency of input signal is doubled by pulse generator, division ratio is decreased to 4. Two d-flop-flops are connected in series to produce quarter rate signal from the output clock signal. Loop latency decrease by using only 2 d-flip-flops also positively contributes to the PLL performance.

4. Simulation Results

A. Functionality & Power consumptions

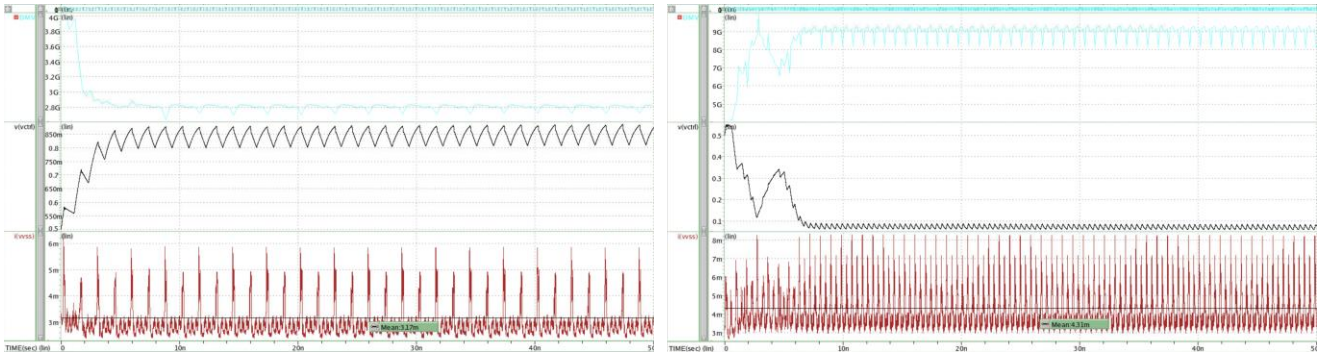


Figure 7. Frequency conversion & Power consumption results at 2.8Ghz(left) and 9Ghz(right) clock output

Figure 7 shows the functionality of the PLL. It is proven that our PLL successfully generates the output clock from 2.8Ghz to 9Ghz at 1V supply voltage, with Vctrl initial voltage of 0.5V. The overall structure consumes less than 5mW total, which is the result of the usage of low power VCO.

B. Jitter

The measured peak-to-peak jitter was 12.5ps for both 2.8Ghz (from 14ns to 50ns) and 9Ghz (from 39ns to 50ns) output clock. If we assume that the noise is gaussian, the standard deviation for 100 samples is 2.327, and the rms jitter is calculated as 2.686ps [4]. This value is 0.75% of the 2.8Ghz clock period, and 2.42% of the 9Ghz clock period. As shown in the graph of VCO in figure 5, the gain of the VCO is small at 2.8Ghz clock output, and this led to the relatively low rms jitter for 2.8Ghz output clock.

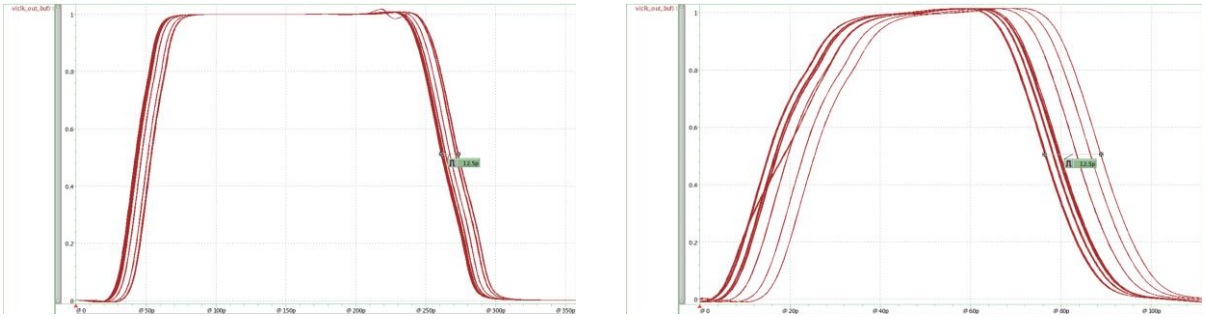


Figure 8. Measured eye diagram (peak-to-peak jitter) at 2.8Ghz(left) and 9Ghz(right) clock outputs

C. Injection mechanism

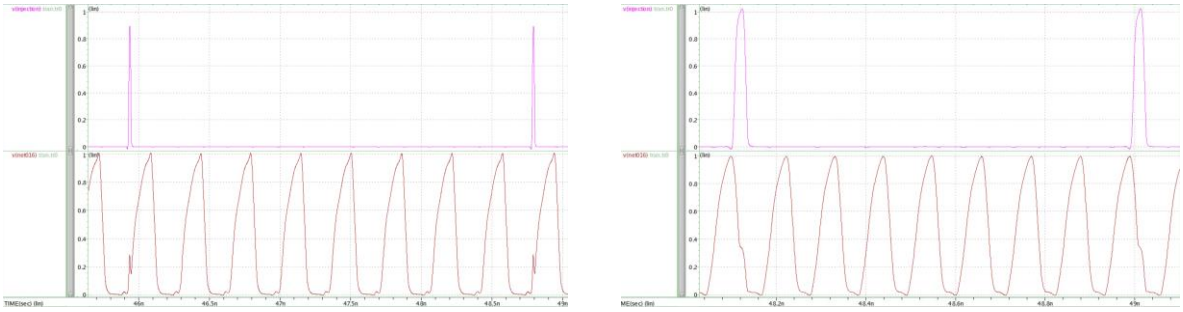


Figure 8. Injection operations at 2.8Ghz(left) and 9Ghz(right) clock outputs

It is also observed that the injection mechanisms are properly applied to the output of the VCO. If the timing delay of the injection is more optimized, the spur generated by the injection could be mitigated.

5. Relevant Calculations

$$K_c = \frac{C_1}{C_2} = 2\left(\tan\varphi_M{}^2 + \tan\varphi_M\sqrt{\tan\varphi_M{}^2 + 1}\right)$$

$$For\ a\ stable\ loop, let\ \varphi_M = 80°. Then,$$

$$K_c = \frac{C_1}{C_2} \approx 130, let\ C_2 = 0.5pF, C_1 = 65pF$$

$$With\ above\ PLL\ structure,$$

$$\omega_{BW} \approx \frac{\omega_{in}}{10} = \frac{\omega_{ref}}{5} = \frac{K_{VCO}\cdot I_{cp}\cdot R_1}{4\cdot 2\pi}$$

$$Let\ R_1 = 5k\Omega\ , then\ for\ \omega_{ref,max} = 1.125GHz,$$

$$I_{cp} = 194.995\mu A \approx 200\mu A$$

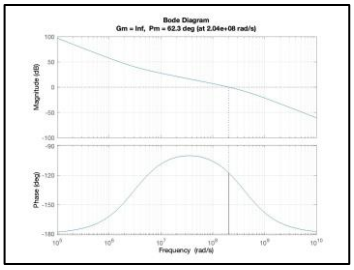


Figure 10. Parameter Calculation and Loop Gain Bode Plot

Phase margin of 80 degrees with 9Ghz bandwidth was our objective. Since the division ratio was 8, maximum reference clock is calculated as 1.125Ghz. Figure 10 shows the result of our calculations for obtaining the parameter values, and loop gain bode plot is also shown corresponding to the parameters.

6. Reference

[1] ISSCC, Hyojun Kim, Hyeong-Seok Oh, Woosong Jung, Yoonho Song, Jonghyun Oh, Deog-Kyoon Jeong, 17 March 2022, “A 100MHz-Reference, 8GHz/16GHz, 177fsrms/223fsrms RO-Based IL-ADPLL Incorporating Reference Octupler with Probability-Based Fast Phase-Error Calibration”

[2] IEEE Electron Device Letters, Aashit Kamath, Zhixian Chen, Negar Shen, Navab Singh, G. Q. Lo, Dim-Lee Kwong, Dominik Kasprowicz, Andrzej Pfitzner, Wojciech P. Maly, February 2012, “Realizing AND and OR Functions With Single Vertical-Slit Field-Effect Transistor”

[3] ISSCC, Kwanseo Park, Woorham Bae, Jinhyung Lee, Jeongho Hwang, Deog-Kyoon Jeong, 3 September 2018, “A 6.7-11.2 Gb/s, 2.25 pJ/bit, Single-Loop Referenceless CDR With Multi-Phase, Oversampling PFD in 65-nm CMOS”

[4] SiTime, 4 April 2019, “Clock Jitter Definitions and Measurement Methods”