Advanced Digital Integrated Circuits
Design Project (Due: 06/20/2023 23:59)

The objective of this project is to design a wide operating range PLL. The primary goal is to achieve the specifications given in Table 1 with minimum power consumption.

Table 1. PLL Specifications

Technology	SNU 45nm CMOS
Supply Voltage (V_{DD})	≤ 1.0 V
Output Frequency	0.5 ~ 10 GHz
Divide Ratio	8
Input Frequency	62.5 ~ 1250 MHz
Output Clock Jitter (rms)	≤ 0.1% (of T_{VCO})
Power	Minimum

Report Guidelines

The report should describe all the design choices you made with justification, present relevant simulation results and should **not exceed 5 pages**. The report should strictly adhere to the following outlines:

(1) Overall design approach with emphasis on trade-offs and design choices made to arrive at your PLL architecture should be presented in the first two pages. You should explain your design decisions and compare the tradeoffs with alternative choices.

(2) Clearly drawn complete schematic of each block in PLL (do not cut-and-paste Cadence schematic) along with tabulated device sizes and bias currents of the key devices should be shown in the second and third pages.

(3) Clearly annotated simulated results should be presented in page 4.

(4) All the relevant calculations to achieve the simulated performance should be provided in page 5.

(5) Use LaTex or MS WORD to type-set your report and name the report as: lastname1_lastname2_project.pdf