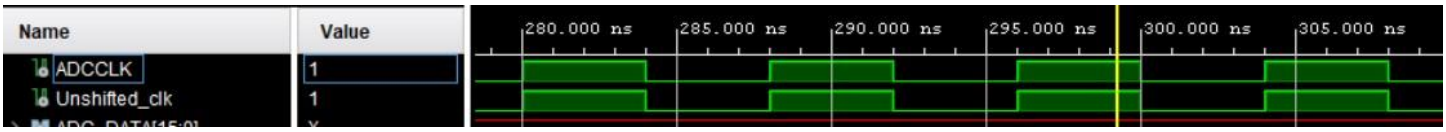
Question #1:

At startup, before any phase incrementing has been done by the testbench, what is the phase offset in degrees between the input clock and your created ADC clock?

Prior to any phase shifting, the ADC-CLK and unshifted clock are in phase with each other and therefore have a phase offset of 0°.



Question #2:

How many properly executed PSINCs are needed to rotate the ADC-CLK a full 360 degrees back to where it started in relation to the unshifted clock?

Each PSINC shifts the ADC-CLK by $17.9ps$ in relation to the unshifted clock. A full 360-degree rotation is equivalent to shifting one period of the 125 MHz clock rate:

$$\frac{T_{clk}}{phase\ increment} = \frac{1/(125 \times 10^6)}{17.9 \times 10^{-12}} \approx 447$$

Therefore, 447 properly executed PSINCs are needed to phase shift the ADC-CLK 360 degrees in relation to the unshifted clock.

Question #3:

For each valid PSINC completed by the clock wizard, how much time shift of the ADC-clock is achieved (in picoseconds please)

The time shift of a PSINC increment is given by:

$$\frac{1}{56 * F_{VCO}}$$

The F_{VCO} for the clocking wizard in the provided design is 1000 MHz per the IP configuration wizard.

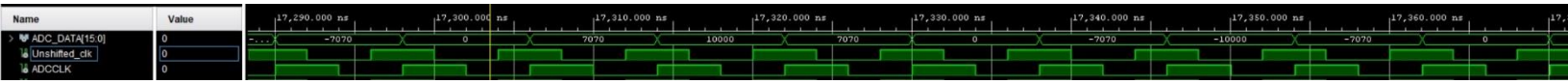
$$\frac{1}{56 * 10^9} = 17.9$$

Therefore, for each PSINC completed, the ADC-CLK is time shifted by 17.9 picoseconds.

Question #4:

If you were asked to pick the perfect phase shift in degrees to align the ADC-Clock with the input clock, what would it be?

The valid data pattern appears to be between 56 and 168 PSINCs which correlate to between $1002.4ps$ and $3007.2\ ps$ of time-shift. Taking these as the boundaries of the eye diagram, the "perfect phase shift" would be in the center of the eye which is 112 PSINCs or 2004.8ps of time shift which equates to roughly a $90°$ phase shift. Below is the data pattern at that point:



Question #5:

Upload your project here, or provide a link to a git repository which I can clone. The project should simulate and if run for a sufficient amount of time, should show the valid ADC numbers from the 8-point sine-wave with amplitude 10000.

The Vivado project has been uploaded here: https://github.com/brianmedendorp/lab8

Question #6:

In your simulation, at what simulation time (in ns) is the ideal ADC shift point reached? (The instructor will run your simulation to this time in ns and hope to see valid data being captured on the output data)

The ideal ADC shift point occurs at approximately the $17280\ ns$ timestamp.